What is "**Embedded - Microcontrollers**"?

"**Embedded - Microcontrollers**" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "**Embedded - Microcontrollers**"

Details	
Product Status	Last Time Buy
Core Processor	XC800
Core Size	8-Bit
Speed	24MHz
Connectivity	LINbus, SSI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	34
Program Memory Size	24KB (24K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	1.75K x 8
Voltage - Supply (Vcc/Vdd)	4.5V ~ 5.5V
Data Converters	A/D 8x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	48-LQFP
Supplier Device Package	PG-TQFP-48
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/xc886lm6ffa5vackxuma1

3.2.2 Special Function Register

The Special Function Registers (SFRs) occupy direct internal data memory space in the range 80_H to FF_H. All registers, except the program counter, reside in the SFR area. The SFRs include pointers and registers that provide an interface between the CPU and the on-chip peripherals. As the 128-SFR range is less than the total number of registers required, address extension mechanisms are required to increase the number of addressable SFRs. The address extension mechanisms include:

• Mapping
• Paging

3.2.2.1 Address Extension by Mapping

Address extension is performed at the system level by mapping. The SFR area is extended into two portions: the standard (non-mapped) SFR area and the mapped SFR area. Each portion supports the same address range 80_H to FF_H, bringing the number of addressable SFRs to 256. The extended address range is not directly controlled by the CPU instruction itself, but is derived from bit RMAP in the system control register SYSCON0 at address $8F_H$. To access SFRs in the mapped area, bit RMAP in SFR SYSCON0 must be set. Alternatively, the SFRs in the standard area can be accessed by clearing bit RMAP. The SFR area can be selected as shown in **Figure 8**.

As long as bit RMAP is set, the mapped SFR area can be accessed. This bit is not cleared automatically by hardware. Thus, before standard/mapped registers are accessed, bit RMAP must be cleared/set, respectively, by software.

3.2.4 XC886/888 Register Overview

The SFRs of the XC886/888 are organized into groups according to their functional units. The contents (bits) of the SFRs are summarized in **Chapter 3.2.4.1** to **Chapter 3.2.4.14**.

Note: The addresses of the bitaddressable SFRs appear in bold typeface.

3.2.4.1 CPU Registers

The CPU SFRs can be accessed in both the standard and mapped memory areas (RMAP = 0 or 1).

Table 5   CPU Register Overview

Addr	Register Name	Bit	7	6	5	4	3	2	1	0
RMAP = 0 or 1										
81$_H$	**SP** Reset: 07$_H$ Stack Pointer Register	Bit Field				SP				
		Type				rw				
82$_H$	**DPL** Reset: 00$_H$ Data Pointer Register Low	Bit Field	DPL7	DPL6	DPL5	DPL4	DPL3	DPL2	DPL1	DPL0
		Type	rw	rw	rw	rw	rw	rw	rw	rw
83$_H$	**DPH** Reset: 00$_H$ Data Pointer Register High	Bit Field	DPH7	DPH6	DPH5	DPH4	DPH3	DPH2	DPH1	DPH0
		Type	rw	rw	rw	rw	rw	rw	rw	rw
87$_H$	**PCON** Reset: 00$_H$ Power Control Register	Bit Field	SMOD		0		GF1	GF0	0	IDLE
		Type	rw		r		rw	rw	r	rw
88$_H$	**TCON** Reset: 00$_H$ Timer Control Register	Bit Field	TF1	TR1	TF0	TR0	IE1	IT1	IE0	IT0
		Type	rwh	rw	rwh	rw	rwh	rw	rwh	rw
89$_H$	**TMOD** Reset: 00$_H$ Timer Mode Register	Bit Field	GATE1	T1S	T1M		GATE0	T0S	T0M	
		Type	rw	rw	rw		rw	rw	rw	
8A$_H$	**TL0** Reset: 00$_H$ Timer 0 Register Low	Bit Field				VAL				
		Type				rwh				
8B$_H$	**TL1** Reset: 00$_H$ Timer 1 Register Low	Bit Field				VAL				
		Type				rwh				
8C$_H$	**TH0** Reset: 00$_H$ Timer 0 Register High	Bit Field				VAL				
		Type				rwh				
8D$_H$	**TH1** Reset: 00$_H$ Timer 1 Register High	Bit Field				VAL				
		Type				rwh				
98$_H$	**SCON** Reset: 00$_H$ Serial Channel Control Register	Bit Field	SM0	SM1	SM2	REN	TB8	RB8	TI	RI
		Type	rw	rw	rw	rw	rw	rwh	rwh	rwh
99$_H$	**SBUF** Reset: 00$_H$ Serial Data Buffer Register	Bit Field				VAL				
		Type				rwh				
A2$_H$	**EO** Reset: 00$_H$ Extended Operation Register	Bit Field		0		TRAP_EN		0		DPSEL0
		Type		r		rw		r		rw

Table 6   MDU Register Overview (cont'd)

Addr	Register Name	Bit	7	6	5	4	3	2	1	0
B3$_H$	**MR1** Reset: 00$_H$ MDU Result Register 1	Bit Field	DATA							
		Type	rh							
B4$_H$	**MD2** Reset: 00$_H$ MDU Operand Register 2	Bit Field	DATA							
		Type	rw							
B4$_H$	**MR2** Reset: 00$_H$ MDU Result Register 2	Bit Field	DATA							
		Type	rh							
B5$_H$	**MD3** Reset: 00$_H$ MDU Operand Register 3	Bit Field	DATA							
		Type	rw							
B5$_H$	**MR3** Reset: 00$_H$ MDU Result Register 3	Bit Field	DATA							
		Type	rh							
B6$_H$	**MD4** Reset: 00$_H$ MDU Operand Register 4	Bit Field	DATA							
		Type	rw							
B6$_H$	**MR4** Reset: 00$_H$ MDU Result Register 4	Bit Field	DATA							
		Type	rh							
B7$_H$	**MD5** Reset: 00$_H$ MDU Operand Register 5	Bit Field	DATA							
		Type	rw							
B7$_H$	**MR5** Reset: 00$_H$ MDU Result Register 5	Bit Field	DATA							
		Type	rh							

3.2.4.3   CORDIC Registers

The CORDIC SFRs can be accessed in the mapped memory area (RMAP = 1).

Table 7   CORDIC Register Overview

Addr	Register Name	Bit	7	6	5	4	3	2	1	0
RMAP = 1										
9A$_H$	**CD_CORDXL** Reset: 00$_H$ CORDIC X Data Low Byte	Bit Field	DATAL							
		Type	rw							
9B$_H$	**CD_CORDXH** Reset: 00$_H$ CORDIC X Data High Byte	Bit Field	DATAH							
		Type	rw							
9C$_H$	**CD_CORDYL** Reset: 00$_H$ CORDIC Y Data Low Byte	Bit Field	DATAL							
		Type	rw							
9D$_H$	**CD_CORDYH** Reset: 00$_H$ CORDIC Y Data High Byte	Bit Field	DATAH							
		Type	rw							
9E$_H$	**CD_CORDZL** Reset: 00$_H$ CORDIC Z Data Low Byte	Bit Field	DATAL							
		Type	rw							
9F$_H$	**CD_CORDZH** Reset: 00$_H$ CORDIC Z Data High Byte	Bit Field	DATAH							
		Type	rw							

Table 8   SCU Register Overview (cont'd)

Addr	Register Name	Bit	7	6	5	4	3	2	1	0
BE$_H$	**COCON** Reset: 00$_H$ Clock Output Control Register	Bit Field	0		TLEN	COUTS	COREL			
		Type	r		rw	rw	rw			
E9$_H$	**MISC_CON** Reset: 00$_H$ Miscellaneous Control Register	Bit Field	0							DFLASHEN
		Type	r							rwh
RMAP = 0, PAGE 3										
B3$_H$	**XADDRH** Reset: F0$_H$ On-chip XRAM Address Higher Order	Bit Field	ADDRH							
		Type	rw							
B4$_H$	**IRCON3** Reset: 00$_H$ Interrupt Request Register 3	Bit Field	0		CANSRC5	CCU6SR1	0		CANSRC4	CCU6SR0
		Type	r		rwh	rwh	r		rwh	rwh
B5$_H$	**IRCON4** Reset: 00$_H$ Interrupt Request Register 4	Bit Field	0		CANSRC7	CCU6SR3	0		CANSRC6	CCU6SR2
		Type	r		rwh	rwh	r		rwh	rwh
B7$_H$	**MODPISEL1** Reset: 00$_H$ Peripheral Input Select Register 1	Bit Field	EXINT6IS	0		UR1RIS		T21EXIS	JTAGTDIS1	JTAGTCKS1
		Type	rw	r		rw		rw	rw	rw
BA$_H$	**MODPISEL2** Reset: 00$_H$ Peripheral Input Select Register 2	Bit Field	0				T21IS	T2IS	T1IS	T0IS
		Type	r				rw	rw	rw	rw
BB$_H$	**PMCON2** Reset: 00$_H$ Power Mode Control Register 2	Bit Field	0						UART1_DIS	T21_DIS
		Type	r						rw	rw
BD$_H$	**MODSUSP** Reset: 01$_H$ Module Suspend Control Register	Bit Field	0			T21SUSP	T2SUSP	T13SUSP	T12SUSP	WDTSUSP
		Type	r			rw	rw	rw	rw	rw

3.2.4.5   WDT Registers

The WDT SFRs can be accessed in the mapped memory area (RMAP = 1).

Table 9   WDT Register Overview

Addr	Register Name	Bit	7	6	5	4	3	2	1	0
RMAP = 1										
BB$_H$	**WDTCON** Reset: 00$_H$ Watchdog Timer Control Register	Bit Field	0		WINBEN	WDTPR	0	WDTEN	WDTRS	WDTIN
		Type	r		rw	rh	r	rw	rwh	rw
BC$_H$	**WDTREL** Reset: 00$_H$ Watchdog Timer Reload Register	Bit Field	WDTREL							
		Type	rw							
BD$_H$	**WDTWINB** Reset: 00$_H$ Watchdog Window-Boundary Count Register	Bit Field	WDTWINB							
		Type	rw							

Table 10   Port Register Overview (cont'd)

Addr	Register Name	Bit	7	6	5	4	3	2	1	0
RMAP = 0, PAGE 1										
80$_H$	**P0_PUDSEL**　　　**Reset: FF$_H$** P0 Pull-Up/Pull-Down Select Register	Bit Field	P7	P6	P5	P4	P3	P2	P1	P0
		Type	rw	rw	rw	rw	rw	rw	rw	rw
86$_H$	**P0_PUDEN**　　　**Reset: C4$_H$** P0 Pull-Up/Pull-Down Enable Register	Bit Field	P7	P6	P5	P4	P3	P2	P1	P0
		Type	rw	rw	rw	rw	rw	rw	rw	rw
90$_H$	**P1_PUDSEL**　　　**Reset: FF$_H$** P1 Pull-Up/Pull-Down Select Register	Bit Field	P7	P6	P5	P4	P3	P2	P1	P0
		Type	rw	rw	rw	rw	rw	rw	rw	rw
91$_H$	**P1_PUDEN**　　　**Reset: FF$_H$** P1 Pull-Up/Pull-Down Enable Register	Bit Field	P7	P6	P5	P4	P3	P2	P1	P0
		Type	rw	rw	rw	rw	rw	rw	rw	rw
92$_H$	**P5_PUDSEL**　　　**Reset: FF$_H$** P5 Pull-Up/Pull-Down Select Register	Bit Field	P7	P6	P5	P4	P3	P2	P1	P0
		Type	rw	rw	rw	rw	rw	rw	rw	rw
93$_H$	**P5_PUDEN**　　　**Reset: FF$_H$** P5 Pull-Up/Pull-Down Enable Register	Bit Field	P7	P6	P5	P4	P3	P2	P1	P0
		Type	rw	rw	rw	rw	rw	rw	rw	rw
A0$_H$	**P2_PUDSEL**　　　**Reset: FF$_H$** P2 Pull-Up/Pull-Down Select Register	Bit Field	P7	P6	P5	P4	P3	P2	P1	P0
		Type	rw	rw	rw	rw	rw	rw	rw	rw
A1$_H$	**P2_PUDEN**　　　**Reset: 00$_H$** P2 Pull-Up/Pull-Down Enable Register	Bit Field	P7	P6	P5	P4	P3	P2	P1	P0
		Type	rw	rw	rw	rw	rw	rw	rw	rw
B0$_H$	**P3_PUDSEL**　　　**Reset: BF$_H$** P3 Pull-Up/Pull-Down Select Register	Bit Field	P7	P6	P5	P4	P3	P2	P1	P0
		Type	rw	rw	rw	rw	rw	rw	rw	rw
B1$_H$	**P3_PUDEN**　　　**Reset: 40$_H$** P3 Pull-Up/Pull-Down Enable Register	Bit Field	P7	P6	P5	P4	P3	P2	P1	P0
		Type	rw	rw	rw	rw	rw	rw	rw	rw
C8$_H$	**P4_PUDSEL**　　　**Reset: FF$_H$** P4 Pull-Up/Pull-Down Select Register	Bit Field	P7	P6	P5	P4	P3	P2	P1	P0
		Type	rw	rw	rw	rw	rw	rw	rw	rw
C9$_H$	**P4_PUDEN**　　　**Reset: 04$_H$** P4 Pull-Up/Pull-Down Enable Register	Bit Field	P7	P6	P5	P4	P3	P2	P1	P0
		Type	rw	rw	rw	rw	rw	rw	rw	rw
RMAP = 0, PAGE 2										
80$_H$	**P0_ALTSEL0**　　　**Reset: 00$_H$** P0 Alternate Select 0 Register	Bit Field	P7	P6	P5	P4	P3	P2	P1	P0
		Type	rw	rw	rw	rw	rw	rw	rw	rw
86$_H$	**P0_ALTSEL1**　　　**Reset: 00$_H$** P0 Alternate Select 1 Register	Bit Field	P7	P6	P5	P4	P3	P2	P1	P0
		Type	rw	rw	rw	rw	rw	rw	rw	rw
90$_H$	**P1_ALTSEL0**　　　**Reset: 00$_H$** P1 Alternate Select 0 Register	Bit Field	P7	P6	P5	P4	P3	P2	P1	P0
		Type	rw	rw	rw	rw	rw	rw	rw	rw
91$_H$	**P1_ALTSEL1**　　　**Reset: 00$_H$** P1 Alternate Select 1 Register	Bit Field	P7	P6	P5	P4	P3	P2	P1	P0
		Type	rw	rw	rw	rw	rw	rw	rw	rw
92$_H$	**P5_ALTSEL0**　　　**Reset: 00$_H$** P5 Alternate Select 0 Register	Bit Field	P7	P6	P5	P4	P3	P2	P1	P0
		Type	rw	rw	rw	rw	rw	rw	rw	rw

3.2.4.8 Timer 2 Registers

The Timer 2 SFRs can be accessed in the standard memory area (RMAP = 0).

Table 12   T2 Register Overview

Addr	Register Name	Bit	7	6	5	4	3	2	1	0
RMAP = 0										
C0$_H$	**T2_T2CON** **Reset: 00**$_H$ Timer 2 Control Register	Bit Field	TF2	EXF2	0		EXEN2	TR2	C/$\overline{T2}$	CP/$\overline{RL2}$
		Type	rwh	rwh	r		rw	rwh	rw	rw
C1$_H$	**T2_T2MOD** **Reset: 00**$_H$ Timer 2 Mode Register	Bit Field	T2REGS	T2RHEN	EDGESEL	PREN	T2PRE			DCEN
		Type	rw	rw	rw	rw	rw	rw	rw	rw
C2$_H$	**T2_RC2L** **Reset: 00**$_H$ Timer 2 Reload/Capture Register Low	Bit Field	RC2							
		Type	rwh							
C3$_H$	**T2_RC2H** **Reset: 00**$_H$ Timer 2 Reload/Capture Register High	Bit Field	RC2							
		Type	rwh							
C4$_H$	**T2_T2L** **Reset: 00**$_H$ Timer 2 Register Low	Bit Field	THL2							
		Type	rwh							
C5$_H$	**T2_T2H** **Reset: 00**$_H$ Timer 2 Register High	Bit Field	THL2							
		Type	rwh							

3.2.4.9 Timer 21 Registers

The Timer 21 SFRs can be accessed in the mapped memory area (RMAP = 1).

Table 13   T21 Register Overview

Addr	Register Name	Bit	7	6	5	4	3	2	1	0
RMAP = 1										
C0$_H$	**T21_T2CON** **Reset: 00**$_H$ Timer 2 Control Register	Bit Field	TF2	EXF2	0		EXEN2	TR2	C/$\overline{T2}$	CP/$\overline{RL2}$
		Type	rwh	rwh	r		rw	rwh	rw	rw
C1$_H$	**T21_T2MOD** **Reset: 00**$_H$ Timer 2 Mode Register	Bit Field	T2REGS	T2RHEN	EDGESEL	PREN	T2PRE			DCEN
		Type	rw	rw	rw	rw	rw	rw	rw	rw
C2$_H$	**T21_RC2L** **Reset: 00**$_H$ Timer 2 Reload/Capture Register Low	Bit Field	RC2							
		Type	rwh							
C3$_H$	**T21_RC2H** **Reset: 00**$_H$ Timer 2 Reload/Capture Register High	Bit Field	RC2							
		Type	rwh							
C4$_H$	**T21_T2L** **Reset: 00**$_H$ Timer 2 Register Low	Bit Field	THL2							
		Type	rwh							

3.3 Flash Memory

The Flash memory provides an embedded user-programmable non-volatile memory, allowing fast and reliable storage of user code and data. It is operated from a single 2.5 V supply from the Embedded Voltage Regulator (EVR) and does not require additional programming or erasing voltage. The sectorization of the Flash memory allows each sector to be erased independently.

Features

- In-System Programming (ISP) via UART
- In-Application Programming (IAP)
- Error Correction Code (ECC) for dynamic correction of single-bit errors
- Background program and erase operations for CPU load minimization
- Support for aborting erase operation
- Minimum program width[1] of 32-byte for D-Flash and 64-byte for P-Flash
- 1-sector minimum erase width
- 1-byte read access
- Flash is delivered in erased state (read all zeros)
- Operating supply voltage: 2.5 V ± 7.5 %
- Read access time: $3 \times t_{CCLK}$ = 125 ns[2]
- Program time: 248256 / f_{SYS} = 2.6 ms[3]
- Erase time: 9807360 / f_{SYS} = 102 ms[3]

---

1) P-Flash: 64-byte wordline can only be programmed once, i.e., one gate disturb allowed.
   D-Flash: 32-byte wordline can be programmed twice, i.e., two gate disturbs allowed.

2) Values shown here are typical values. f_{sys} = 96 MHz ± 7.5% (f_{CCLK} = 24 MHz ± 7.5 %) is the maximum frequency range for Flash read access.

3) Values shown here are typical values. f_{sys} = 96 MHz ± 7.5% is the only frequency range for Flash programming and erasing. f_{sysmin} is used for obtaining the worst case timing.

## 3.6   Power Supply System with Embedded Voltage Regulator

The XC886/888 microcontroller requires two different levels of power supply:

- 3.3 V or 5.0 V for the Embedded Voltage Regulator (EVR) and Ports
- 2.5 V for the core, memory, on-chip oscillator, and peripherals

Figure 21 shows the XC886/888 power supply system. A power supply of 3.3 V or 5.0 V must be provided from the external power supply pin. The 2.5 V power supply for the logic is generated by the EVR. The EVR helps to reduce the power consumption of the whole chip and the complexity of the application board design.

The EVR consists of a main voltage regulator and a low power voltage regulator. In active mode, both voltage regulators are enabled. In power-down mode, the main voltage regulator is switched off, while the low power voltage regulator continues to function and provide power supply to the system with low power consumption.
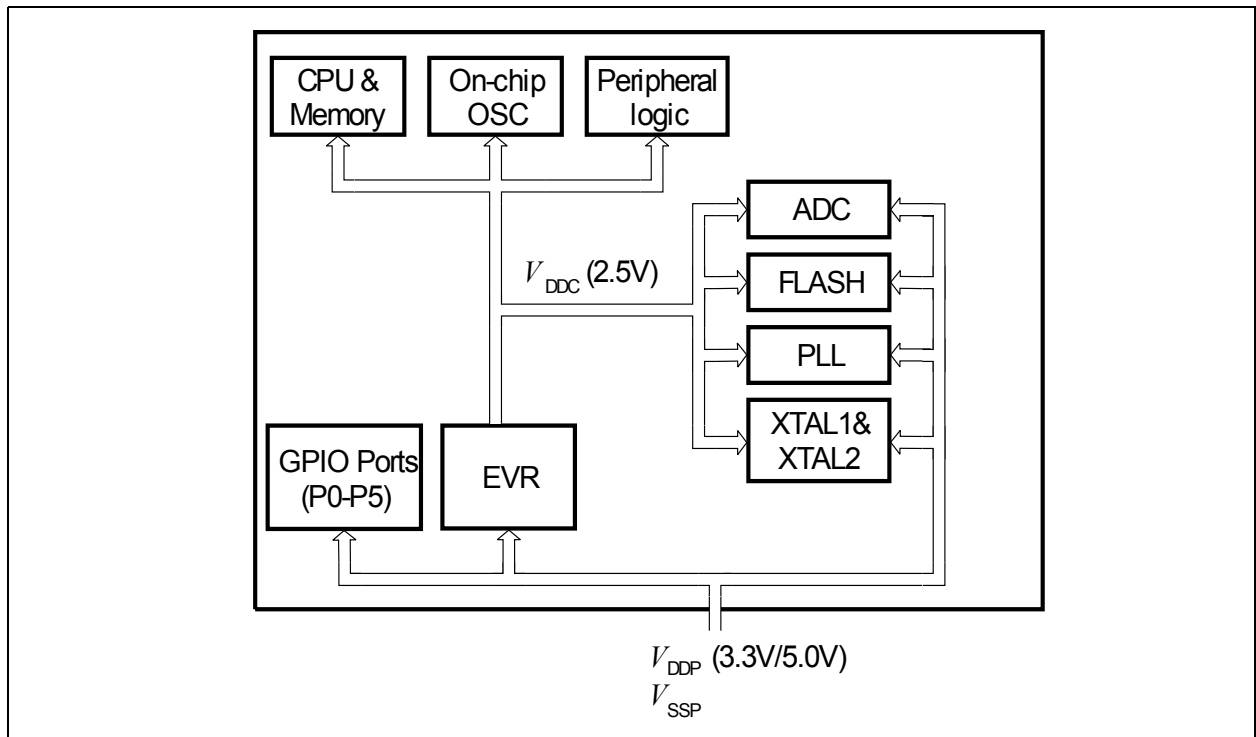
Figure 21   XC886/888 Power Supply System

EVR Features

- Input voltage (V_{DDP}): 3.3 V/5.0 V
- Output voltage (V_{DDC}): 2.5 V ± 7.5%
- Low power voltage regulator provided in power-down mode
- V_{DDC} and V_{DDP} prewarning detection
- V_{DDC} brownout detection

1) BSL mode is automatically entered if no valid password is installed and data at memory address 0000H equals zero.

2) OSC is bypassed in MultiCAN BSL mode

3) Normal user mode with standard JTAG (TCK,TDI,TDO) pins for hot-attach purpose.

Note: The boot options are valid only with the default set of UART and JTAG pins.

3.8 Clock Generation Unit

The Clock Generation Unit (CGU) allows great flexibility in the clock generation for the XC886/888. The power consumption is indirectly proportional to the frequency, whereas the performance of the microcontroller is directly proportional to the frequency. During user program execution, the frequency can be programmed for an optimal ratio between performance and power consumption. Therefore the power consumption can be adapted to the actual application state.

Features

• Phase-Locked Loop (PLL) for multiplying clock source by different factors
• PLL Base Mode
• Prescaler Mode
• PLL Mode
• Power-down mode support

The CGU consists of an oscillator circuit and a PLL. In the XC886/888, the oscillator can be from either of these two sources: the on-chip oscillator (9.6 MHz) or the external oscillator (4 MHz to 12 MHz). The term "oscillator" is used to refer to both on-chip oscillator and external oscillator, unless otherwise stated. After the reset, the on-chip oscillator will be used by default.The external oscillator can be selected via software. In addition, the PLL provides a fail-safe logic to perform oscillator run and loss-of-lock detection. This allows emergency routines to be executed for system recovery or to perform system shut down.

3.8.2 Clock Management

The CGU generates all clock signals required within the microcontroller from a single clock, f_{sys}. During normal system operation, the typical frequencies of the different modules are as follow:

- CPU clock: CCLK, SCLK = 24 MHz
- Fast clock (used by MultiCAN): FCLK = 24 or 48 MHz
- Peripheral clock: PCLK = 24 MHz
- Flash Interface clock: CCLK2 = 48 MHz and CCLK = 24 MHz

In addition, different clock frequencies can be output to pin CLKOUT (P0.0 or P0.7). The clock output frequency, which is derived from the clock output divider (bit COREL), can further be divided by 2 using toggle latch (bit TLEN is set to 1). The resulting output frequency has a 50% duty cycle. **Figure 26** shows the clock distribution of the XC886/888.
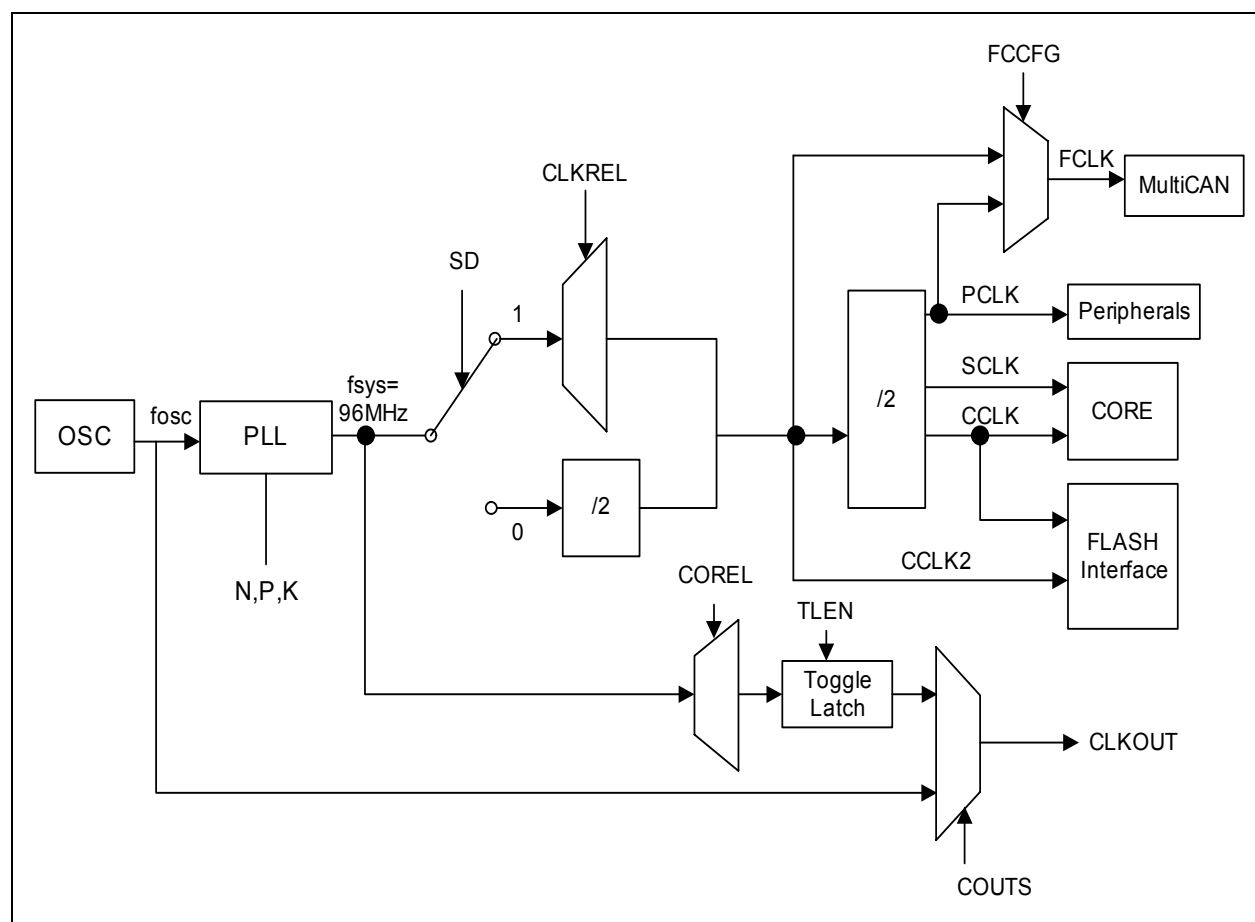
Figure 26   Clock Generation from f_{sys}

3.10   Watchdog Timer

The Watchdog Timer (WDT) provides a highly reliable and secure way to detect and recover from software or hardware failures. The WDT is reset at a regular interval that is predefined by the user. The CPU must service the WDT within this interval to prevent the WDT from causing an XC886/888 system reset. Hence, routine service of the WDT confirms that the system is functioning properly. This ensures that an accidental malfunction of the XC886/888 will be aborted in a user-specified time period.

In debug mode, the WDT is default suspended and stops counting. Therefore, there is no need to refresh the WDT during debugging.

Features

*   16-bit Watchdog Timer
*   Programmable reload value for upper 8 bits of timer
*   Programmable window boundary
*   Selectable input frequency of $f_{PCLK}/2$ or $f_{PCLK}/128$
*   Time-out detection with NMI generation and reset prewarning activation (after which a system reset will be performed)

The WDT is a 16-bit timer incremented by a count rate of $f_{PCLK}/2$ or $f_{PCLK}/128$. This 16-bit timer is realized as two concatenated 8-bit timers. The upper 8 bits of the WDT can be preset to a user-programmable value via a watchdog service access in order to modify the watchdog expire time period. The lower 8 bits are reset on each service access. **Figure 28** shows the block diagram of the WDT unit.
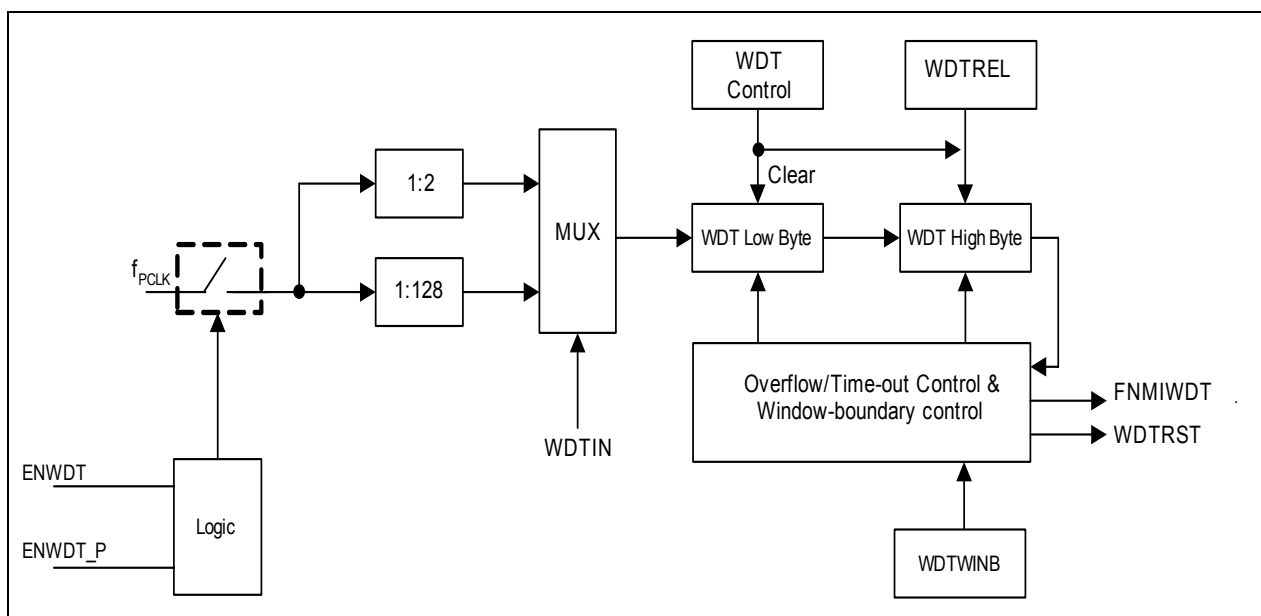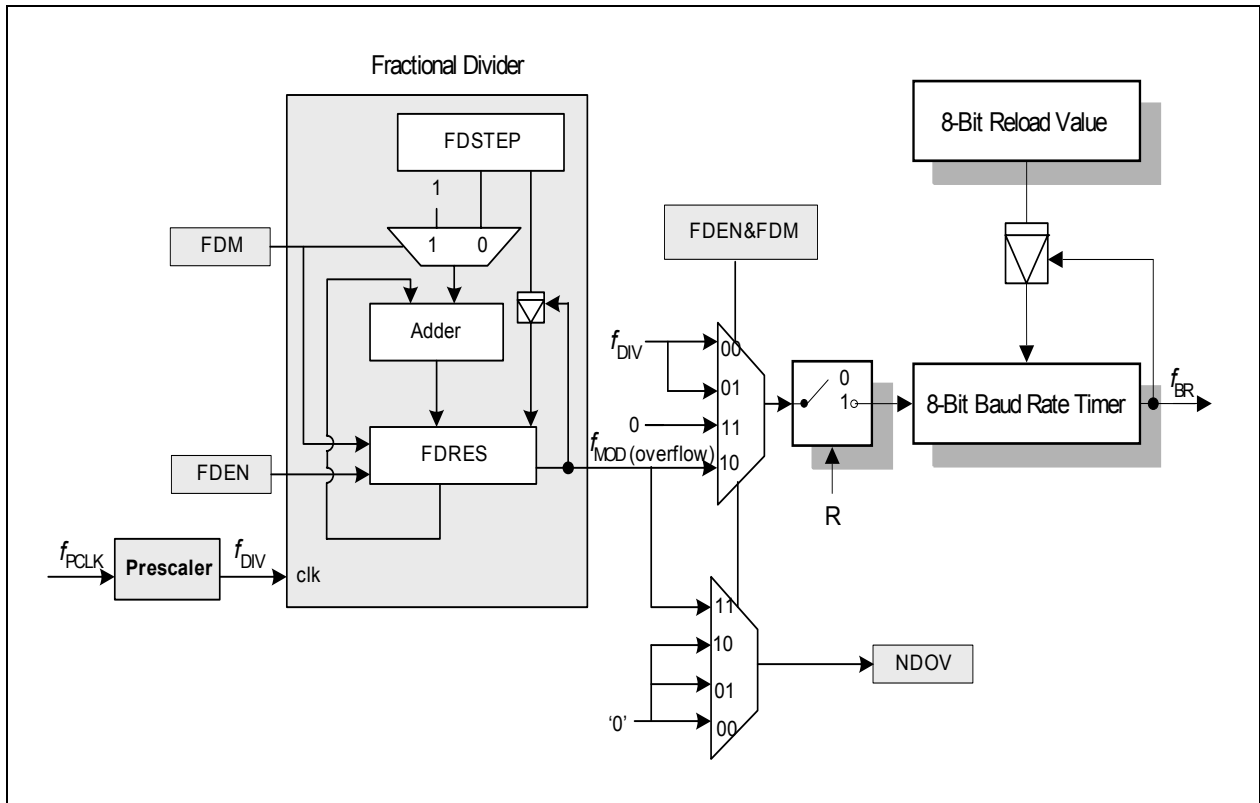

Figure 28   WDT Block Diagram

fractional divider) for generating a wide range of baud rates based on its input clock f_{PCLK}, see **Figure 30**.


Figure 30   Baud-rate Generator Circuitry

The baud rate timer is a count-down timer and is clocked by either the output of the fractional divider (f_{MOD}) if the fractional divider is enabled (FDCON.FDEN = 1), or the output of the prescaler (f_{DIV}) if the fractional divider is disabled (FDEN = 0). For baud rate generation, the fractional divider must be configured to fractional divider mode (FDCON.FDM = 0). This allows the baud rate control run bit BCON.R to be used to start or stop the baud rate timer. At each timer underflow, the timer is reloaded with the 8-bit reload value in register BG and one clock pulse is generated for the serial channel.

Enabling the fractional divider in normal divider mode (FDEN = 1 and FDM = 1) stops the baud rate timer and nullifies the effect of bit BCON.R. See **Section 3.14**.

The baud rate (f_{BR}) value is dependent on the following parameters:

- Input clock f_{PCLK}
- Prescaling factor (2^{BRPRE}) defined by bit field BRPRE in register BCON
- Fractional divider (STEP/256) defined by register FDSTEP
  (to be considered only if fractional divider is enabled and operating in fractional divider mode)
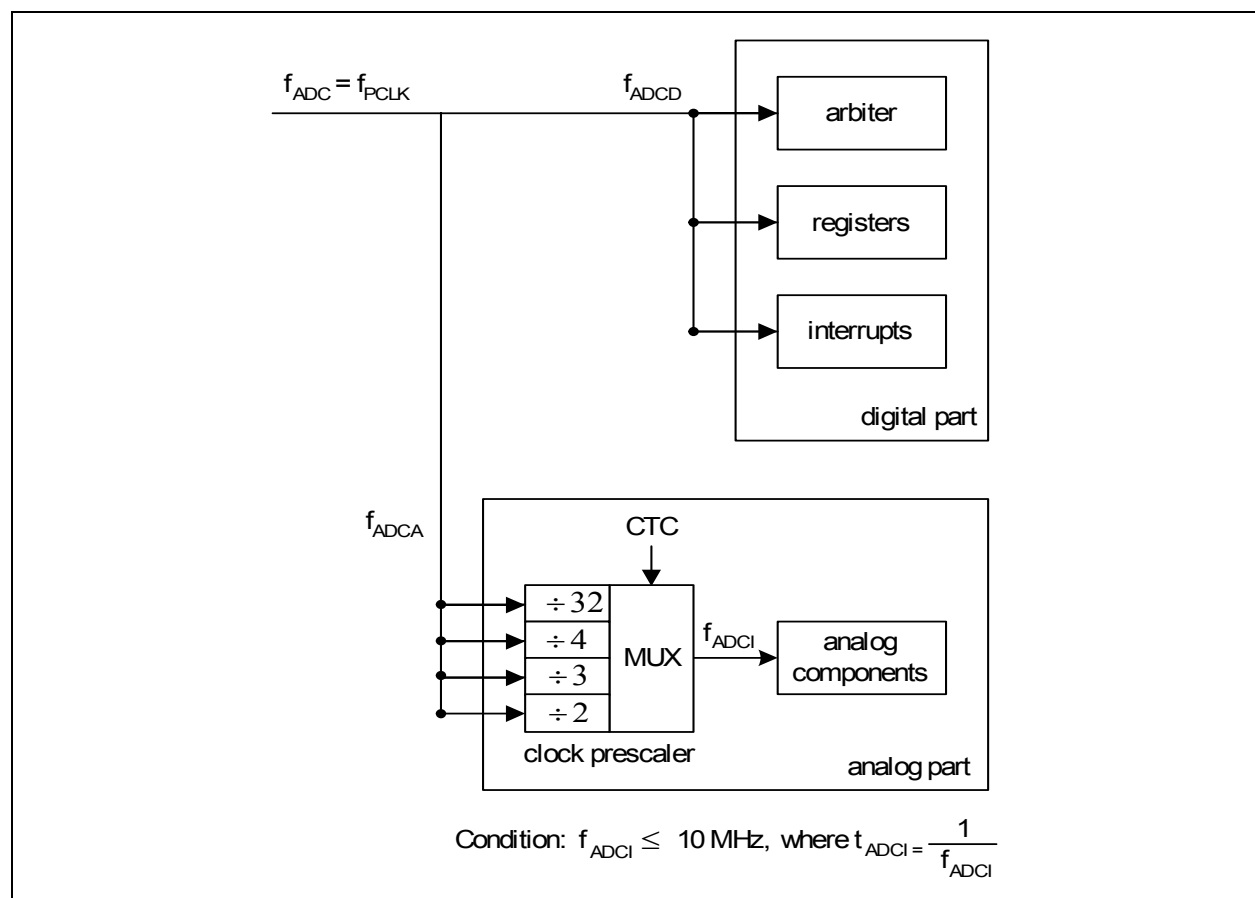- 8-bit reload value (BR_VALUE) for the baud rate timer defined by register BG
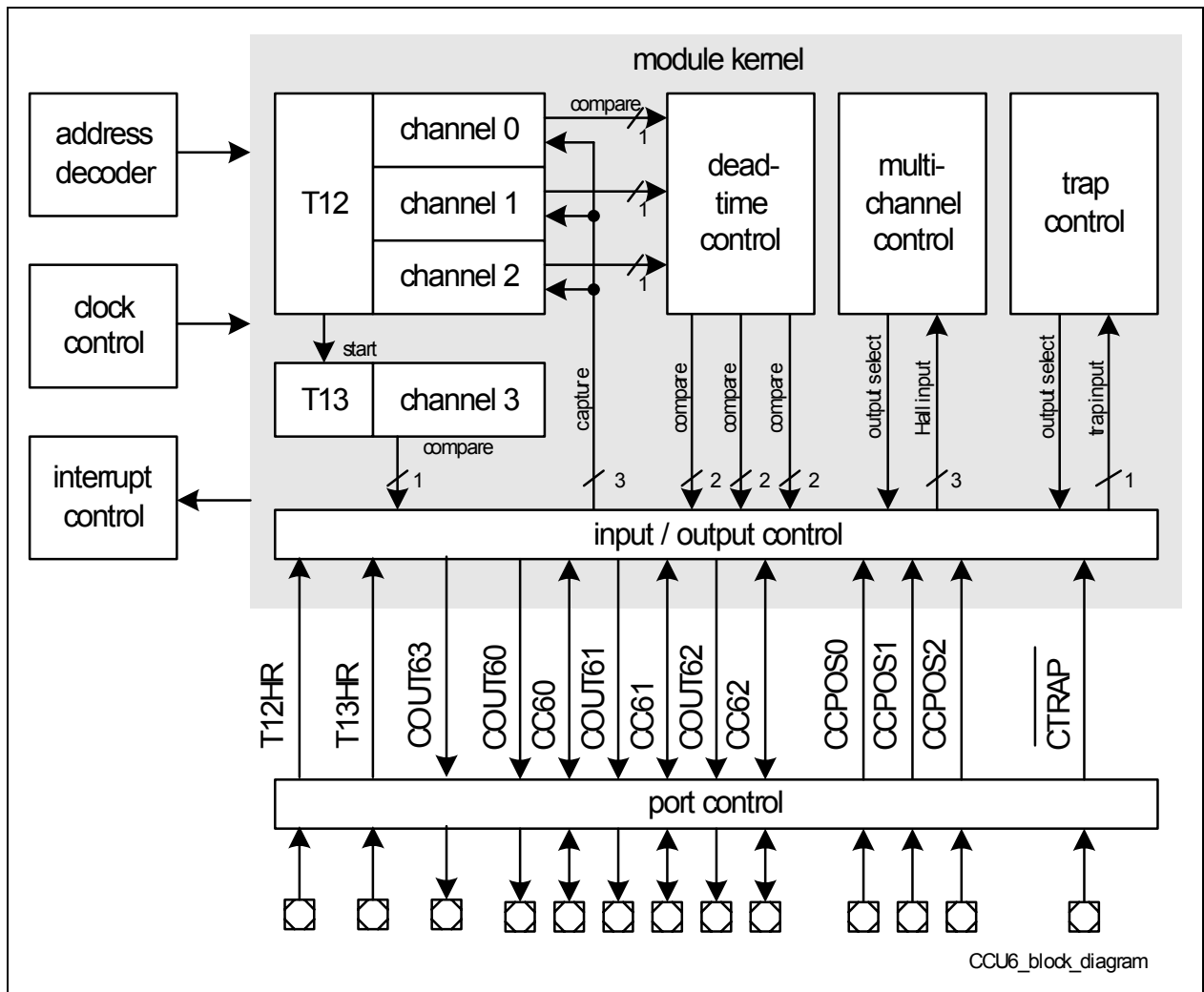
Figure 33   CCU6 Block Diagram

GLOBCTR. A prescaling ratio of 32 can be selected when the maximum performance of the ADC is not required.

Figure 35   ADC Clocking Scheme

For module clock f_{ADC} = 24 MHz, the analog clock f_{ADCI} frequency can be selected as shown in **Table 34**.

Table 34 f_{ADCI} Frequency Selection

Module Clock f_{ADC}	CTC	Prescaling Ratio	Analog Clock f_{ADCI}
24 MHz	00_B	$\div 2$	12 MHz (N.A)
	01_B	$\div 3$	8 MHz
	10_B	$\div 4$	6 MHz
	11_B (default)	$\div 32$	750 kHz

As f_{ADCI} cannot exceed 10 MHz, bit field CTC should not be set to 00_B when f_{ADC} is 24 MHz. During slow-down mode where f_{ADC} may be reduced to 12 MHz, 6 MHz etc., CTC can be set to 00_B as long as the divided analog clock f_{ADCI} does not exceed 10 MHz.

Table 40   ADC Characteristics (Operating Conditions apply; V_{DDP} = 5V Range)

Parameter	Symbol		Limit Values			Unit	Test Conditions/ Remarks
			min.	typ .	max.		
Overload current coupling factor for digital I/O pins	K_{OVD}	CC	–	–	5.0×10^{-3}	–	$I_{OV} > 0$ [1)3)]
			–	–	1.0×10^{-2}	–	$I_{OV} < 0$ [1)3)]
Switched capacitance at the reference voltage input	C_{AREFSW}	CC	–	10	20	pF	[1)4)]
Switched capacitance at the analog voltage inputs	C_{AINSW}	CC	–	5	7	pF	[1)5)]
Input resistance of the reference input	R_{AREF}	CC	–	1	2	kΩ	[1)]
Input resistance of the selected analog channel	R_{AIN}	CC	–	1	1.5	kΩ	[1)]

1) Not subjected to production test, verified by design/characterization

2) TUE is tested at V_{AREF} = 5.0 V, V_{AGND} = 0 V, V_{DDP} = 5.0 V.

3) An overload current (I_{OV}) through a pin injects a certain error current (I_{INJ}) into the adjacent pins. This error current adds to the respective pin's leakage current (I_{OZ}). The amount of error current depends on the overload current and is defined by the overload coupling factor K_{OV}. The polarity of the injected error current is inverse compared to the polarity of the overload current that produces it. The total current through a pin is $|I_{TOT}| = |I_{OZ1}|$ + ($|I_{OV}| \times K_{OV}$). The additional error current may distort the input voltage on analog inputs.

4) This represents an equivalent switched capacitance. This capacitance is not switched to the reference voltage at once. Instead of this, smaller capacitances are successively switched to the reference voltage.

5) The sampling capacity of the conversion C-Network is pre-charged to V_{AREF}/2 before connecting the input to the C-Network. Because of the parasitic elements, the voltage measured at ANx is lower than V_{AREF}/2.
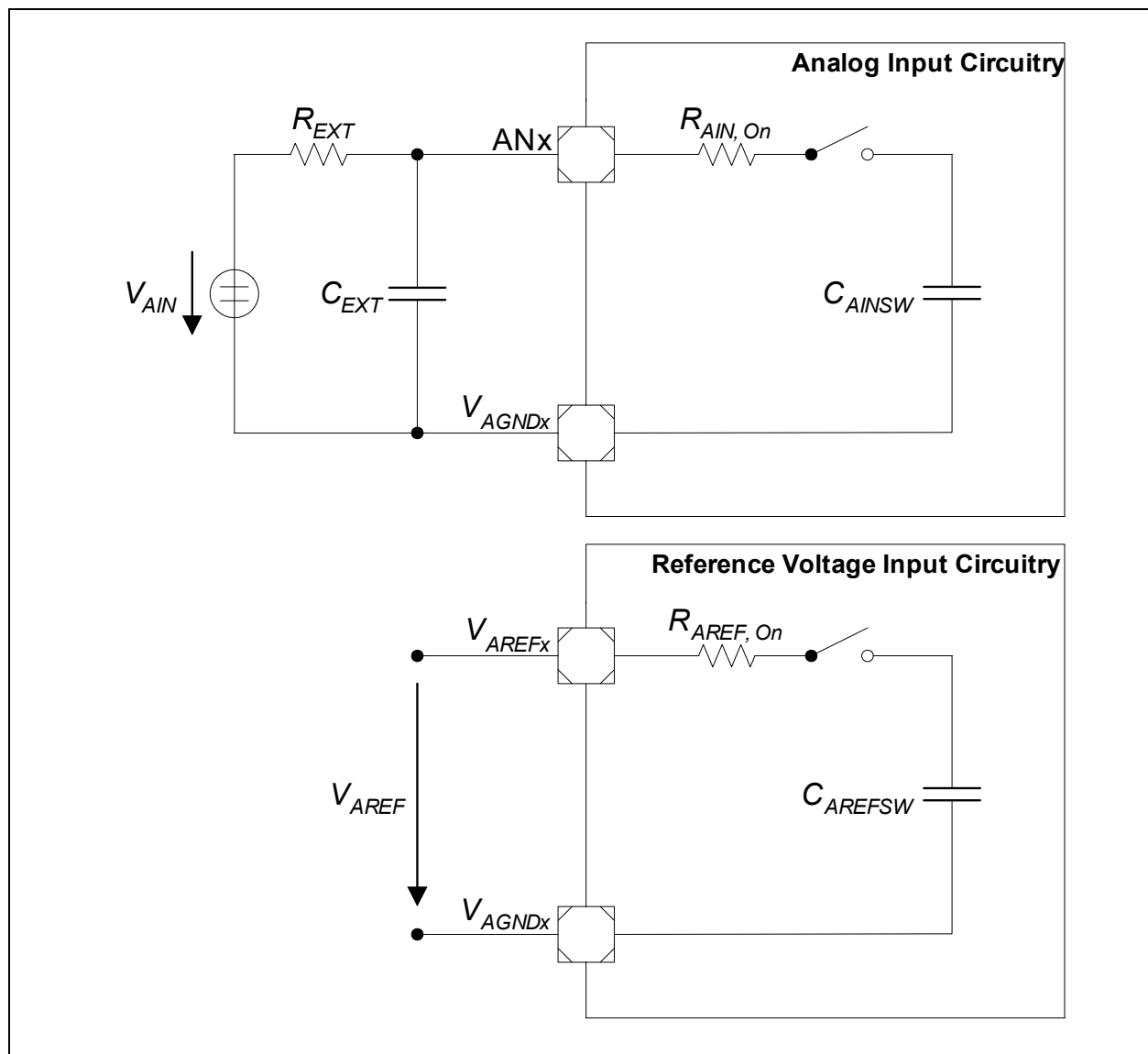
Figure 39   ADC Input Circuits

4.3.4 On-Chip Oscillator Characteristics

Table 47 provides the characteristics of the on-chip oscillator in the XC886/888.

Table 47   On-chip Oscillator Characteristics (Operating Conditions apply)

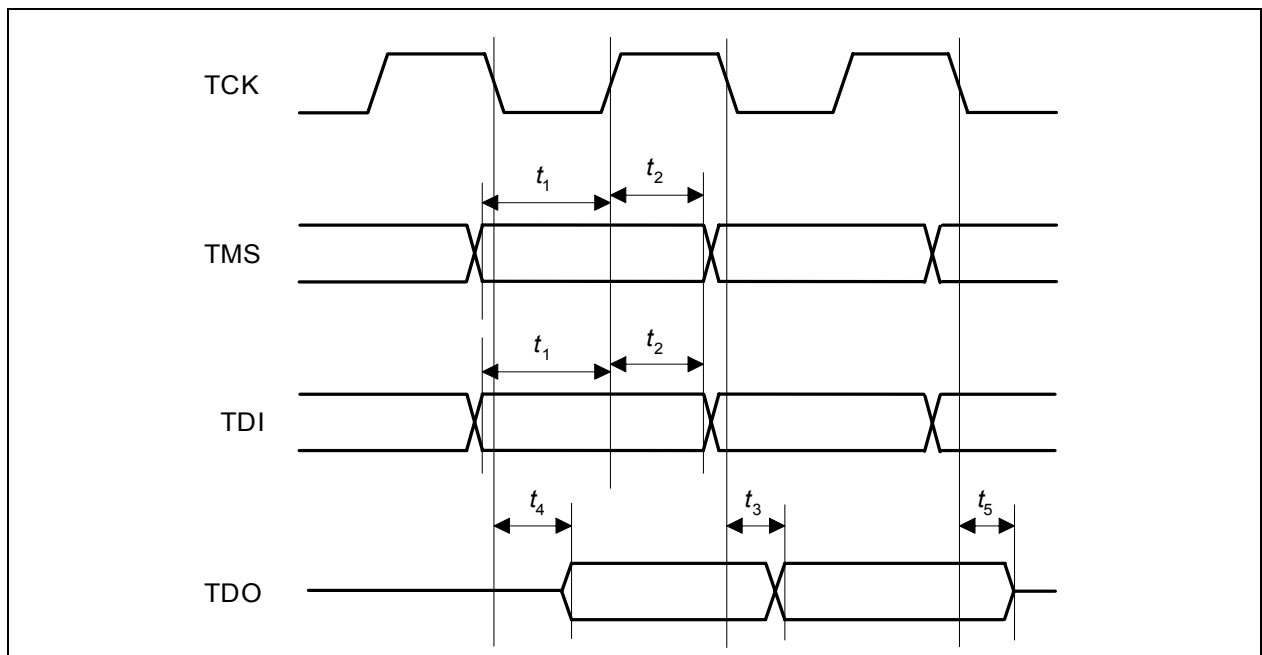| Parameter	Symbol	Limit Values			Unit	Test Conditions
		min.	typ.	max.		
Nominal frequency	f_{NOM} CC	9.36	9.6	9.84	MHz	under nominal conditions[1]
Long term frequency deviation	Δf_{LT} CC	-5.0	–	5.0	%	with respect to f_{NOM}, over lifetime and temperature (-10°C to 125°C), for one given device after trimming
		-6.0	–	0	%	with respect to f_{NOM}, over lifetime and temperature (-40°C to -10°C), for one given device after trimming
Short term frequency deviation	Δf_{ST} CC	-1.0	–	1.0	%	within one LIN message (<10 ms .... 100 ms)

1) Nominal condition: V_{DDC} = 2.5 V, T_A = + 25°C.

Table 50   JTAG Timing (Operating Conditions apply; CL = 50 pF) (cont'd)

Parameter	Symbol		Limits		Unit	Test Conditions
			min	max		
TDO high impedance to valid output from TCK	t_4	CC	-	27	ns	5V Device[1]
			-	36	ns	3.3V Device[1]
TDO valid output to high impedance from TCK	t_5	CC	-	22	ns	5V Device[1]
			-	28	ns	3.3V Device[1]

1) Not all parameters are 100% tested, but are verified by design/characterization and test correlation.

Figure 47   JTAG Timing

Figure 49 shows the package outlines of the XC888.

Figure 49   PG-TQFP-64 Package Outline