Infineon Technologies - XC888CLM8FFI5VACFXUMA1 Datasheet

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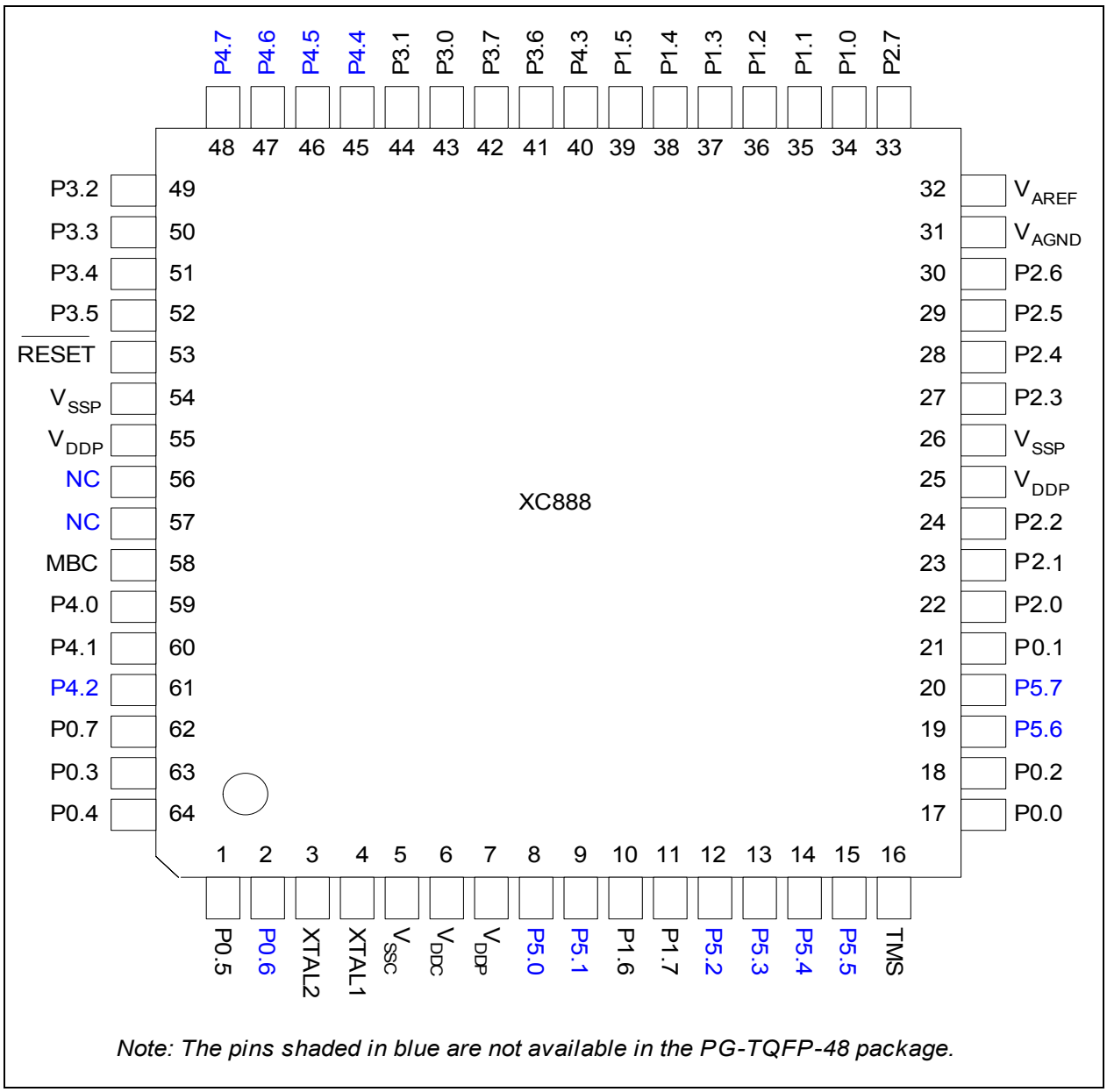
Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	XC800
Core Size	8-Bit
Speed	24MHz
Connectivity	CANbus, LINbus, SSI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	48
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	1.75K x 8
Voltage - Supply (Vcc/Vdd)	4.5V ~ 5.5V
Data Converters	A/D 8x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	PG-TQFP-64
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/xc888clm8ffi5vacfxuma1



Note: The pins shaded in blue are not available in the PG-TQFP-48 package.

Figure 5 XC888 Pin Configuration, PG-TQFP-64 Package (top view)

Table 3 Pin Definitions and Functions (cont'd)

Symbol	Pin Number (TQFP-48/64)	Type	Reset State	Function
P3		I/O		**Port 3** Port 3 is an 8-bit bidirectional general purpose I/O port. It can be used as alternate functions for CCU6, UART1, Timer 21 and MultiCAN.
P3.0	35/43		Hi-Z	CCPOS1_2 CCU6 Hall Input 1 CC60_0 Input/Output of Capture/Compare channel 0 RXDO1_1 UART1 Transmit Data Output
P3.1	36/44		Hi-Z	CCPOS0_2 CCU6 Hall Input 0 CC61_2 Input/Output of Capture/Compare channel 1 COUT60_0 Output of Capture/Compare channel 0 TXD1_1 UART1 Transmit Data Output/Clock Output
P3.2	37/49		Hi-Z	CCPOS2_2 CCU6 Hall Input 2 RXDC1_1 MultiCAN Node 1 Receiver Input RXD1_1 UART1 Receive Data Input CC61_0 Input/Output of Capture/Compare channel 1
P3.3	38/50		Hi-Z	COUT61_0 Output of Capture/Compare channel 1 TXDC1_1 MultiCAN Node 1 Transmitter Output
P3.4	39/51		Hi-Z	CC62_0 Input/Output of Capture/Compare channel 2 RXDC0_1 MultiCAN Node 0 Receiver Input T2EX1_0 Timer 21 External Trigger Input
P3.5	40/52		Hi-Z	COUT62_0 Output of Capture/Compare channel 2 EXF21_0 Timer 21 External Flag Output TXDC0_1 MultiCAN Node 0 Transmitter Output
P3.6	33/41		PD	$\overline{\text{CTRAP\_0}}$ CCU6 Trap Input

Table 3 Pin Definitions and Functions (cont'd)

Symbol	Pin Number (TQFP-48/64)	Type	Reset State	Function	
P5		I/O		**Port 5** Port 5 is an 8-bit bidirectional general purpose I/O port. It can be used as alternate functions for UART, UART1 and JTAG.	
P5.0	–/8		PU	EXINT1_1	External Interrupt Input 1
P5.1	–/9		PU	EXINT2_1	External Interrupt Input 2
P5.2	–/12		PU	RXD_2	UART Receive Data Input
P5.3	–/13		PU	TXD_2	UART Transmit Data Output/Clock Output
P5.4	–/14		PU	RXDO_2	UART Transmit Data Output
P5.5	–/15		PU	TDO_2 TXD1_2	JTAG Serial Data Output UART1 Transmit Data Output/ Clock Output
P5.6	–/19		PU	TCK_2 RXDO1_2	JTAG Clock Input UART1 Transmit Data Output
P5.7	–/20		PU	TDI_2 RXD1_2	JTAG Serial Data Input UART1 Receive Data Input

Table 5 CPU Register Overview (cont'd)

Addr	Register Name	Bit	7	6	5	4	3	2	1	0
$A8_H$	**IEN0** **Reset: 00_H** Interrupt Enable Register 0	Bit Field	EA	0	ET2	ES	ET1	EX1	ET0	EX0
		Type	rw	r	rw	rw	rw	rw	rw	rw
$B8_H$	**IP** **Reset: 00_H** Interrupt Priority Register	Bit Field	0		PT2	PS	PT1	PX1	PT0	PX0
		Type	r		rw	rw	rw	rw	rw	rw
$B9_H$	**IPH** **Reset: 00_H** Interrupt Priority High Register	Bit Field	0		PT2H	PSH	PT1H	PX1H	PT0H	PX0H
		Type	r		rw	rw	rw	rw	rw	rw
$D0_H$	**PSW** **Reset: 00_H** Program Status Word Register	Bit Field	CY	AC	F0	RS1	RS0	OV	F1	P
		Type	rwh	rwh	rw	rw	rw	rwh	rw	rh
$E0_H$	**ACC** **Reset: 00_H** Accumulator Register	Bit Field	ACC7	ACC6	ACC5	ACC4	ACC3	ACC2	ACC1	ACC0
		Type	rw	rw	rw	rw	rw	rw	rw	rw
$E8_H$	**IEN1** **Reset: 00_H** Interrupt Enable Register 1	Bit Field	ECCIP 3	ECCIP 2	ECCIP 1	ECCIP 0	EXM	EX2	ESSC	EADC
		Type	rw	rw	rw	rw	rw	rw	rw	rw
$F0_H$	**B** **Reset: 00_H** B Register	Bit Field	B7	B6	B5	B4	B3	B2	B1	B0
		Type	rw	rw	rw	rw	rw	rw	rw	rw
$F8_H$	**IP1** **Reset: 00_H** Interrupt Priority 1 Register	Bit Field	PCCIP 3	PCCIP 2	PCCIP 1	PCCIP 0	PXM	PX2	PSSC	PADC
		Type	rw	rw	rw	rw	rw	rw	rw	rw
$F9_H$	**IPH1** **Reset: 00_H** Interrupt Priority 1 High Register	Bit Field	PCCIP 3H	PCCIP 2H	PCCIP 1H	PCCIP 0H	PXMH	PX2H	PSSC H	PADC H
		Type	rw	rw	rw	rw	rw	rw	rw	rw

3.2.4.2 MDU Registers

The MDU SFRs can be accessed in the mapped memory area (RMAP = 1).

Table 6 MDU Register Overview

Addr	Register Name	Bit	7	6	5	4	3	2	1	0
RMAP = 1										
$B0_H$	**MDUSTAT** **Reset: 00_H** MDU Status Register	Bit Field	0					BSY	IERR	IRDY
		Type	r					rh	rwh	rwh
$B1_H$	**MDUCON** **Reset: 00_H** MDU Control Register	Bit Field	IE	IR	RSEL	STAR T	OPCODE			
		Type	rw	rw	rw	rwh	rw			
$B2_H$	**MD0** **Reset: 00_H** MDU Operand Register 0	Bit Field	DATA							
		Type	rw							
$B2_H$	**MR0** **Reset: 00_H** MDU Result Register 0	Bit Field	DATA							
		Type	rh							
$B3_H$	**MD1** **Reset: 00_H** MDU Operand Register 1	Bit Field	DATA							
		Type	rw							

Table 10 Port Register Overview (cont'd)

Addr	Register Name	Bit	7	6	5	4	3	2	1	0
RMAP = 0, PAGE 1										
80_H	**P0_PUDSEL Reset: FF_H** P0 Pull-Up/Pull-Down Select Register	Bit Field	P7	P6	P5	P4	P3	P2	P1	P0
		Type	rw	rw	rw	rw	rw	rw	rw	rw
86_H	**P0_PUDEN Reset: $C4_H$** P0 Pull-Up/Pull-Down Enable Register	Bit Field	P7	P6	P5	P4	P3	P2	P1	P0
		Type	rw	rw	rw	rw	rw	rw	rw	rw
90_H	**P1_PUDSEL Reset: FF_H** P1 Pull-Up/Pull-Down Select Register	Bit Field	P7	P6	P5	P4	P3	P2	P1	P0
		Type	rw	rw	rw	rw	rw	rw	rw	rw
91_H	**P1_PUDEN Reset: FF_H** P1 Pull-Up/Pull-Down Enable Register	Bit Field	P7	P6	P5	P4	P3	P2	P1	P0
		Type	rw	rw	rw	rw	rw	rw	rw	rw
92_H	**P5_PUDSEL Reset: FF_H** P5 Pull-Up/Pull-Down Select Register	Bit Field	P7	P6	P5	P4	P3	P2	P1	P0
		Type	rw	rw	rw	rw	rw	rw	rw	rw
93_H	**P5_PUDEN Reset: FF_H** P5 Pull-Up/Pull-Down Enable Register	Bit Field	P7	P6	P5	P4	P3	P2	P1	P0
		Type	rw	rw	rw	rw	rw	rw	rw	rw
$A0_H$	**P2_PUDSEL Reset: FF_H** P2 Pull-Up/Pull-Down Select Register	Bit Field	P7	P6	P5	P4	P3	P2	P1	P0
		Type	rw	rw	rw	rw	rw	rw	rw	rw
$A1_H$	**P2_PUDEN Reset: 00_H** P2 Pull-Up/Pull-Down Enable Register	Bit Field	P7	P6	P5	P4	P3	P2	P1	P0
		Type	rw	rw	rw	rw	rw	rw	rw	rw
$B0_H$	**P3_PUDSEL Reset: BF_H** P3 Pull-Up/Pull-Down Select Register	Bit Field	P7	P6	P5	P4	P3	P2	P1	P0
		Type	rw	rw	rw	rw	rw	rw	rw	rw
$B1_H$	**P3_PUDEN Reset: 40_H** P3 Pull-Up/Pull-Down Enable Register	Bit Field	P7	P6	P5	P4	P3	P2	P1	P0
		Type	rw	rw	rw	rw	rw	rw	rw	rw
$C8_H$	**P4_PUDSEL Reset: FF_H** P4 Pull-Up/Pull-Down Select Register	Bit Field	P7	P6	P5	P4	P3	P2	P1	P0
		Type	rw	rw	rw	rw	rw	rw	rw	rw
$C9_H$	**P4_PUDEN Reset: 04_H** P4 Pull-Up/Pull-Down Enable Register	Bit Field	P7	P6	P5	P4	P3	P2	P1	P0
		Type	rw	rw	rw	rw	rw	rw	rw	rw
RMAP = 0, PAGE 2										
80_H	**P0_ALTSEL0 Reset: 00_H** P0 Alternate Select 0 Register	Bit Field	P7	P6	P5	P4	P3	P2	P1	P0
		Type	rw	rw	rw	rw	rw	rw	rw	rw
86_H	**P0_ALTSEL1 Reset: 00_H** P0 Alternate Select 1 Register	Bit Field	P7	P6	P5	P4	P3	P2	P1	P0
		Type	rw	rw	rw	rw	rw	rw	rw	rw
90_H	**P1_ALTSEL0 Reset: 00_H** P1 Alternate Select 0 Register	Bit Field	P7	P6	P5	P4	P3	P2	P1	P0
		Type	rw	rw	rw	rw	rw	rw	rw	rw
91_H	**P1_ALTSEL1 Reset: 00_H** P1 Alternate Select 1 Register	Bit Field	P7	P6	P5	P4	P3	P2	P1	P0
		Type	rw	rw	rw	rw	rw	rw	rw	rw
92_H	**P5_ALTSEL0 Reset: 00_H** P5 Alternate Select 0 Register	Bit Field	P7	P6	P5	P4	P3	P2	P1	P0
		Type	rw	rw	rw	rw	rw	rw	rw	rw

Table 11 ADC Register Overview (cont'd)

Addr	Register Name	Bit	7	6	5	4	3	2	1	0
$D3_H$	**ADC_RESR3H Reset: 00_H** Result Register 3 High	Bit Field	RESULT							
		Type	rh							
RMAP = 0, PAGE 3										
CA_H	**ADC_RESRA0L Reset: 00_H** Result Register 0, View A Low	Bit Field	RESULT			VF	DRC	CHNR		
		Type	rh			rh	rh	rh		
CB_H	**ADC_RESRA0H Reset: 00_H** Result Register 0, View A High	Bit Field	RESULT							
		Type	rh							
CC_H	**ADC_RESRA1L Reset: 00_H** Result Register 1, View A Low	Bit Field	RESULT			VF	DRC	CHNR		
		Type	rh			rh	rh	rh		
CD_H	**ADC_RESRA1H Reset: 00_H** Result Register 1, View A High	Bit Field	RESULT							
		Type	rh							
CE_H	**ADC_RESRA2L Reset: 00_H** Result Register 2, View A Low	Bit Field	RESULT			VF	DRC	CHNR		
		Type	rh			rh	rh	rh		
CF_H	**ADC_RESRA2H Reset: 00_H** Result Register 2, View A High	Bit Field	RESULT							
		Type	rh							
$D2_H$	**ADC_RESRA3L Reset: 00_H** Result Register 3, View A Low	Bit Field	RESULT			VF	DRC	CHNR		
		Type	rh			rh	rh	rh		
$D3_H$	**ADC_RESRA3H Reset: 00_H** Result Register 3, View A High	Bit Field	RESULT							
		Type	rh							
RMAP = 0, PAGE 4										
CA_H	**ADC_RCR0 Reset: 00_H** Result Control Register 0	Bit Field	VFCTR	WFR	0	IEN	0			DRCTR
		Type	rw	rw	r	rw	r			rw
CB_H	**ADC_RCR1 Reset: 00_H** Result Control Register 1	Bit Field	VFCTR	WFR	0	IEN	0			DRCTR
		Type	rw	rw	r	rw	r			rw
CC_H	**ADC_RCR2 Reset: 00_H** Result Control Register 2	Bit Field	VFCTR	WFR	0	IEN	0			DRCTR
		Type	rw	rw	r	rw	r			rw
CD_H	**ADC_RCR3 Reset: 00_H** Result Control Register 3	Bit Field	VFCTR	WFR	0	IEN	0			DRCTR
		Type	rw	rw	r	rw	r			rw
CE_H	**ADC_VFCR Reset: 00_H** Valid Flag Clear Register	Bit Field	0				VFC3	VFC2	VFC1	VFC0
		Type	r				w	w	w	w
RMAP = 0, PAGE 5										
CA_H	**ADC_CHINFR Reset: 00_H** Channel Interrupt Flag Register	Bit Field	CHINF7	CHINF6	CHINF5	CHINF4	CHINF3	CHINF2	CHINF1	CHINF0
		Type	rh	rh	rh	rh	rh	rh	rh	rh
CB_H	**ADC_CHINCR Reset: 00_H** Channel Interrupt Clear Register	Bit Field	CHINC7	CHINC6	CHINC5	CHINC4	CHINC3	CHINC2	CHINC1	CHINC0
		Type	w	w	w	w	w	w	w	w

3.2.4.12 SSC Registers

The SSC SFRs can be accessed in the standard memory area (RMAP = 0).

Table 16 SSC Register Overview

Addr	Register Name	Bit	7	6	5	4	3	2	1	0
RMAP = 0										
$A9_H$	**SSC_PISEL** **Reset: 00_H** Port Input Select Register	Bit Field	0					CIS	SIS	MIS
		Type	r					rw	rw	rw
AA_H	**SSC_CONL** **Reset: 00_H** Control Register Low Programming Mode	Bit Field	LB	PO	PH	HB	BM			
		Type	rw	rw	rw	rw	rw			
AA_H	**SSC_CONL** **Reset: 00_H** Control Register Low Operating Mode	Bit Field	0				BC			
		Type	r				rh			
AB_H	**SSC_CONH** **Reset: 00_H** Control Register High Programming Mode	Bit Field	EN	MS	0	AREN	BEN	PEN	REN	TEN
		Type	rw	rw	r	rw	rw	rw	rw	rw
AB_H	**SSC_CONH** **Reset: 00_H** Control Register High Operating Mode	Bit Field	EN	MS	0	BSY	BE	PE	RE	TE
		Type	rw	rw	r	rh	rwh	rwh	rwh	rwh
AC_H	**SSC_TBL** **Reset: 00_H** Transmitter Buffer Register Low	Bit Field	TB_VALUE							
		Type	rw							
AD_H	**SSC_RBL** **Reset: 00_H** Receiver Buffer Register Low	Bit Field	RB_VALUE							
		Type	rh							
AE_H	**SSC_BRL** **Reset: 00_H** Baud Rate Timer Reload Register Low	Bit Field	BR_VALUE							
		Type	rw							
AF_H	**SSC_BRH** **Reset: 00_H** Baud Rate Timer Reload Register High	Bit Field	BR_VALUE							
		Type	rw							

3.2.4.13 MultiCAN Registers

The MultiCAN SFRs can be accessed in the standard memory area (RMAP = 0).

Table 17 CAN Register Overview

Addr	Register Name	Bit	7	6	5	4	3	2	1	0
RMAP = 0										
$D8_H$	**ADCON** **Reset: 00_H** CAN Address/Data Control Register	Bit Field	V3	V2	V1	V0	AUAD		BSY	RWEN
		Type	rw	rw	rw	rw	rw		rh	rw
$D9_H$	**ADL** **Reset: 00_H** CAN Address Register Low	Bit Field	CA9	CA8	CA7	CA6	CA5	CA4	CA3	CA2
		Type	rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh
DA_H	**ADH** **Reset: 00_H** CAN Address Register High	Bit Field	0				CA13	CA12	CA11	CA10
		Type	r				rwh	rwh	rwh	rwh

Table 19 shows the Flash data retention and endurance targets.

Table 19 Flash Data Retention and Endurance (Operating Conditions apply)

Retention	Endurance[1)]	Size	Remarks
Program Flash			
20 years	1,000 cycles	up to 32 Kbytes[2)]	for 32-Kbyte Variant
20 years	1,000 cycles	up to 24 Kbytes[2)]	for 24-Kbyte Variant
Data Flash			
20 years	1,000 cycles	4 Kbytes	
5 years	10,000 cycles	1 Kbyte	
2 years	70,000 cycles	512 bytes	
2 years	100,000 cycles	128 bytes	

1) One cycle refers to the programming of all wordlines in a sector and erasing of sector. The Flash endurance data specified in Table 19 is valid only if the following conditions are fulfilled:
- the maximum number of erase cycles per Flash sector must not exceed 100,000 cycles.
- the maximum number of erase cycles per Flash bank must not exceed 300,000 cycles.
- the maximum number of program cycles per Flash bank must not exceed 2,500,000 cycles.

2) If no Flash is used for data, the Program Flash size can be up to the maximum Flash size available in the device variant. Having more Data Flash will mean less Flash is available for Program Flash.

3.3.1 Flash Bank Sectorization

The XC886/888 product family offers Flash devices with either 24 Kbytes or 32 Kbytes of embedded Flash memory. Each Flash device consists of Program Flash (P-Flash) and Data Flash (D-Flash) bank(s) with different sectorization shown in Figure 11. Both types can be used for code and data storage. The label “Data” neither implies that the D-Flash is mapped to the data memory region, nor that it can only be used for data storage. It is used to distinguish the different Flash bank sectorizations.

The 32-Kbyte Flash device consists of 6 P-Flash and 2 D-Flash banks, while the 24-Kbyte Flash device consists of also of 6 P-Flash banks but with the upper 2 banks only 2 Kbytes each, and only 1 D-Flash bank. The XC886/888 ROM devices offer a single 4-Kbyte D-Flash bank.

The P-Flash banks are always grouped in pairs. As such, the P-Flash banks are also sometimes referred to as P-Flash bank pair. Each sector in a P-Flash bank is grouped with the corresponding sector from the other bank within a bank pair to form a P-Flash bank pair sector.

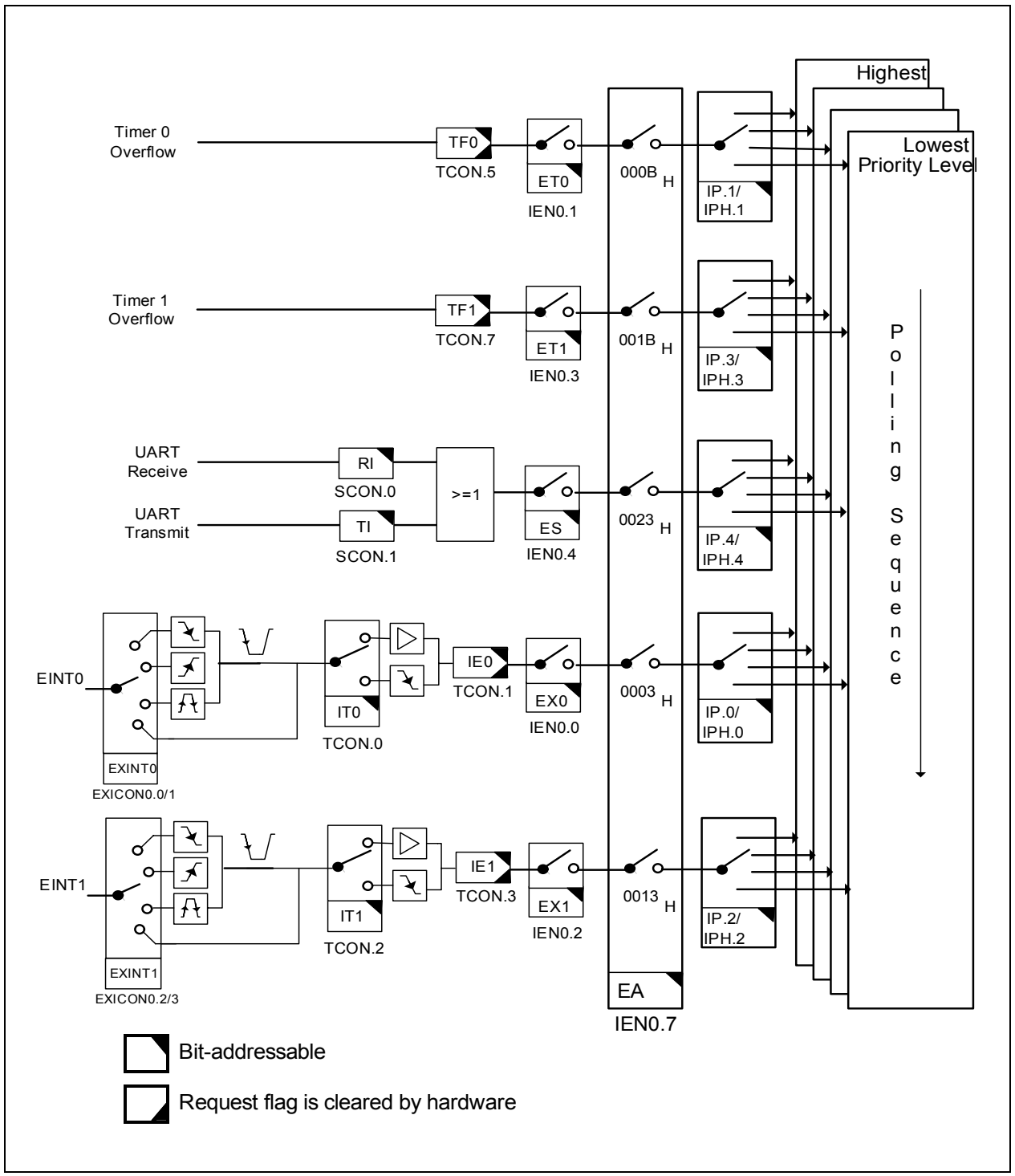


Figure 14 Interrupt Request Sources (Part 1)

3.4.3 Interrupt Priority

An interrupt that is currently being serviced can only be interrupted by a higher-priority interrupt, but not by another interrupt of the same or lower priority. Hence, an interrupt of the highest priority cannot be interrupted by any other interrupt request.

If two or more requests of different priority levels are received simultaneously, the request of the highest priority is serviced first. If requests of the same priority are received simultaneously, then an internal polling sequence determines which request is serviced first. Thus, within each priority level, there is a second priority structure determined by the polling sequence shown in **Table 21**.

Table 21 Priority Structure within Interrupt Level

Source	Level
Non-Maskable Interrupt (NMI)	(highest)
External Interrupt 0	1
Timer 0 Interrupt	2
External Interrupt 1	3
Timer 1 Interrupt	4
UART Interrupt	5
Timer 2,UART Normal Divider Overflow, MultiCAN, LIN Interrupt	6
ADC, MultiCAN Interrupt	7
SSC Interrupt	8
External Interrupt 2, Timer 21, UART1, UART1 Normal Divider Overflow, MDU, CORDIC Interrupt	9
External Interrupt [6:3], MultiCAN Interrupt	10
CCU6 Interrupt Node Pointer 0, MultiCAN interrupt	11
CCU6 Interrupt Node Pointer 1, MultiCAN Interrupt	12
CCU6 Interrupt Node Pointer 2, MultiCAN Interrupt	13
CCU6 Interrupt Node Pointer 3, MultiCAN Interrupt	14

3.6 Power Supply System with Embedded Voltage Regulator

The XC886/888 microcontroller requires two different levels of power supply:

- 3.3 V or 5.0 V for the Embedded Voltage Regulator (EVR) and Ports
- 2.5 V for the core, memory, on-chip oscillator, and peripherals

Figure 21 shows the XC886/888 power supply system. A power supply of 3.3 V or 5.0 V must be provided from the external power supply pin. The 2.5 V power supply for the logic is generated by the EVR. The EVR helps to reduce the power consumption of the whole chip and the complexity of the application board design.

The EVR consists of a main voltage regulator and a low power voltage regulator. In active mode, both voltage regulators are enabled. In power-down mode, the main voltage regulator is switched off, while the low power voltage regulator continues to function and provide power supply to the system with low power consumption.

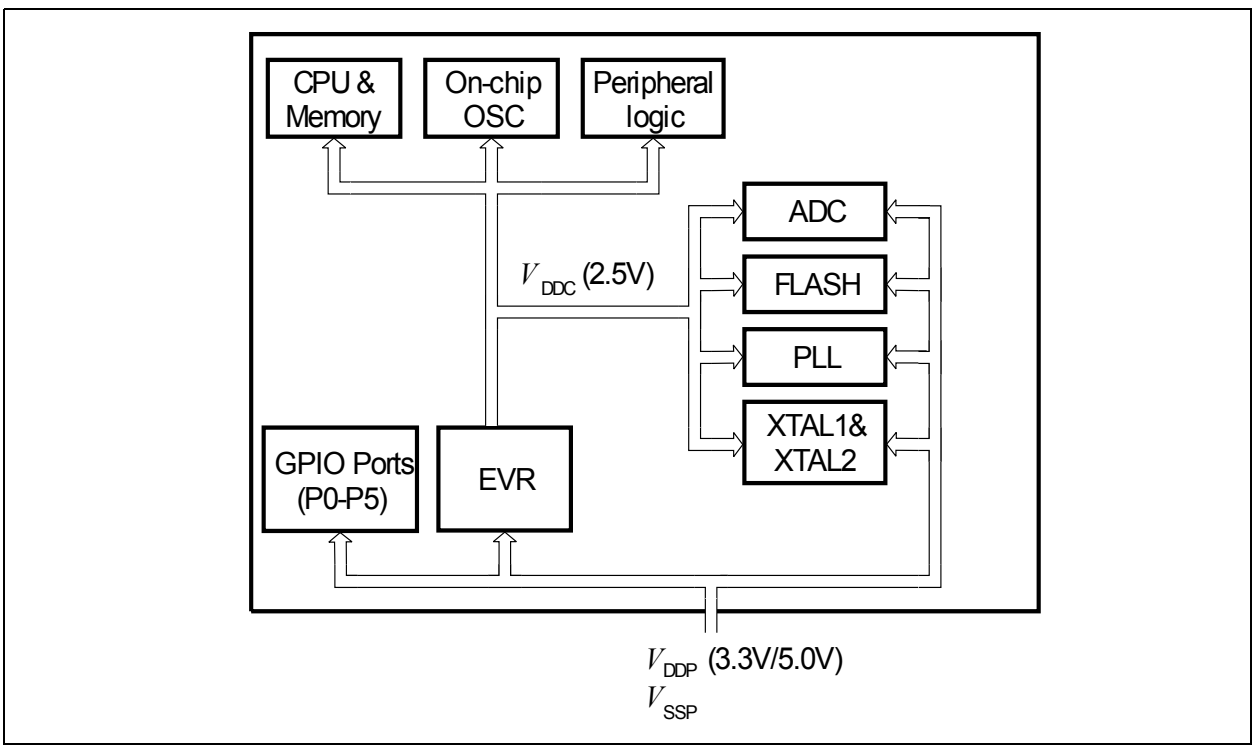


Figure 21 XC886/888 Power Supply System

EVR Features

- Input voltage (V_{DDP}): 3.3 V/5.0 V
- Output voltage (V_{DDC}): 2.5 V ± 7.5%
- Low power voltage regulator provided in power-down mode
- V_{DDC} and V_{DDP} prewarning detection
- V_{DDC} brownout detection

3.12 CORDIC Coprocessor

The CORDIC Coprocessor provides CPU with hardware support for the solving of circular (trigonometric), linear (multiply-add, divide-add) and hyperbolic functions.

Features

- Modes of operation
  - Supports all CORDIC operating modes for solving circular (trigonometric), linear (multiply-add, divide-add) and hyperbolic functions
  - Integrated look-up tables (LUTs) for all operating modes
- Circular vectoring mode: Extended support for values of initial X and Y data up to full range of $[-2^{15},(2^{15}-1)]$ for solving angle and magnitude
- Circular rotation mode: Extended support for values of initial Z data up to full range of $[-2^{15},(2^{15}-1)]$, representing angles in the range $[-\pi,((2^{15}-1)/2^{15})\pi]$ for solving trigonometry
- Implementation-dependent operational frequency of up to 80 MHz
- Gated clock input to support disabling of module
- 16-bit accessible data width
  - 24-bit kernel data width plus 2 overflow bits for X and Y each
  - 20-bit kernel data width plus 1 overflow bit for Z
  - With KEEP bit to retain the last value in the kernel register for a new calculation
- 16 iterations per calculation: Approximately 41 clock-cycles or less, from set of start (ST) bit to set of end-of-calculation flag, excluding time taken for write and read access of data bytes.
- Twos complement data processing
  - Only exception: X result data with user selectable option for unsigned result
- X and Y data generally accepted as integer or rational number; X and Y must be of the same data form
- Entries of LUTs are 20-bit signed integers
  - Entries of atan and atanh LUTs are integer representations (S19) of angles with the scaling such that $[-2^{15},(2^{15}-1)]$ represents the range $[-\pi,((2^{15}-1)/2^{15})\pi]$
  - Accessible Z result data for circular and hyperbolic functions is integer in data form of S15
- Emulated LUT for linear function
  - Data form is 1 integer bit and 15-bit fractional part (1.15)
  - Accessible Z result data for linear function is rational number with fixed data form of S4.11 (signed 4Q16)
- Truncation Error
  - The result of a CORDIC calculation may return an approximation due to truncation of LSBs
  - Good accuracy of the CORDIC calculated result data, especially in circular mode
- Interrupt
  - On completion of a calculation

– Interrupt enabling and corresponding flag

3.13 UART and UART1

The XC886/888 provides two Universal Asynchronous Receiver/Transmitter (UART and UART1) modules for full-duplex asynchronous reception/transmission. Both are also receive-buffered, i.e., they can commence reception of a second byte before a previously received byte has been read from the receive register. However, if the first byte still has not been read by the time reception of the second byte is complete, one of the bytes will be lost.

Features

- Full-duplex asynchronous modes
  – 8-bit or 9-bit data frames, LSB first
  – Fixed or variable baud rate
- Receive buffered
- Multiprocessor communication
- Interrupt generation on the completion of a data transmission or reception

The UART modules can operate in the four modes shown in **Table 29**.

Table 29 UART Modes

Operating Mode	Baud Rate
Mode 0: 8-bit shift register	$f_{PCLK}/2$
Mode 1: 8-bit shift UART	Variable
Mode 2: 9-bit shift UART	$f_{PCLK}/32$ or $f_{PCLK}/64$[1)]
Mode 3: 9-bit shift UART	Variable

1) For UART1 module, the baud rate is fixed at $f_{PCLK}/64$.

There are several ways to generate the baud rate clock for the serial port, depending on the mode in which it is operating. In mode 0, the baud rate for the transfer is fixed at $f_{PCLK}/2$. In mode 2, the baud rate is generated internally based on the UART input clock and can be configured to either $f_{PCLK}/32$ or $f_{PCLK}/64$. For UART1 module, only $f_{PCLK}/64$ is available. The variable baud rate is set by the underflow rate on the dedicated baud-rate generator. For UART module, the variable baud rate alternatively can be set by the overflow rate on Timer 1.

3.13.1 Baud-Rate Generator

Both UART modules have their own dedicated baud-rate generator, which is based on a programmable 8-bit reload value, and includes divider stages (i.e., prescaler and

3.17 Timer 0 and Timer 1

Timer 0 and Timer 1 can function as both timers or counters. When functioning as a timer, Timer 0 and Timer 1 are incremented every machine cycle, i.e. every 2 input clocks (or 2 PCLKs). When functioning as a counter, Timer 0 and Timer 1 are incremented in response to a 1-to-0 transition (falling edge) at their respective external input pins, T0 or T1.

Timer 0 and 1 are fully compatible and can be configured in four different operating modes for use in a variety of applications, see **Table 32**. In modes 0, 1 and 2, the two timers operate independently, but in mode 3, their functions are specialized.

Table 32 Timer 0 and Timer 1 Modes

Mode	Operation
0	**13-bit timer** The timer is essentially an 8-bit counter with a divide-by-32 prescaler. This mode is included solely for compatibility with Intel 8048 devices.
1	**16-bit timer** The timer registers, TLx and THx, are concatenated to form a 16-bit counter.
2	**8-bit timer with auto-reload** The timer register TLx is reloaded with a user-defined 8-bit value in THx upon overflow.
3	**Timer 0 operates as two 8-bit timers** The timer registers, TL0 and TH0, operate as two separate 8-bit counters. Timer 1 is halted and retains its count even if enabled.

3.21 Analog-to-Digital Converter

The XC886/888 includes a high-performance 10-bit Analog-to-Digital Converter (ADC) with eight multiplexed analog input channels. The ADC uses a successive approximation technique to convert the analog voltage levels from up to eight different sources. The analog input channels of the ADC are available at Port 2.

Features

- Successive approximation
- 8-bit or 10-bit resolution
  (TUE of ± 1 LSB and ± 2 LSB, respectively)
- Eight analog channels
- Four independent result registers
- Result data protection for slow CPU access
  (wait-for-read mode)
- Single conversion mode
- Autoscan functionality
- Limit checking for conversion results
- Data reduction filter
  (accumulation of up to 2 conversion results)
- Two independent conversion request sources with programmable priority
- Selectable conversion request trigger
- Flexible interrupt generation with configurable service nodes
- Programmable sample time
- Programmable clock divider
- Cancel/restart feature for running conversions
- Integrated sample and hold circuitry
- Compensation of offset errors
- Low power modes

3.21.1 ADC Clocking Scheme

A common module clock f_{ADC} generates the various clock signals used by the analog and digital parts of the ADC module:

- f_{ADCA} is input clock for the analog part.
- f_{ADCI} is internal clock for the analog part (defines the time base for conversion length and the sample time). This clock is generated internally in the analog part, based on the input clock f_{ADCA} to generate a correct duty cycle for the analog components.
- f_{ADCD} is input clock for the digital part.

The internal clock for the analog part f_{ADCI} is limited to a maximum frequency of 10 MHz. Therefore, the ADC clock prescaler must be programmed to a value that ensures f_{ADCI} does not exceed 10 MHz. The prescaler ratio is selected by bit field CTC in register

4.2.2 Supply Threshold Characteristics

Table 39 provides the characteristics of the supply threshold in the XC886/888.

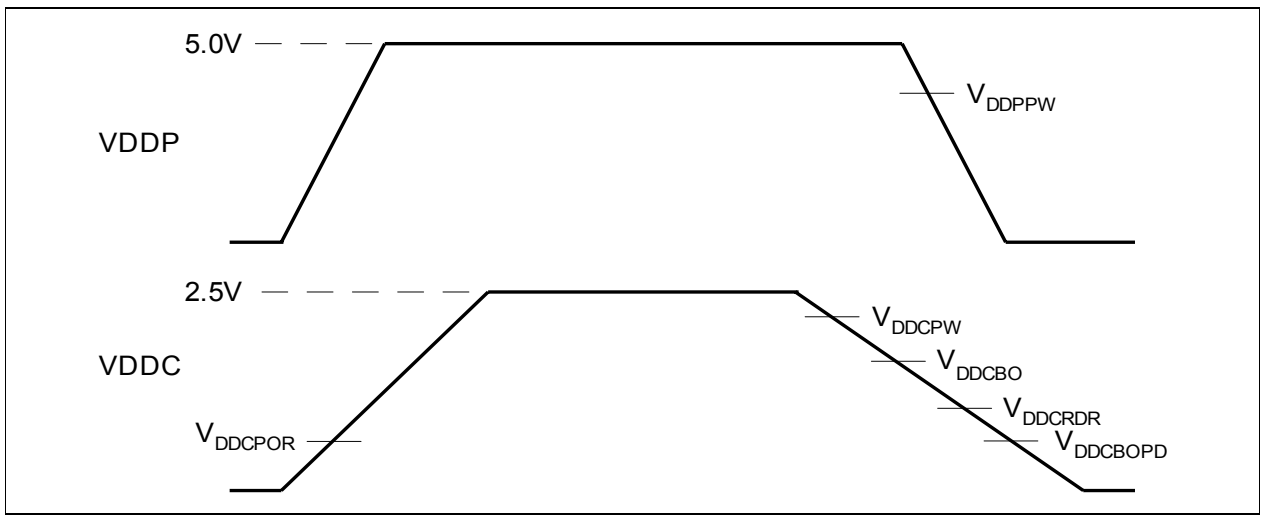


Figure 38 Supply Threshold Parameters

Table 39 Supply Threshold Parameters (Operating Conditions apply)

Parameters	Symbol		Limit Values			Unit
			min.	typ.	max.	
V_{DDC} prewarning voltage[1)]	V_{DDCPW}	CC	2.2	2.3	2.4	V
V_{DDC} brownout voltage in active mode[1)]	V_{DDCBO}	CC	2.0	2.1	2.2	V
RAM data retention voltage	V_{DDCRDR}	CC	0.9	1.0	1.1	V
V_{DDC} brownout voltage in power-down mode[2)]	$V_{DDCBOPD}$	CC	1.3	1.5	1.7	V
V_{DDP} prewarning voltage[3)]	V_{DDPPW}	CC	3.4	4.0	4.6	V
Power-on reset voltage[2)4)]	V_{DDCPOR}	CC	1.3	1.5	1.7	V

1) Detection is disabled in power-down mode.

2) Detection is enabled in both active and power-down mode.

3) Detection is enabled for external power supply of 5.0V.
Detection must be disabled for external power supply of 3.3V.

4) The reset of EVR is extended by 300 µs typically after the VDDC reaches the power-on reset voltage.

Table 43 Power Supply Current Parameters (Operating Conditions apply; V_{DDP} = 3.3V range)

Parameter	Symbol	Limit Values		Unit	Test Condition
		typ.[1]	max.[2]		
V_{DDP} = 3.3V Range					
Active Mode	I_{DDP}	25.6	31.0	mA	Flash Device[3]
		23.4	28.6	mA	ROM Device[3]
Idle Mode	I_{DDP}	19.9	24.7	mA	Flash Device[4]
		17.5	20.7	mA	ROM Device[4]
Active Mode with slow-down enabled	I_{DDP}	13.3	16.2	mA	Flash Device[5]
		11.5	13.7	mA	ROM Device[5]
Idle Mode with slow-down enabled	I_{DDP}	11.1	14.4	mA	Flash Device[6]
		9.3	11.4	mA	ROM Device[6]

1) The typical I_{DDP} values are periodically measured at T_A = + 25 °C and V_{DDP} = 3.3 V.

2) The maximum I_{DDP} values are measured under worst case conditions (T_A = + 125 °C and V_{DDP} = 3.6 V).

3) I_{DDP} (active mode) is measured with: CPU clock and input clock to all peripherals running at 24 MHz(set by on-chip oscillator of 9.6 MHz and NDIV in PLL_CON to 1001_B), $\overline{\text{RESET}}$ = V_{DDP}, no load on ports.

4) I_{DDP} (idle mode) is measured with: CPU clock disabled, watchdog timer disabled, input clock to all peripherals enabled and running at 24 MHz, $\overline{\text{RESET}}$ = V_{DDP}, no load on ports.

5) I_{DDP} (active mode with slow-down mode) is measured with: CPU clock and input clock to all peripherals running at 8 MHz by setting CLKREL in CMCON to 0110_B, $\overline{\text{RESET}}$ = V_{DDP}, no load on ports.

6) I_{DDP} (idle mode with slow-down mode) is measured with: CPU clock disabled, watchdog timer disabled, input clock to all peripherals enabled and running at 8 MHz by setting CLKREL in CMCON to 0110_B,, $\overline{\text{RESET}}$ = V_{DDP}, no load on ports.

Table 50 JTAG Timing (Operating Conditions apply; CL = 50 pF) (cont'd)

Parameter	Symbol		Limits		Unit	Test Conditions
			min	max		
TDO high impedance to valid output from TCK	t_4	CC	-	27	ns	5V Device[1)]
			-	36	ns	3.3V Device[1)]
TDO valid output to high impedance from TCK	t_5	CC	-	22	ns	5V Device[1)]
			-	28	ns	3.3V Device[1)]

1) Not all parameters are 100% tested, but are verified by design/characterization and test correlation.

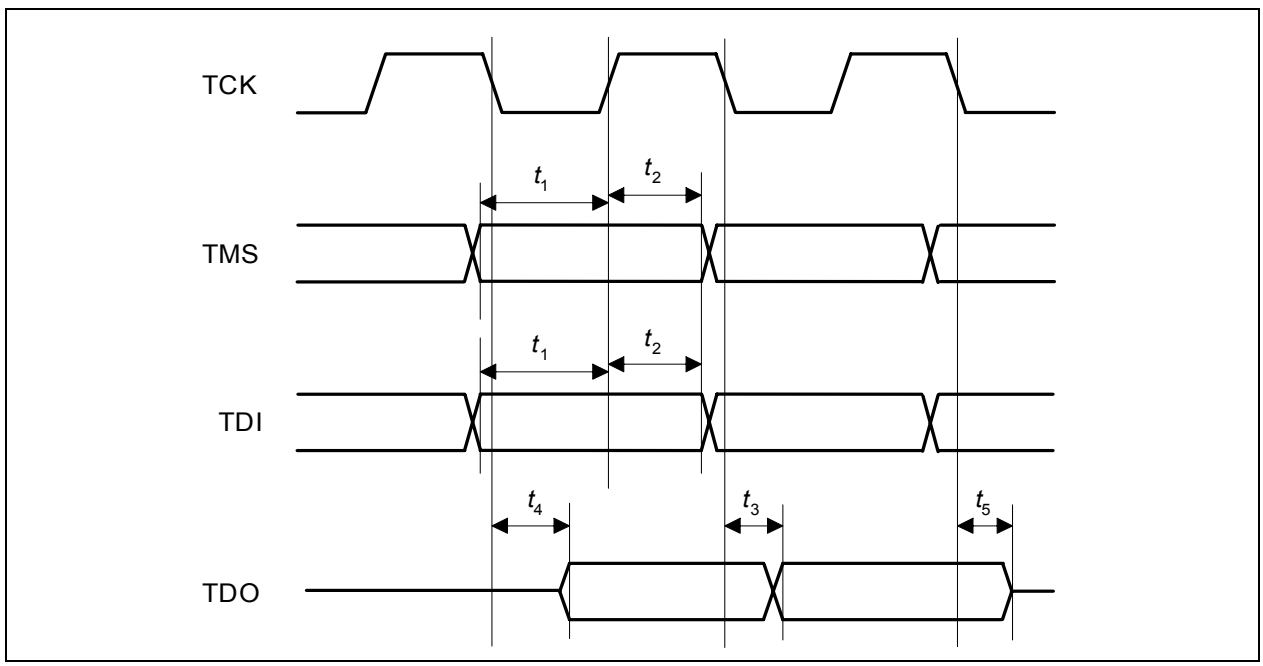
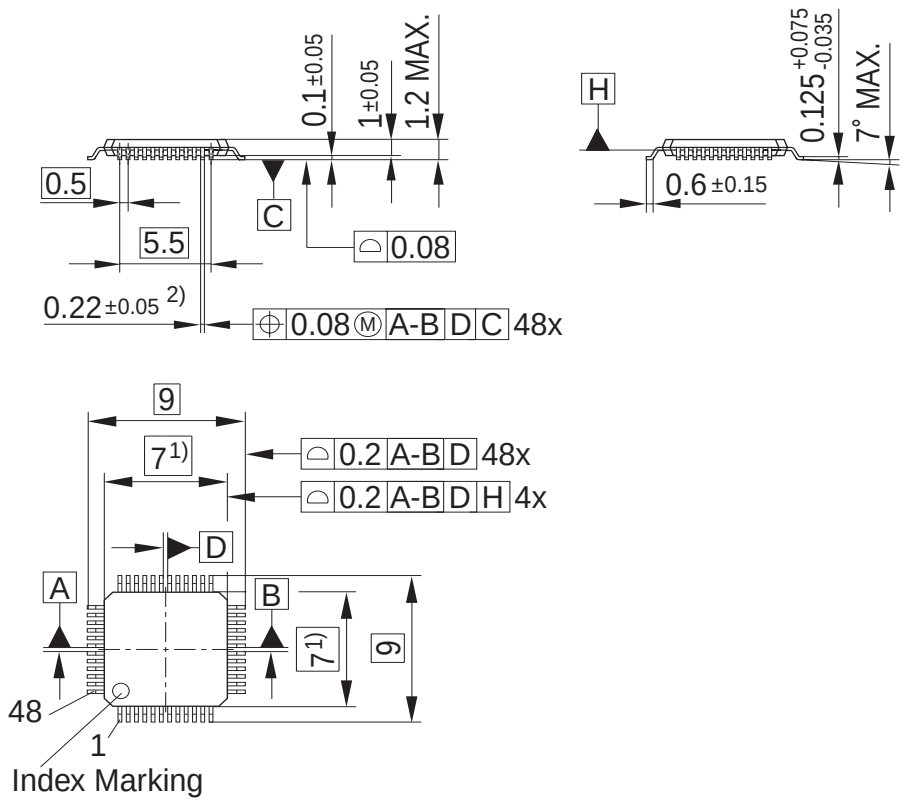


Figure 47 JTAG Timing

5.2 Package Outline

Figure 48 shows the package outlines of the XC886.



1) Does not include plastic or metal protrusion of 0.25 max. per side
2) Does not include dambar protrusion of 0.08 max. per side

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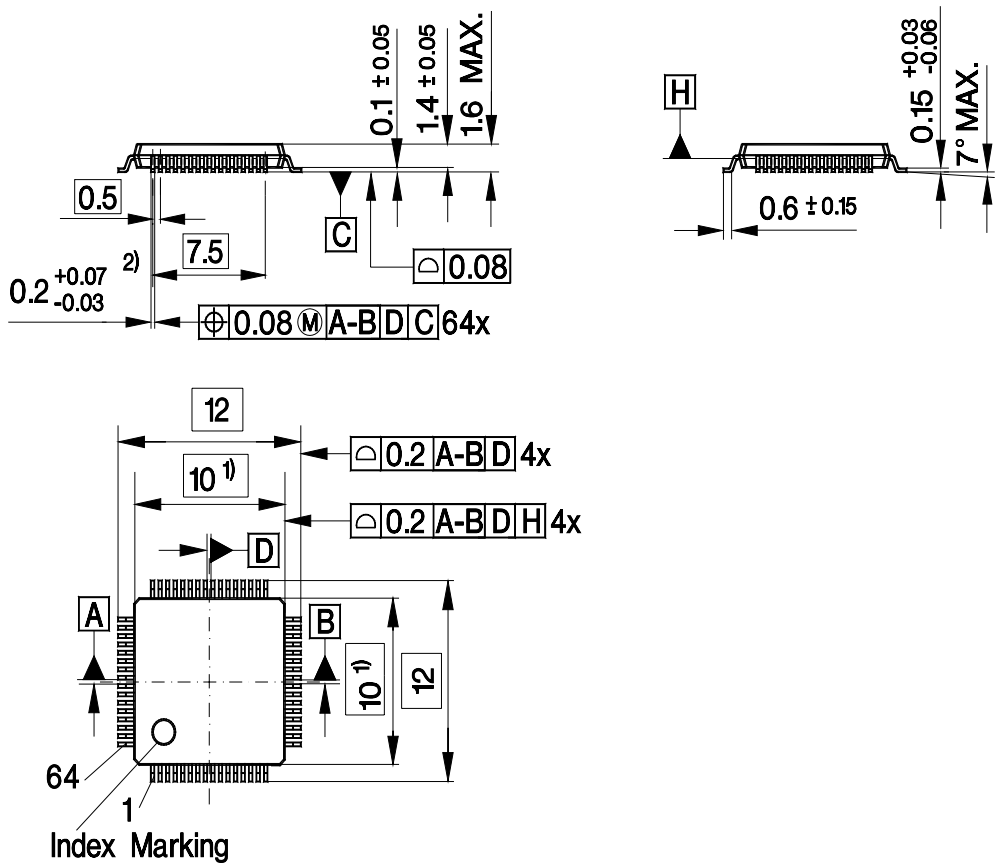
Figure 48 PG-TQFP-48 Package Outline

Figure 49 shows the package outlines of the XC888.



1) Does not include plastic or metal protrusion of 0.25 max. per side
2) Does not include dambar protrusion of 0.08 max. per side

Figure 49 PG-TQFP-64 Package Outline