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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	Z8
Core Size	8-Bit
Speed	12MHz
Connectivity	EBI/EMI
Peripherals	POR, WDT
Number of I/O	24
Program Memory Size	4KB (4K x 8)
Program Memory Type	OTP
EEPROM Size	-
RAM Size	237 x 8
Voltage - Supply (Vcc/Vdd)	3.5V ~ 5.5V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	-
Package / Case	-
Supplier Device Package	28-DIP
Purchase URL	https://www.e-xfl.com/product-detail/zilog/z86e3312pec

GENERAL DESCRIPTION (Continued)

nals, and parallel I/O with or without handshake, and address/data bus for interfacing external memory.

Notes: All signals with a preceding front slash, "/", are active Low. For example, B//W (WORD is active Low); /B/W (BYTE is active Low, only).

Power connections follow conventional descriptions below:

Connection	Circuit	Device
Power	V_{CC}	V_{DD}
Ground	GND	V_{SS}

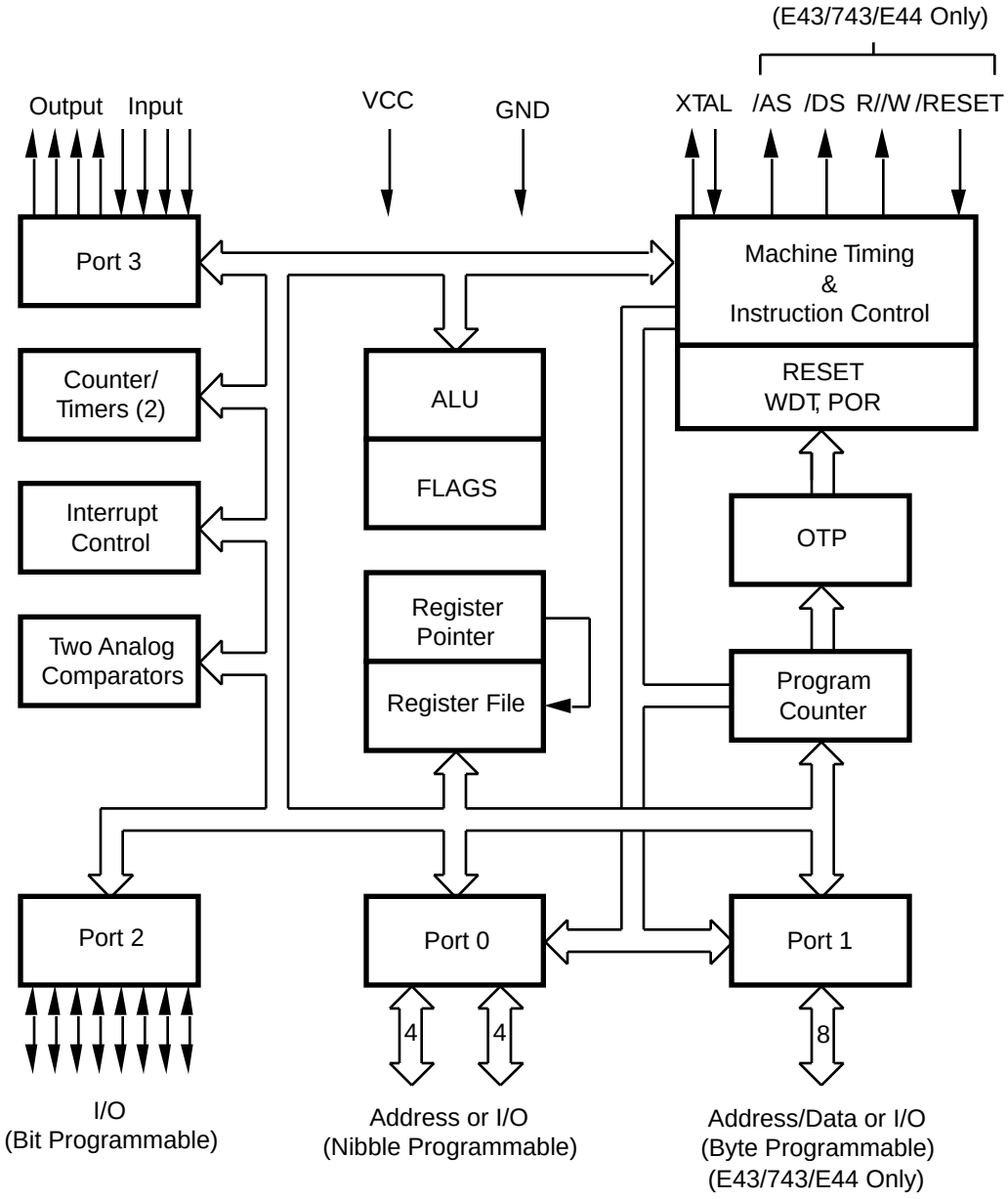

Figure 1. Functional Block Diagram

PIN IDENTIFICATION

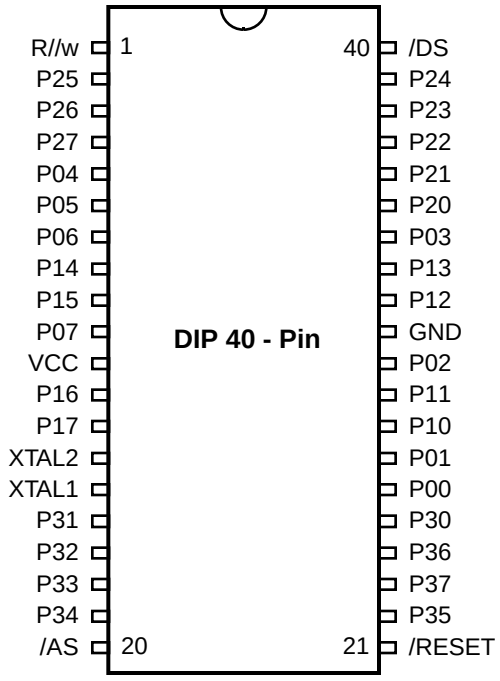

Figure 3. 40-Pin DIP Pin Configuration Standard Mode

Table 1. 40-Pin DIP Pin Identification Standard Mode

Pin #	Symbol	Function	Direction
1	R//W	Read/Write	Output
2-4	P25-P27	Port 2, Pins 5,6,7	In/Output
5-7	P04-P06	Port 0, Pins 4,5,6	In/Output
8-9	P14-P15	Port 1, Pins 4,5	In/Output
10	P07	Port 0, Pin 7	In/Output
11	V_{CC}	Power Supply	
12-13	P16-P17	Port 1, Pins 6,7	In/Output
14	XTAL2	Crystal Oscillator	Output
15	XTAL1	Crystal Oscillator	Input
16-18	P31-P33	Port 3, Pins 1,2,3	Input
19	P34	Port 3, Pin 4	Output
20	/AS	Address Strobe	Output
21	/RESET	Reset	Input
22	P35	Port 3, Pin 5	Output
23	P37	Port 3, Pin 7	Output
24	P36	Port 3, Pin 6	Output
25	P30	Port 3, Pin 0	Input
26-27	P00-P01	Port 0, Pins 0,1	In/Output
28-29	P10-P11	Port 1, Pins 0,1	In/Output
30	P02	Port 0, Pin 2	In/Output
31	GND	Ground	
32-33	P12-P13	Port 1, Pins 2,3	In/Output
34	P03	Port 0, Pin 3	In/Output
35-39	P20-P24	Port 2, Pins 0,1,2,3,4	In/Output
40	/DS	Data Strobe	Output

PIN IDENTIFICATION (Continued)

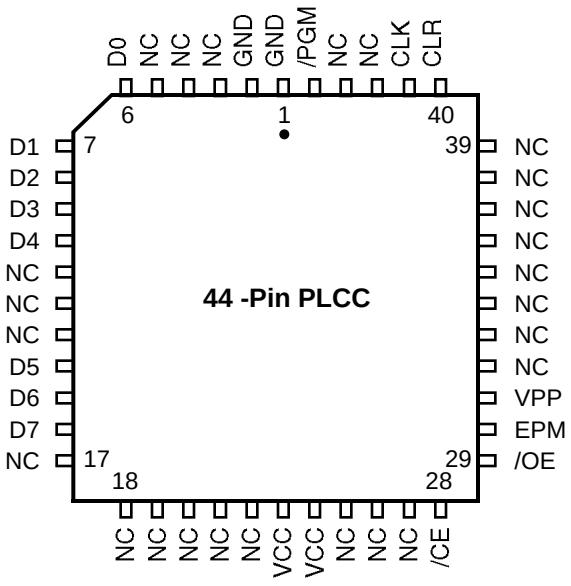

Figure 7. 44-Pin PLCC Pin Configuration EPROM Programming Mode

Table 5. 44-Pin PLCC Pin Configuration EPROM Programming Mode

Pin #	Symbol	Function	Direction
1-2	GND	Ground	
3-5	NC	No Connection	
6-10	D0-D4	Data 0,1,2,3,4	In/Output
11-13	NC	No Connection	
14-16	D5-D7	Data 5,6,7	In/Output
17-22	NC	No Connection	
23-24	VCC	Power Supply	
25-27	NC	No Connection	
28	/CE	Chip Select	Input

Table 5. 44-Pin PLCC Pin Configuration EPROM Programming Mode

Pin #	Symbol	Function	Direction
29	/OE	Output Enable	Input
30	EPM	EPROM Prog. Mode	Input
31	V_{PP}	Prog. Voltage	Input
32-39	NC	No Connection	
40	CLR	Clear	Input
41	CLK	Clock	Input
42-43	NC	No Connection	
44	/PGM	Prog. Mode	Input

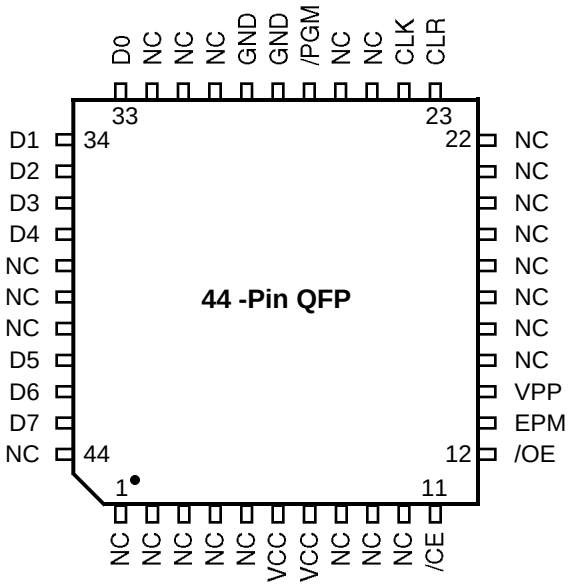

Figure 8. 44-Pin QFP Pin Configuration
EPROM Programming Mode

Table 6. 44-Pin QFP Pin Identification
EPROM Programming Mode

Pin #	Symbol	Function	Direction
1-5	NC	No Connection	
6-7	V_{CC}	Power Supply	
8-10	NC	No Connection	
11	/CE	Chip Select	Input
12	/OE	Output Enable	Input
13	EPM	EPROM Prog. Mode	Input
14	V_{PP}	Prog. Voltage	Input
15-22	NC	No Connection	
23	CLR	Clear	Input

Table 6. 44-Pin QFP Pin Identification
EPROM Programming Mode

Pin #	Symbol	Function	Direction
24	CLK	Clock	Input
25-26	NC	No Connection	
27	/PGM	Prog. Mode	Input
28-29	GND	Ground	
30-32	NC	No Connection	
33-37	D0-D4	Data 0,1,2,3,4	In/Output
38-40	NC	No Connection	
41-43	D5-D7	Data 5,6,7	In/Output
44	NC	No Connection	

PIN IDENTIFICATION (Continued)

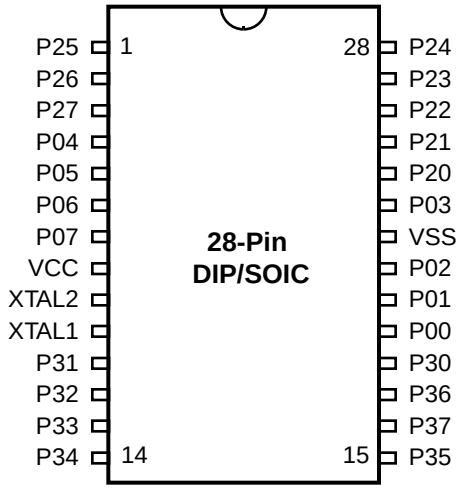

**Figure 9. Standard Mode
28-Pin DIP/SOIC Pin Configuration**

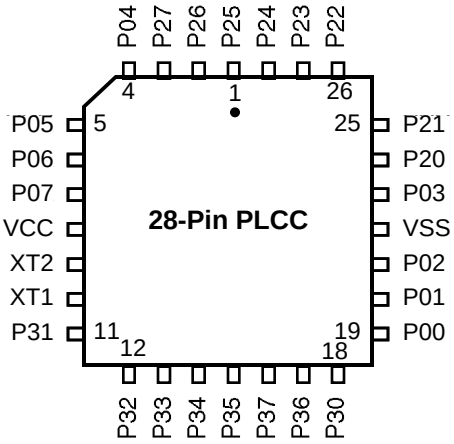

**Figure 10. Standard Mode
28-Pin PLCC Pin Configuration**

**Table 7. 28-Pin DIP/SOIC/PLCC
Pin Identification
Standard Mode**

Pin #	Symbol	Function	Direction
1-3	P25-P27	Port 2, Pins 5,6,	In/Output
4-7	P04-P07	Port 0, Pins 4,5,6,7	In/Output
8	V_{CC}	Power Supply	
9	XTAL2	Crystal Oscillator	Output
10	XTAL1	Crystal Oscillator	Input
11-13	P31-P33	Port 3, Pins 1,2,3	Input
14-15	P34-P35	Port 3, Pins 4,5	Output
16	P37	Port 3, Pin 7	Output
17	P36	Port 3, Pin 6	Output
18	P30	Port 3, Pin 0	Input
19-21	P00-P02	Port 0, Pins 0,1,2	In/Output
22	V_{SS}	Ground	
23	P03	Port 0, Pin 3	In/Output
24-28	P20-P24	Port 2, Pins 0,1,2,3,4	In/Output

DC ELECTRICAL CHARACTERISTICS (Continued)

			T_A=–40 °C to +105 °C					
Sym	Parameter	V_{CC} Note [3]	Min	Max	Typical @ 25°C	Units	Conditions	Notes
I_{ALL}	Auto Latch Low	4.5V	1.4	20	4.7	µA	$0V < V_{IN} < V_{CC}$	9
	Current	5.5V	1.4	20	4.7	µA	$0V < V_{IN} < V_{CC}$	9
I_{ALH}	Auto Latch High	4.5V	–1.0	–10	–3.8	µA	$0V < V_{IN} < V_{CC}$	9
	Current	5.5V	–1.0	–10	–3.8	µA	$0V < V_{IN} < V_{CC}$	9
T_{POR}	Power On Reset	4.5V	2.0	14	4	ms		
		5.5V	2.0	14	4	ms		
V_{LV}	Auto Reset Voltage		2.0	3.3	2.8	V		1

1. Device does function down to the Auto Reset voltage.
2. GND=0V
3. The V_{CC} voltage specification of 5.5V guarantees 5.0V ± 0.5V.
4. All outputs unloaded, I/O pins floating, inputs at rail.
5. CL1= CL2 = 22 pF
6. Same as note [4] except inputs at V_{CC}.
7. Maximum temperature is 70°C
8. STD Mode (not Low EMI Mode)
9. Auto Latch (mask option) selected
10. For analog comparator inputs when analog comparators are enabled.
11. Clock must be forced Low, when XTAL1 is clock driven and XTAL2 is floating.
12. Typicals are at V_{CC} = 5.0V
13. Z86E43/743/E44 only.
14. WDT is not running.

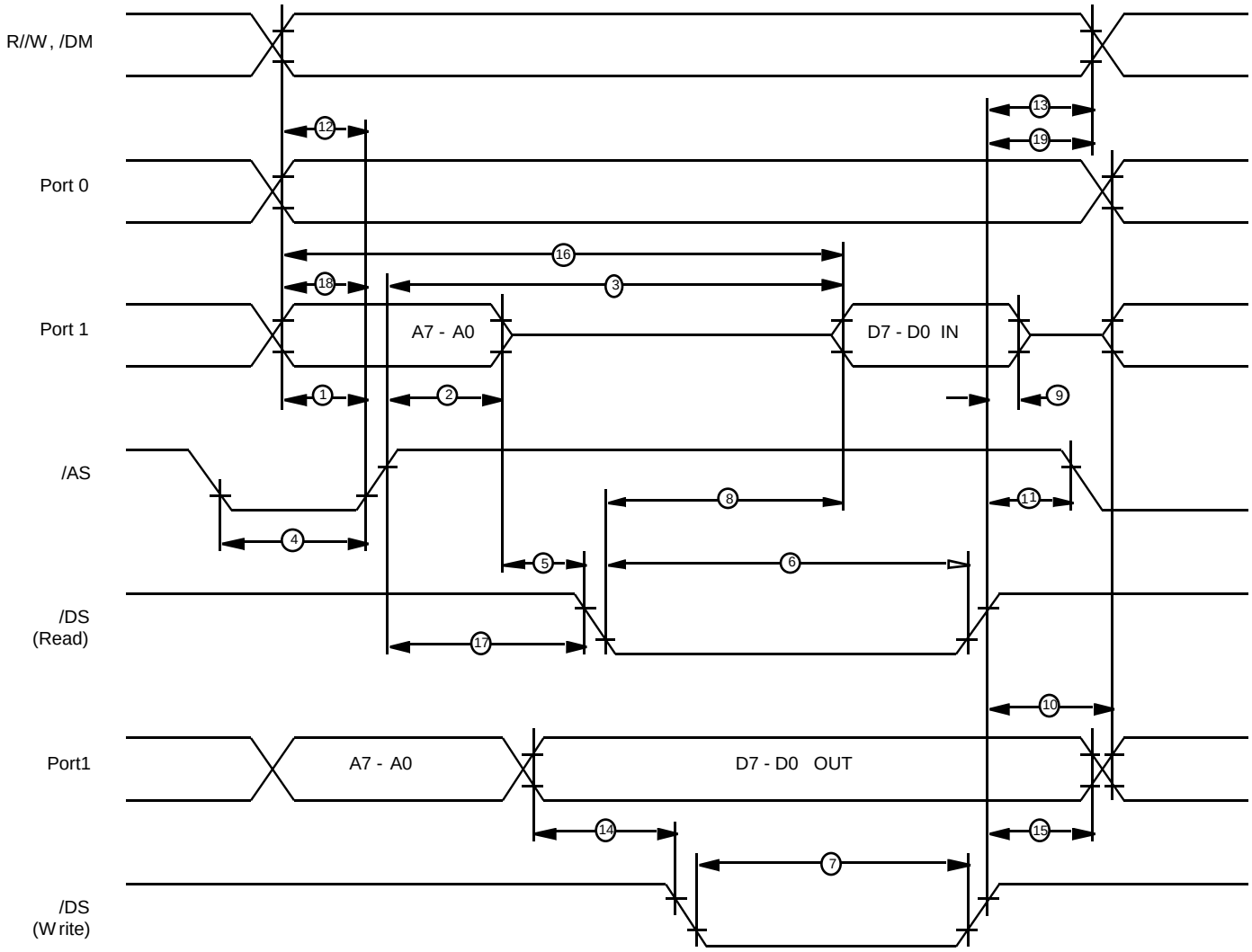

Figure 14. External I/O or Memory Read/Write Timing (Z86E43/743/E44 Only)

DC ELECTRICAL CHARACTERISTICS (Continued)

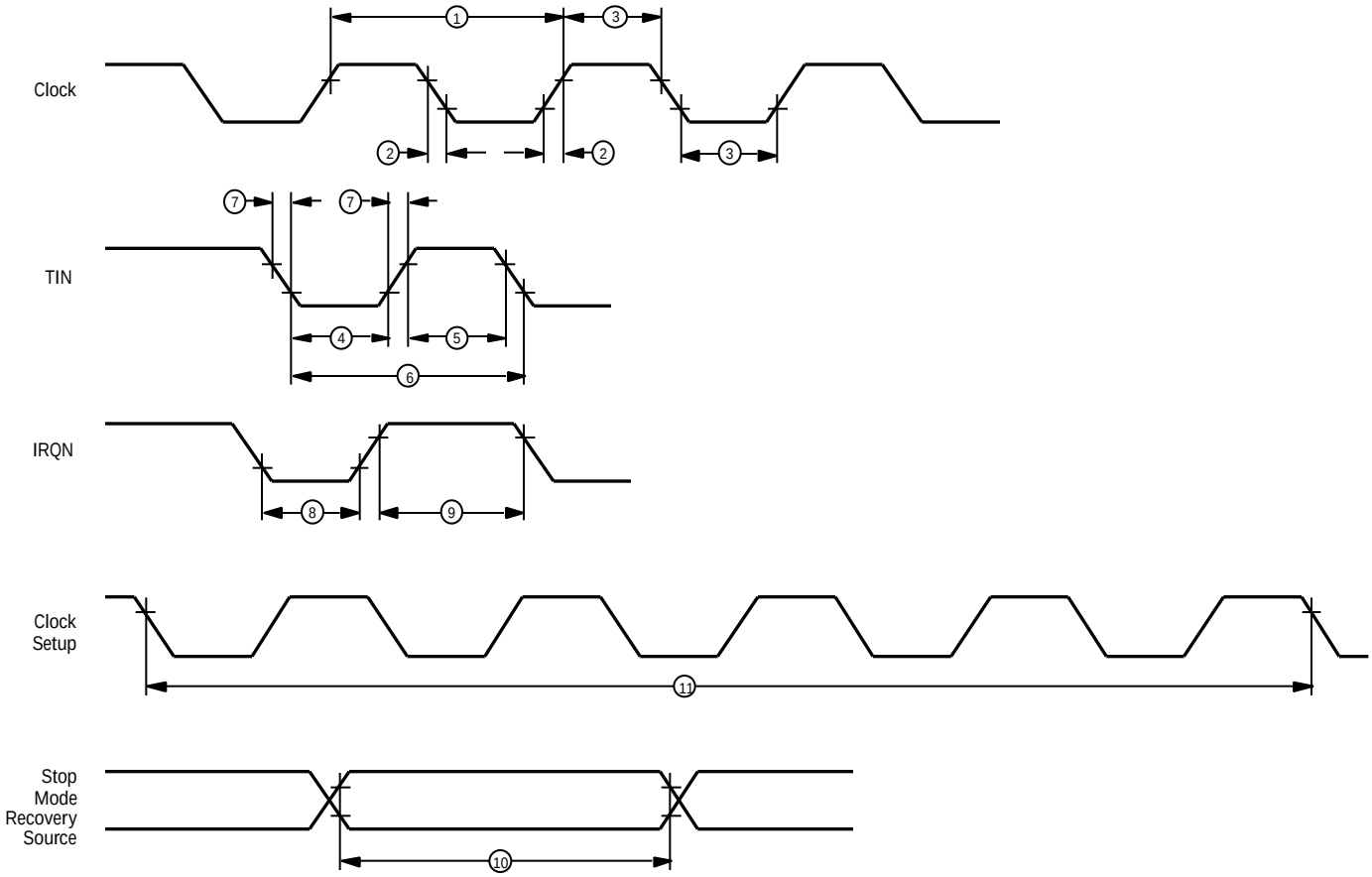

Figure 15. Additional Timing Diagram

Additional Timing Table (Divide-By-One Mode)

				T_A = 0 °C to +70 °C					
				4 MHz		6 MHz			
No	Symbol	Parameter	V_{CC} Note [6]	Min	Max	Min	Max	Units	Notes
1	TpC	Input Clock Period	3.5V	250	DC	166	DC	ns	1,7,8
			5.5V	250	DC	166	DC	ns	1,7,8
2	TrC,TfC	Clock Input Rise & Fall Times	3.5V		25		25	ns	1,7,8
			5.5V		25		25	ns	1,7,8
3	TwC	Input Clock Width	3.5V	100		100		ns	1,7,8
			5.5V	100		100		ns	1,7,8
4	TwTinL	Timer Input Low Width	3.5V	100		100		ns	1,7,8
			5.5V	70		70		ns	1,7,8
5	TwTinH	Timer Input High Width	3.5V	5TpC		5TpC			1,7,8
			5.5V	5TpC		5TpC			1,7,8
6	TpTin	Timer Input Period	3.5V	8TpC		8TpC			1,7,8
			5.5V	8TpC		8TpC			1,7,8
7	TrTin, TfTin	Timer Input Rise & Fall Timer	3.5V		100		100	ns	1,7,8
			5.5V		100		100	ns	1,7,8
8A	TwIL	Int. Request Low Time	3.5V	100		100		ns	1,2,7,8
			5.5V	70		70		ns	1,2,7,8
8B	TwIL	Int. Request Low Time	3.5V	5TpC		5TpC			1,3,7,8
			5.5V	5TpC		5TpC			1,3,7,8
9	TwIH	Int. Request Input High Time	3.5V	5TpC		5TpC			1,2,7,8
			5.5V	5TpC		5TpC			1,2,7,8
10	Twsm	STOP Mode Recovery Width Spec	3.5V	12		12		ns	4,8
			5.5V	12		12		ns	4,8
11	Tost	Oscillator Startup Time	3.5V		5TpC		5TpC		4,8,9
			5.5V		5TpC		5TpC		4,8,9

Notes:

1. Timing Reference uses 0.7 V_{CC} for a logic 1 and 0.2 V_{CC} for a logic 0.
2. Interrupt request via Port 3 (P31-P33).
3. Interrupt request via Port 3 (P30).
4. SMR-D5 = 1, POR STOP Mode Delay is on.
5. Reg. WDTMR.
6. The V_{CC} voltage specification of 5.5V guarantees 5.0V ±0.5V and the V_{CC} voltage specification of 3.5V guarantees 3.5V only.
7. SMR D1 = 0.
8. Maximum frequency for internal system clock is 4 MHz when using Low EMI OSC PCON Bit D7 = 0.
9. For RC and LC oscillator, and for oscillator driven by clock driver.

Additional Timing Table (Divide-By-One Mode)

				T_A = -40 °C to +105 °C					
				4 MHz		6 MHz			
No	Symbol	Parameter	V_{CC} Note [6]	Min	Max	Min	Max	Units	Notes
1	TpC	Input Clock Period	4.5V	250	DC	166	DC	ns	1,7,8
			5.5V	250	DC	166	DC	ns	1,7,8
2	TrC,TfC	Clock Input Rise &	4.5V		25		25	ns	1,7,8
		Fall Times	5.5V		25		25	ns	1,7,8
3	TwC	Input Clock Width	4.5V	100		100		ns	1,7,8
			5.5V	100		100		ns	1,7,8
4	TwTinL	Timer Input Low	4.5V	100		100		ns	1,7,8
		Width	5.5V	70		70		ns	1,7,8
5	TwTinH	Timer Input High	4.5V	5TpC		5TpC			1,7,8
		Width	5.5V	5TpC		5TpC			1,7,8
6	TpTin	Timer Input Period	4.5V	8TpC		8TpC			1,7,8
			5.5V	8TpC		8TpC			1,7,8
7	TrTin, TfTin	Timer Input Rise	4.5V		100		100	ns	1,7,8
		& Fall Timer	5.5V		100		100	ns	1,7,8
8A	TwIL	Int. Request Low	4.5V	100		100		ns	1,2,7,8
		Time	5.5V	70		70		ns	1,2,7,8
8B	TwIL	Int. Request Low	4.5V	5TpC		5TpC			1,3,7,8
		Time	5.5V	5TpC		5TpC			1,3,7,8
9	TwIH	Int. Request Input	4.5V	5TpC		5TpC			1,2,7,8
		High Time	5.5V	5TpC		5TpC			1,2,7,8
10	Twsm	STOP Mode	4.5V	12		12		ns	4,8
		Recovery Width	5.5V	12		12		ns	4,8
		Spec							
11	Tost	Oscillator Startup	4.5V		5TpC		5TpC		4,8,9
		Time	5.5V		5TpC		5TpC		4,8,9

Notes:

1. Timing Reference uses 0.7 V_{CC} for a logic 1 and 0.2 V_{CC} for a logic 0.
2. Interrupt request via Port 3 (P31-P33).
3. Interrupt request via Port 3 (P30).
4. SMR-D5 = 1, POR STOP Mode Delay is on.
5. Reg. WDTMR.
6. The V_{CC} voltage specification of 5.5V guarantees 5.0V ±0.5V and the V_{CC} voltage specification of 3.5V guarantees 3.5V only.
7. SMR D1 = 0.
8. Maximum frequency for internal system clock is 4 MHz when using Low EMI OSC PCON Bit D7 = 0.
9. For RC and LC oscillator, and for oscillator driven by clock driver.

Handshake Timing Diagrams

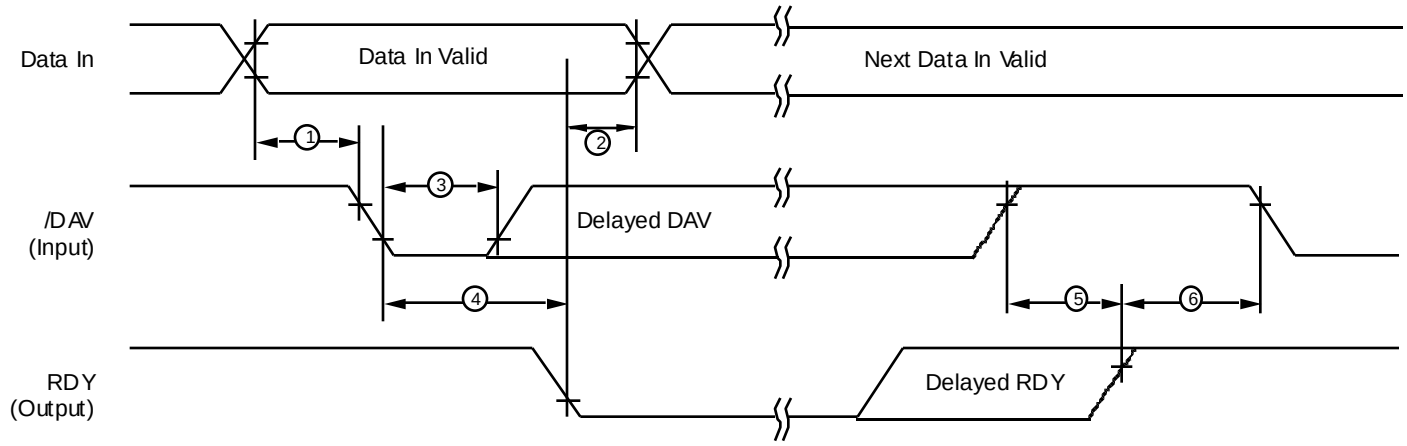

Figure 16. Input Handshake Timing

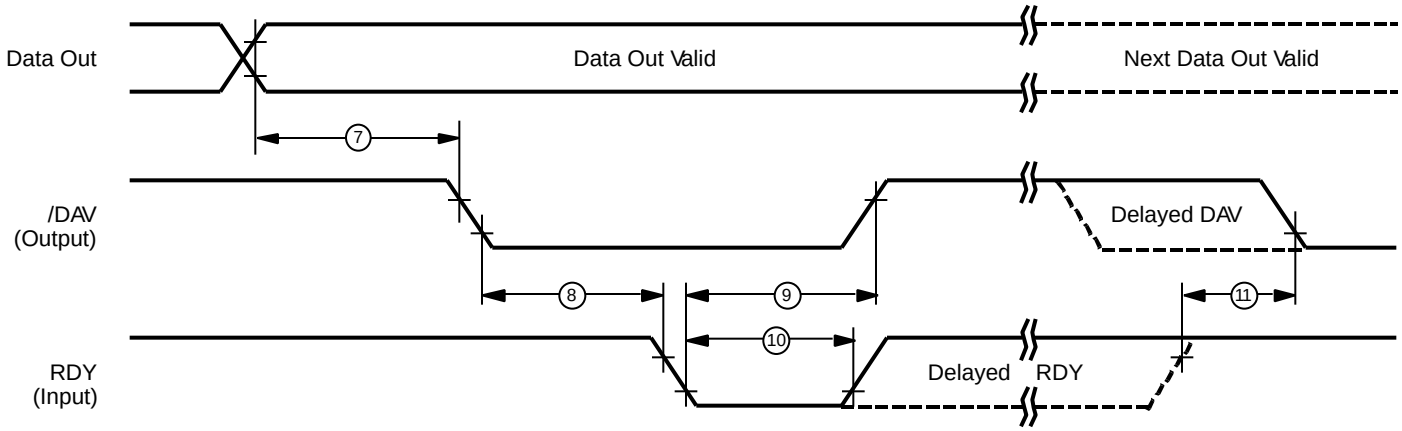

Figure 17. Output Handshake Timing

PIN FUNCTIONS (Continued)

Port 1 (P17-P10). Port 1 is an 8-bit, bidirectional, CMOS-compatible port with multiplexed Address (A7-A0) and Data (D7-D0) ports. These eight I/O lines can be programmed as inputs or outputs or can be configured under software control as an Address/Data port for interfacing external memory. The input buffers are Schmitt-triggered and the output buffers can be globally programmed as either push-pull or open-drain. Low EMI output buffers can be globally programmed by the software. Port 1 can be placed under handshake control. In this configuration, Port 3, lines P33 and P34 are used as the handshake controls RDY1 and /DAV1 (Ready and Data Available). To interface external memory, Port 1 must be programmed for the multiplexed Address/Data mode. If more than 256 external locations are required, Port 0 outputs the additional lines (Figure 19).

Port 1 can be placed in the high-impedance state along with Port 0, /AS, /DS, and R//W, allowing the Z86E43/743/E44 to share common resources in multiprocessor and DMA applications. In ROM mode, Port 1 is defined as input after reset.

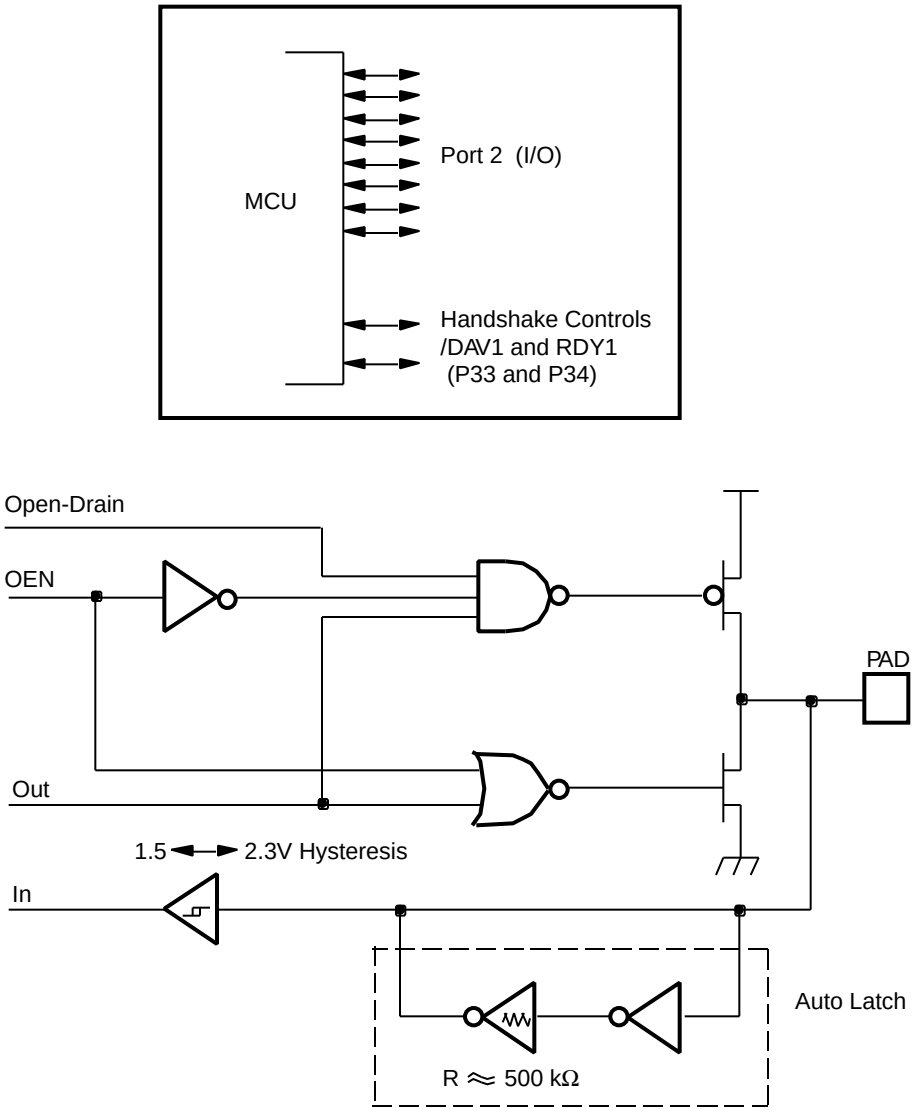

Figure 19. Port 1 Configuration (Z86E43/743/E44 Only)

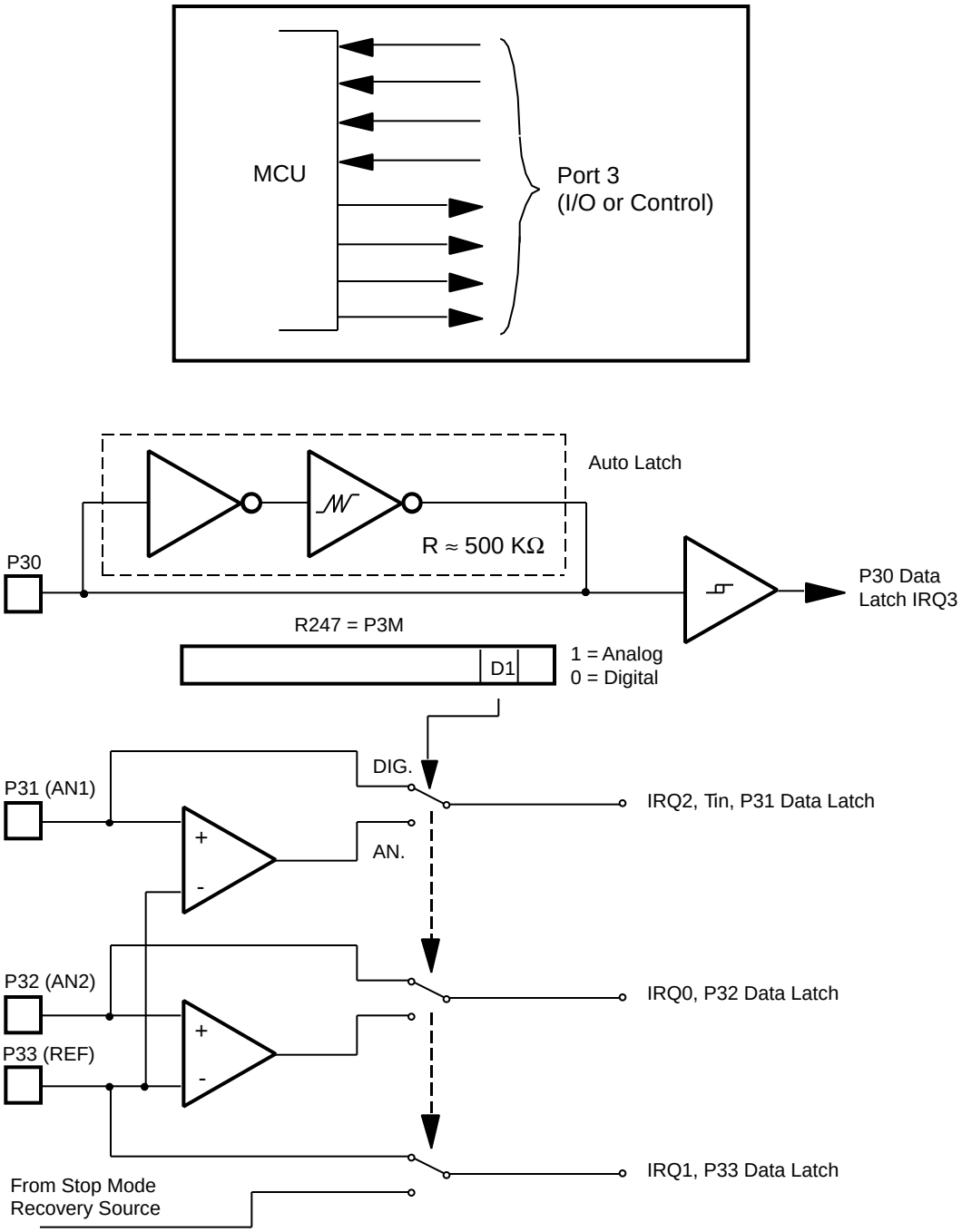

Figure 21. Port 3 Configuration

FUNCTIONAL DESCRIPTION

The MCU incorporates the following special functions to enhance the standard Z8 architecture to provide the user with increased design flexibility.

RESET. The device is reset in one of three ways:

1. Power-On Reset
2. Watch-Dog Timer
3. Stop-Mode Recovery Source

Note: Having the Auto Power-on Reset circuitry built-in, the MCU does not need to be connected to an external power-on reset circuit. The reset time is Tpor. The MCU does not re-initialize WDTMR, SMR, P2M, and P3M registers to their reset values on a Stop-Mode Recovery operation.

Note: The device V_{CC} must rise up to the operating V_{CC} specification before the TPOR expires.

Program Memory. The MCU can address up to 4/8/16 KB of Internal Program Memory (Figure 22). The first 12 bytes of program memory are reserved for the interrupt vectors. These locations contain six 16-bit vectors that correspond to the six available interrupts. For EPROM mode, byte 12 (000CH) to address 4095 (0FFFH)/8191 (1FFFH)/16384 (3FFFH), consists of programmable EPROM. After reset, the program counter points at the address 000CH, which is the starting address of the user program.

In ROMless mode, the Z86E43/743/E44 can address up to 64 KB of External Program Memory. The ROM/ROMless option is only available on the 44-pin devices.

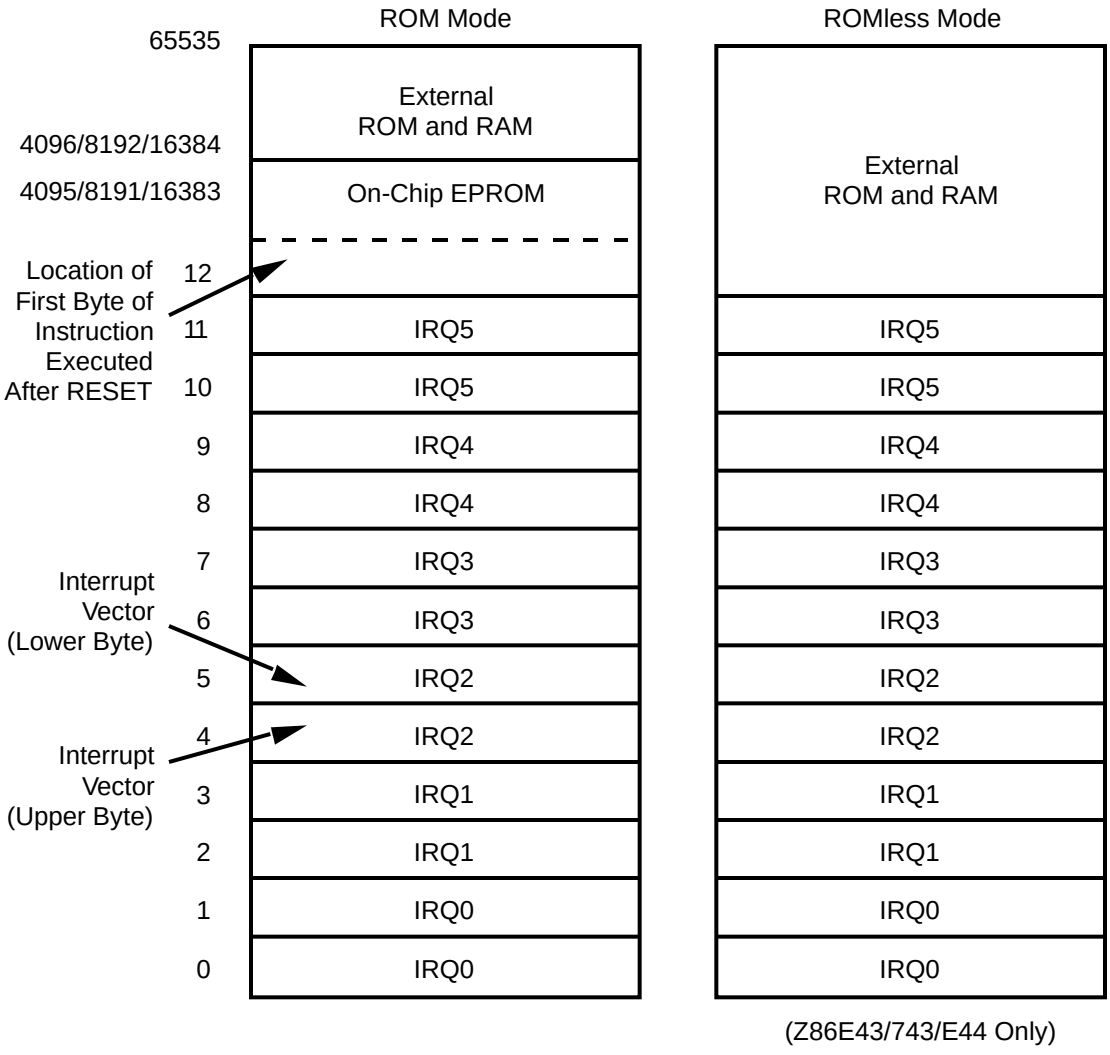

Figure 22. Program Memory Map

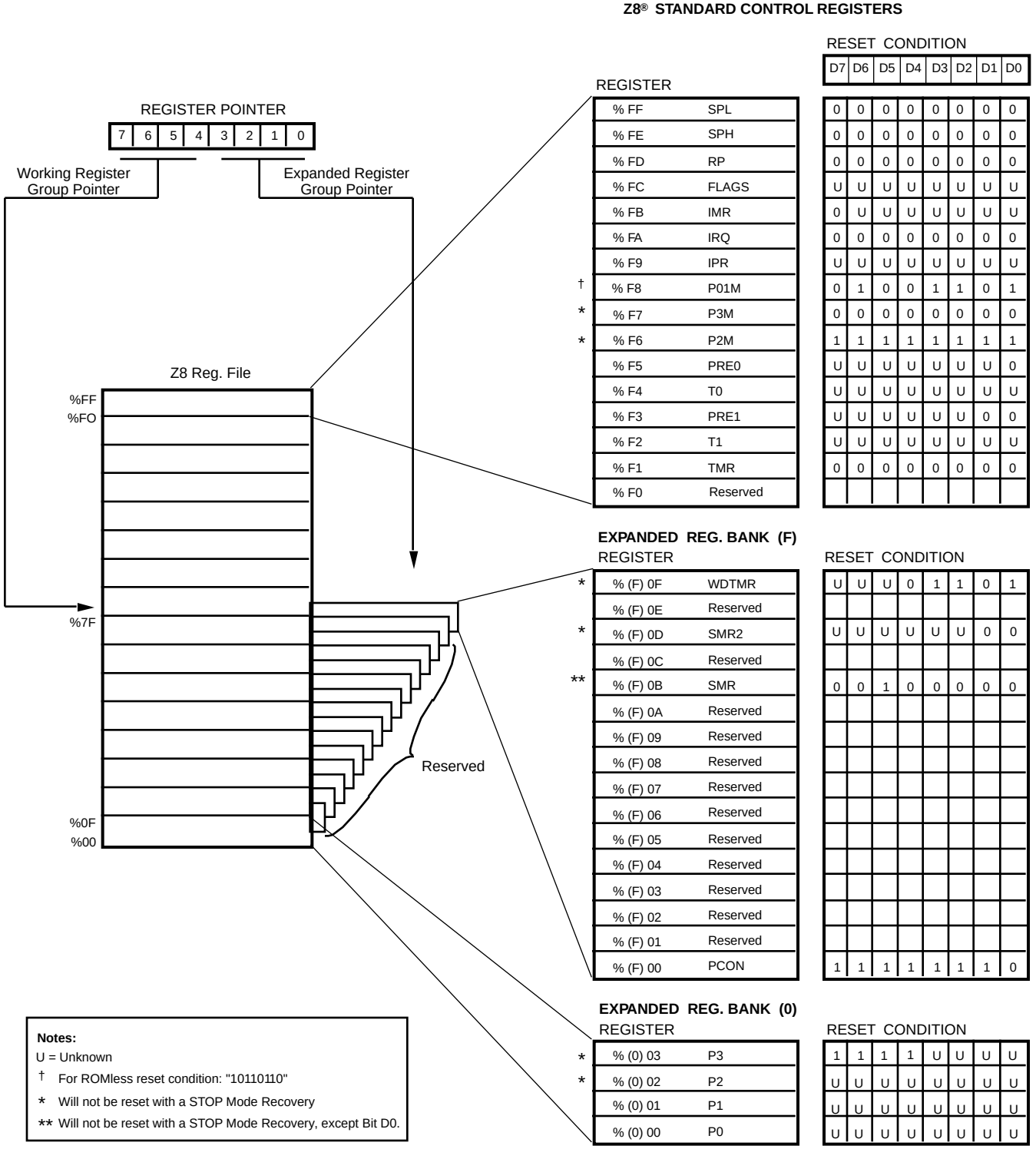

Figure 26. Expanded Register File Architecture

FUNCTIONAL DESCRIPTION (Continued)

Interrupts. The MCU has six different interrupts from six different sources. The interrupts are maskable and prioritized (Figure 28). The six sources are divided as follows: four sources are claimed by Port 3 lines P33-P30) and two in counter/timers. The Interrupt Mask Register globally or individually enables or disables the six interrupt requests (Table 10).

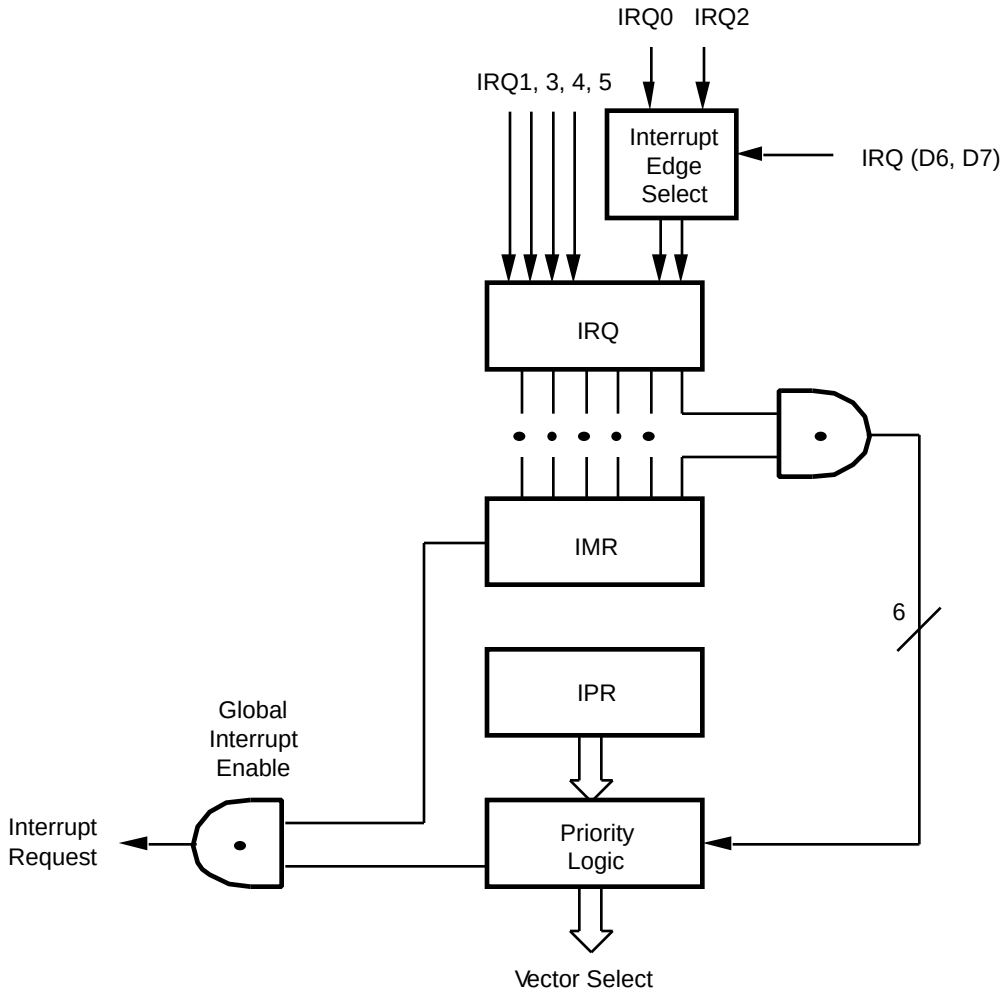

Figure 28. Interrupt Block Diagram

Table 10. Interrupt Types, Sources, and Vectors

Name	Source	Vector Location	Comments
IRQ0	/DAV0, IRQ0	0, 1	External (P32), Rising/Falling Edge Triggered
IRQ1	IRQ1	2, 3	External (P33), Falling Edge Triggered
IRQ2	/DAV2, IRQ2, T_{IN}	4, 5	External (P31), Rising/Falling Edge Triggered
IRQ3	IRQ3	6, 7	External (P30), Falling Edge Triggered
IRQ4	T0	8, 9	Internal
IRQ5	TI	10, 11	Internal

Comparator Output Port 3 (D0). Bit 0 controls the comparator output in Port 3. A "1" in this location brings the comparator outputs to P34 and P37, and a "0" releases the Port to its standard I/O configuration. The default value is 0.

Port 1 Open-Drain (D1). Port 1 can be configured as an open-drain by resetting this bit (D1=0) or configured as push-pull active by setting this bit (D1=1). The default value is 1.

Port 0 Open-Drain (D2). Port 0 can be configured as an open-drain by resetting this bit (D2=0) or configured as push-pull active by setting this bit (D2=1). The default value is 1.

Low EMI Port 0 (D3). Port 0 can be configured as a Low EMI Port by resetting this bit (D3=0) or configured as a Standard Port by setting this bit (D3=1). The default value is 1.

Low EMI Port 1 (D4). Port 1 can be configured as a Low EMI Port by resetting this bit (D4=0) or configured as a Standard Port by setting this bit (D4=1). The default value is 1. **Note:** The emulator does not support Port 1 low EMI mode and must be set D4 = 1.

Low EMI Port 2 (D5). Port 2 can be configured as a Low EMI Port by resetting this bit (D5=0) or configured as a Standard Port by setting this bit (D5=1). The default value is 1.

Low EMI Port 3 (D6). Port 3 can be configured as a Low EMI Port by resetting this bit (D6=0) or configured as a Standard Port by setting this bit (D6=1). The default value is 1.

Low EMI OSC (D7). This bit of the PCON Register controls the low EMI noise oscillator. A "1" in this location configures the oscillator with standard drive. While a "0" configures the oscillator with low noise drive, however, it does not affect the relationship of SCLK and XTAL. The low EMI mode will reduce the drive of the oscillator (OSC). The default value is 1. **Note:** 4 MHz is the maximum external clock frequency when running in the low EMI oscillator mode.

Stop-Mode Recovery Register (SMR). This register selects the clock divide value and determines the mode of Stop-Mode Recovery (Figure 31). All bits are Write Only except bit 7 which is a Read Only. Bit 7 is a flag bit that is hardware set on the condition of STOP Recovery and reset by a power-on cycle. Bit 6 controls whether a low or high level is required from the recovery source. Bit 5 controls the reset delay after recovery. Bits 2, 3, and 4 of the SMR register specify the Stop-Mode Recovery Source. The SMR is located in Bank F of the Expanded Register File at address 0BH.

FUNCTIONAL DESCRIPTION (Continued)

Table 12. Stop-Mode Recovery Source

D4	D3	D2	SMR Source selection
0	0	0	POR recovery only
0	0	1	P30 transition
0	1	0	P31 transition (Not in analog mode)
0	1	1	P32 transition (Not in analog mode)
1	0	0	P33 transition (Not in analog mode)
1	0	1	P27 transition
1	1	0	Logical NOR of Port 2 bits 0-3
1	1	1	Logical NOR of Port 2 bits 0-7

Stop-Mode Recovery Delay Select (D5). The 5 ms RESET delay after Stop-Mode Recovery is disabled by programming this bit to a zero. A "1" in this bit will cause a 5 ms RESET delay after Stop-Mode Recovery. The default condition of this bit is 1. If the fast wake up mode is selected, the Stop-Mode Recovery source needs to be kept active for at least 5TpC.

Stop-Mode Recovery Level Select (D6). A "1" in this bit defines that a high level on any one of the recovery sources wakes the MCU from STOP Mode. A 0 defines low level recovery. The default value is 0.

Cold or Warm Start (D7). This bit is set by the device upon entering STOP Mode. A "0" in this bit indicates that the device has been reset by POR (cold). A "1" in this bit indicates the device was awakened by a SMR source (warm).

Stop-Mode Recovery Register 2 (SMR2). This register contains additional Stop-Mode Recovery sources. When the Stop-Mode Recovery sources are selected in this register then SMR Register Bits D2, D3, and D4 must be 0.

SMR:10		Operation
D1	D0	Description of Action
0	0	POR and/or external reset recovery
0	1	Logical AND of P20 through P23
1	0	Logical AND of P20 through P27

Watch-Dog Timer Mode Register (WDTMR). The WDT is a retriggerable one-shot timer that resets the Z8 if it reaches its terminal count. The WDT is disabled after Power-On Reset and initially enabled by executing the WDT instruction and refreshed on subsequent executions of the WDT instruction. The WDT is driven either by an on-board RC oscillator or an external oscillator from XTAL1 pin. The POR clock source is selected with bit 4 of the WDT register.

Note: Execution of the WDT instruction affects the Z (Zero), S (Sign), and V (Overflow) flags.

WDT Time-Out Period (D0 and D1). Bits 0 and 1 control a tap circuit that determines the time-out periods that can be obtained (Table 13). The default value of D0 and D1 are 1 and 0, respectively.

Table 13. Time-out Period of WDT

D1	D0	Time-out of the Internal RC OSC	Time-out of the System Clock
0	0	5 ms	128 SCLK
0	1	10 ms*	256 SCLK*
1	0	20 ms	512 SCLK
1	1	80 ms	2048 SCLK

Notes:
*The default setting is 10 ms.

WDT During HALT Mode (D2). This bit determines whether or not the WDT is active during HALT Mode. A "1" indicates that the WDT is active during HALT. A "0" disables the WDT in HALT Mode. The default value is "1".

WDT During STOP Mode (D3). This bit determines whether or not the WDT is active during STOP mode. A "1" indicates active during STOP. A "0" disables the WDT during STOP Mode. This is applicable only when the WDT clock source is the internal RC oscillator.

Clock Source For WDT (D4). This bit determines which oscillator source is used to clock the internal POR and WDT counter chain. If the bit is a 1, the internal RC oscillator is bypassed and the POR and WDT clock source is driven from the external pin, XTAL1, and the WDT is stopped in STOP Mode. The default configuration of this bit is 0, which selects the RC oscillator.

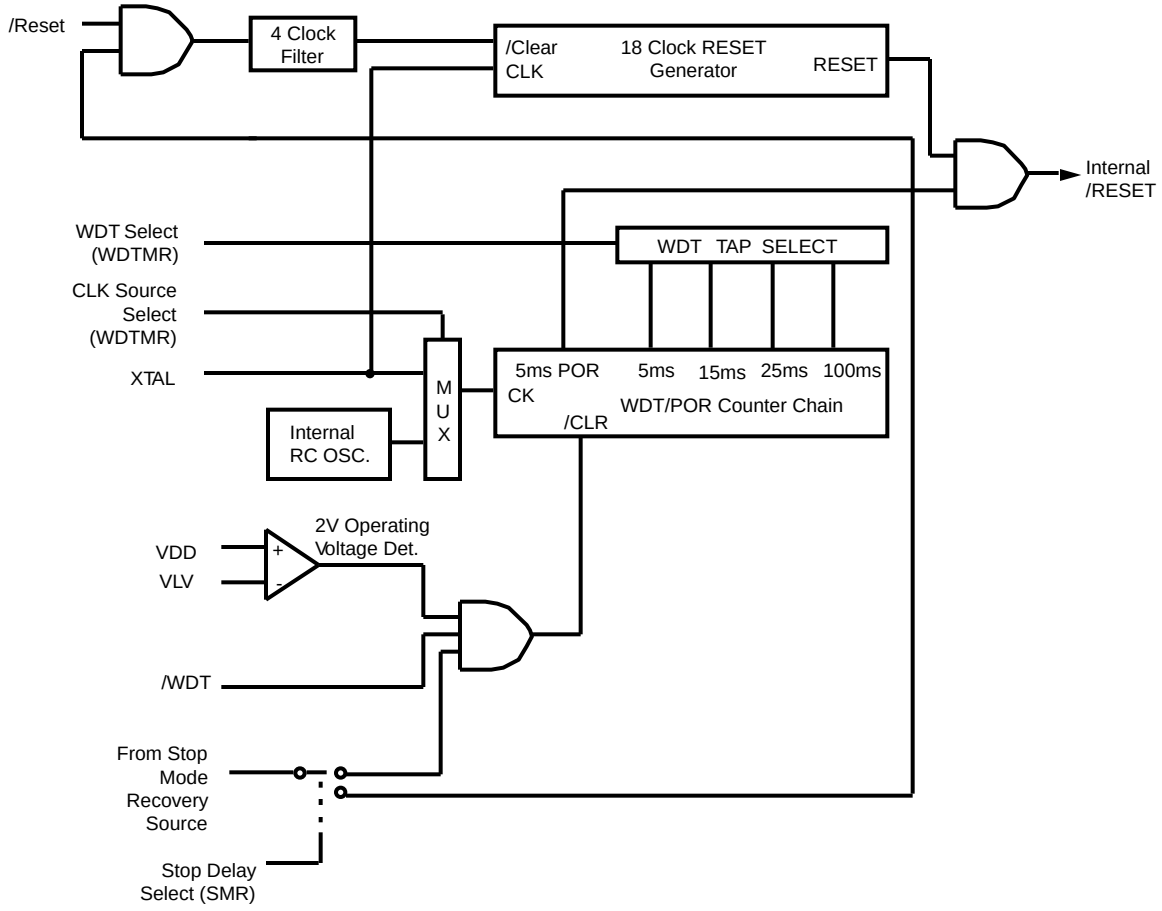

Figure 34. Resets and WDT

ORDERING INFORMATION

Z86E43/743/E44 (12 MHz)

40-Pin DIP	44-Pin PLCC	44-Pin QFP
Z86E4312PSC	Z86E4312VSC	Z86E4312FSC
Z86E4312PEC	Z86E4312VEC	Z86E4312FEC
Z8674312PSC	Z8674312VSC	Z8674312FSC
Z8674312PEC	Z8674312VEC	Z8674312FEC
Z86E4412PSC	Z86E4412VSC	Z86E4412FSC
Z86E4412PEC	Z86E4412VEC	Z86E4412FEC

Z86E33/733/E34 (12 MHz)

28-Pin DIP	28-Pin SOIC	28-Pin PLCC
Z86E3312PSC	Z86E3312SSC	Z86E3312VSC
Z86E3312PEC	Z86E3312SEC	Z86E3312VEC
Z8673312PSC	Z8673312SSC	Z8673312VSC
Z8673312PEC	Z8673312SEC	Z8673312VEC
Z86E3412PSC	Z86E3412SSC	Z86E3412VSC
Z86E3412PEC	Z86E3412SEC	Z86E3412VEC

For fast results, contact your local Zilog sales office for assistance in ordering the part desired.

Package

P = Plastic DIP
V = Plastic Chip Carrier
F = Plastic Quad Flat Pack
S = SOIC (Small Outline Integrated Circuit)

Speed

12 = 12 MHz

Environmental

C = Plastic Standard

Temperature

S = 0 °C to +70 °C
E = -40 °C to +105 °C

Example:

Z 86E43 12 P S C is a Z8E43, 12 MHz, DIP, 0° to +70°C, Plastic Standard Flow