Lattice Semiconductor Corporation - ISPLSI 5256VE-100LT128 Datasheet

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Understanding Embedded - CPLDs (Complex Programmable Logic Devices)

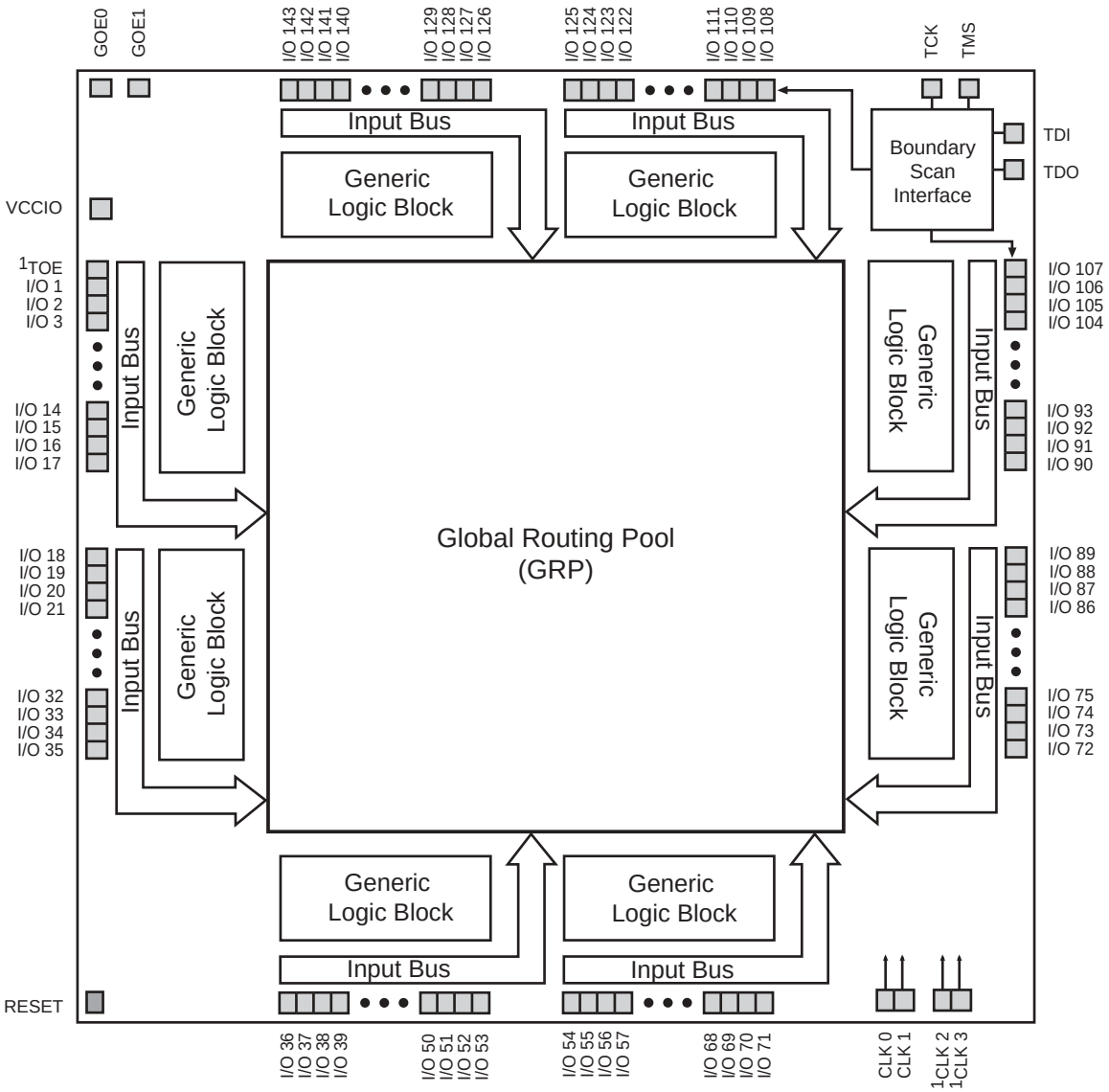
Embedded - CPLDs, or Complex Programmable Logic Devices, are highly versatile digital logic devices used in electronic systems. These programmable components are designed to perform complex logical operations and can be customized for specific applications. Unlike fixed-function ICs, CPLDs offer the flexibility to reprogram their configuration, making them an ideal choice for various embedded systems. They consist of a set of logic gates and programmable interconnects, allowing designers to implement complex logic circuits without needing custom hardware.

Applications of Embedded - CPLDs

Details	
Product Status	Obsolete
Programmable Type	In System Programmable
Delay Time tpd(1) Max	10 ns
Voltage Supply - Internal	3V ~ 3.6V
Number of Logic Elements/Blocks	8
Number of Macrocells	256
Number of Gates	12000
Number of I/O	96
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	128-LQFP
Supplier Device Package	128-TQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/isplsi-5256ve-100lt128

Functional Block Diagram

Figure 1. ispLSI 5256VE Functional Block Diagram (144-I/O Option)



1. CLK2, CLK3 and TOE signals are shared with I/O signals. Use the table below to determine which I/O is shared by package type.

Package Type	Multplexed Signals		
100 TQFP	1/O 44 / CLK2	I/O 49 / CLK 3	I/O 0 / TOE
128 TQFP	I/O 59 / CLK2	I/O 65 / CLK3	I/O 0 / TOE
256 fpBGA	I/O 119 / CLK2	I/O 131 / CLK3	I/O 0 / TOE
272 BGA	I/O 119 / CLK2	I/O 131 / CLK3	I/O 0 / TOE

Figure 2. ispLSI 5256VE Block Diagram (144 I/O Version)

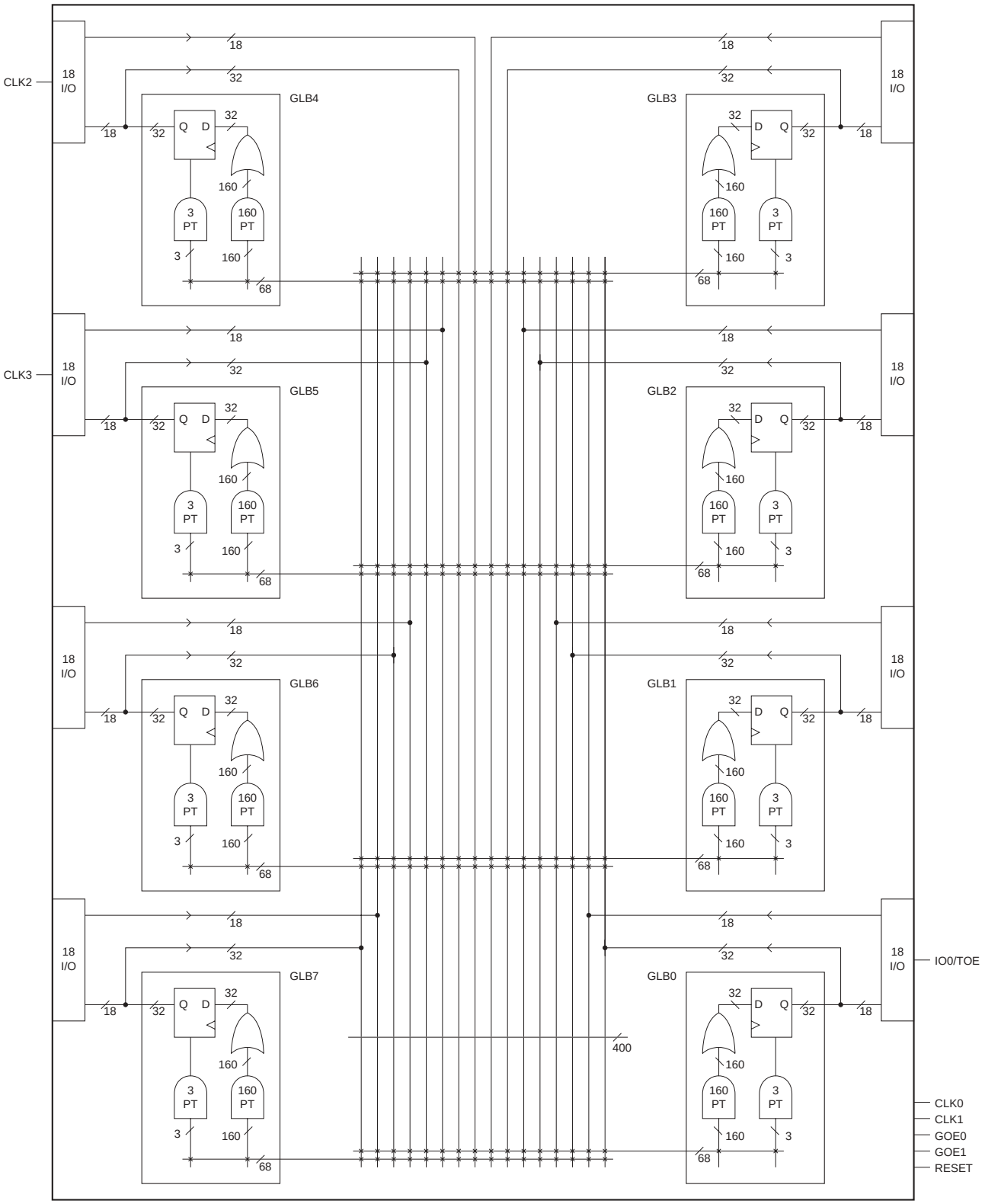


Figure 3. ispLSI 5000VE Generic Logic Block (GLB)

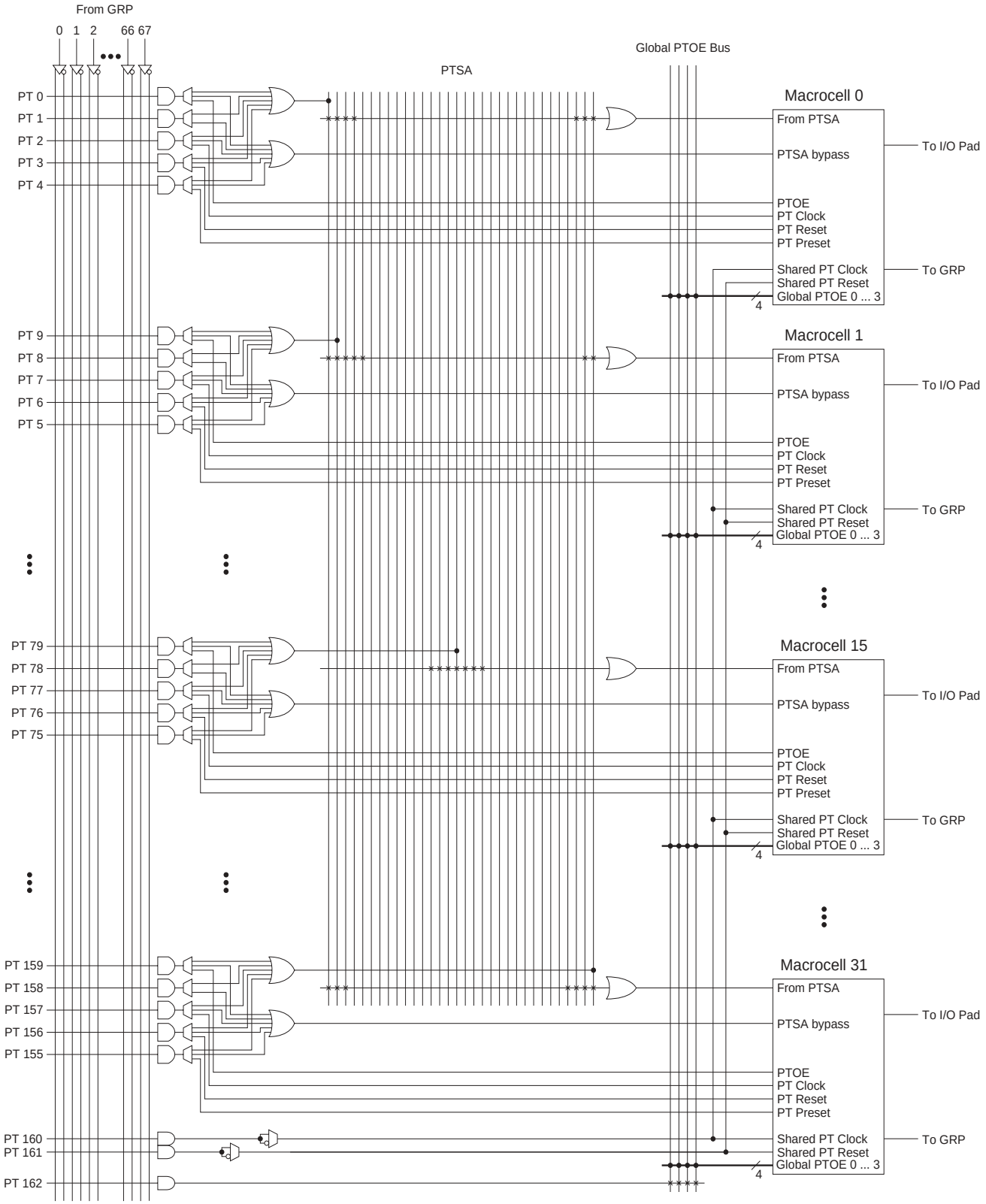
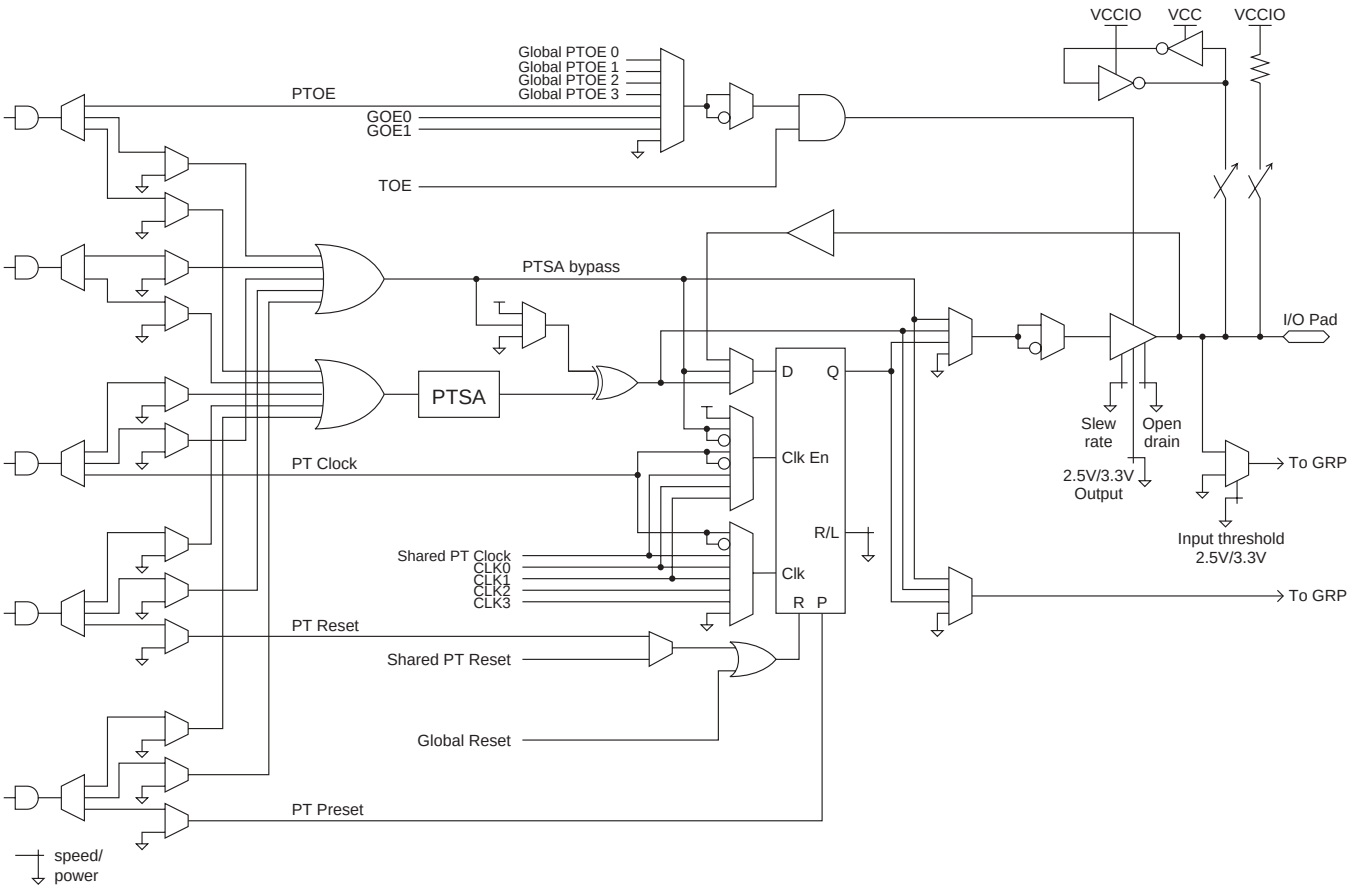


Figure 4. ispLSI 5000VE Macrocell



Note: Not all macrocells have I/O pads.

Global Clock Distribution

The ispLSI 5000VE Family has four dedicated clock input pins: CLK0 - CLK3. CLK0 input is used as the dedicated master clock that has the lowest internal clock skew with no clock inversion to maintain the fastest internal clock speed. The clock inversion is available on the remaining CLK1 - CLK3 signals. By sharing the pins with the I/O pins, CLK2 and CLK3 can not only be inverted but are also available for logic implementation through GRP signal routing. Figure 5 shows these different clock distribution options.

Figure 5. ispLSI 5000VE Global Clock Structure

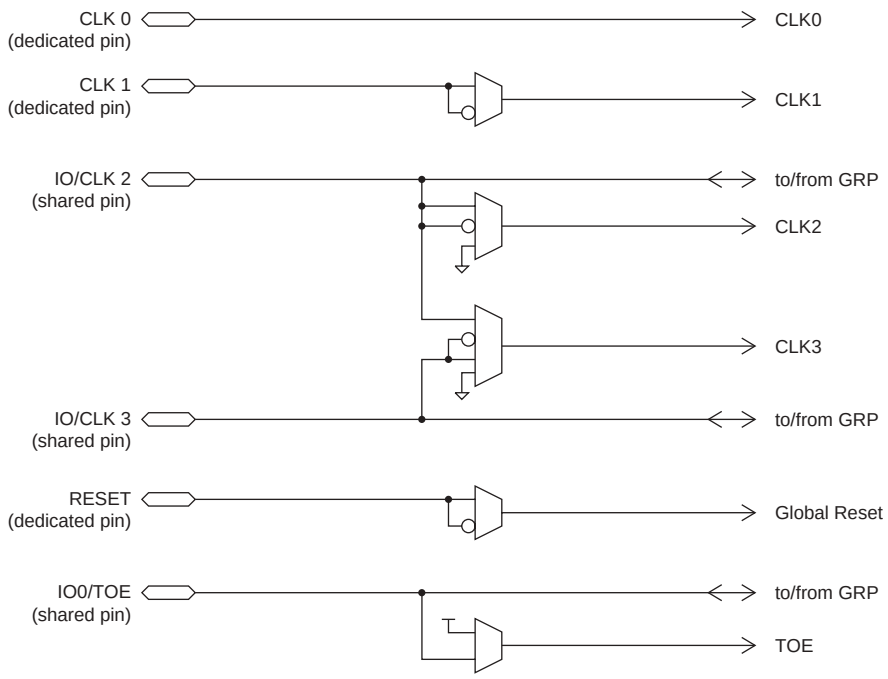


Figure 6. Boundary Scan Register Circuit for I/O Pins

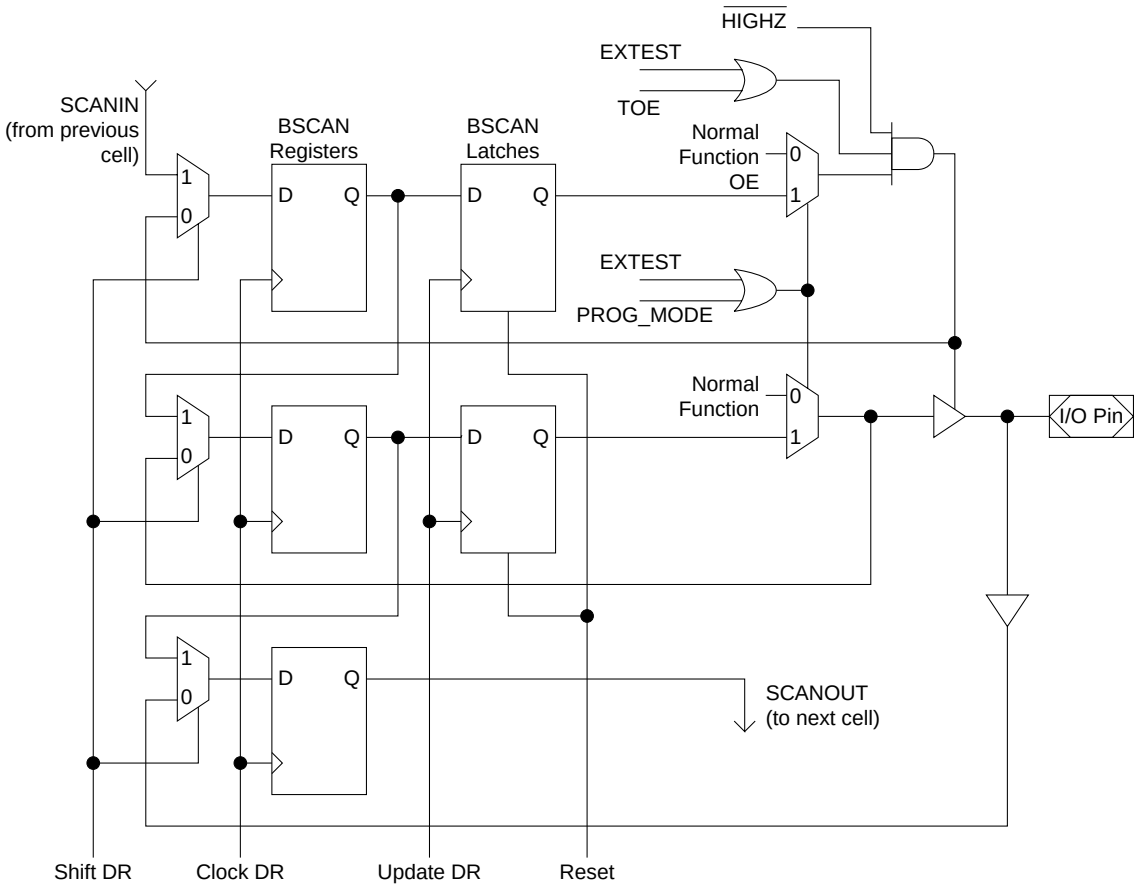


Figure 7. Boundary Scan Register Circuit for Input-Only Pins

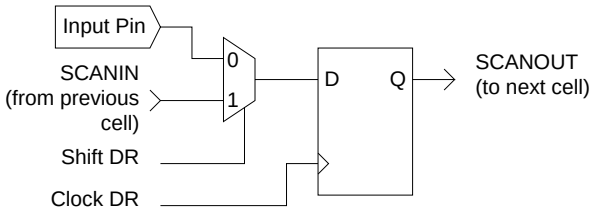
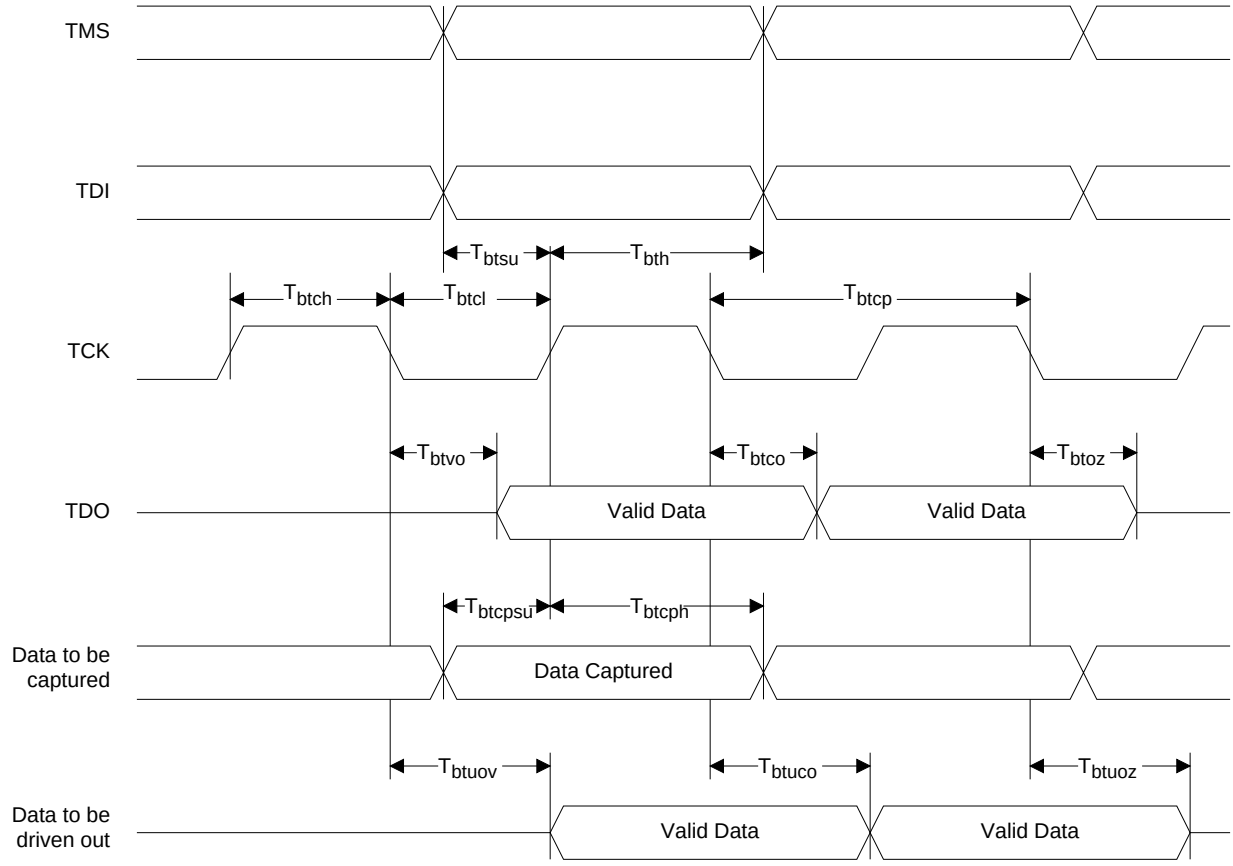


Figure 8. Boundary Scan Waveforms and Timing Specifications



SYMBOL	PARAMETER	MIN	MAX	UNITS
t_{btcp}	TCK [BSCAN test] clock pulse width	125	–	ns
t_{btch}	TCK [BSCAN test] pulse width high	62.5	–	ns
t_{btcl}	TCK [BSCAN test] pulse width low	62.5	–	ns
t_{btsu}	TCK [BSCAN test] setup time	25	–	ns
t_{bth}	TCK [BSCAN test] hold time	25	–	ns
t_{rf}	TCK [BSCAN test] rise and fall time	50	–	mV/ns
t_{btco}	TAP controller falling edge of clock to valid output	–	25	ns
t_{btoz}	TAP controller falling edge of clock to data output disable	–	25	ns
t_{btvo}	TAP controller falling edge of clock to data output enable	–	25	ns
t_{btcpsu}	BSCAN test Capture register setup time	25	–	ns
t_{btcph}	BSCAN test Capture register hold time	25	–	ns
t_{btuco}	BSCAN test Update reg, falling edge of clock to valid output	–	50	ns
t_{btuoz}	BSCAN test Update reg, falling edge of clock to output disable	–	50	ns
t_{btuov}	BSCAN test Update reg, falling edge of clock to output enable	–	50	ns

Absolute Maximum Ratings [1, 2]

Supply Voltage V_{CC} ..... -0.5 to +5.4V

Input Voltage Applied ..... -0.5 to +5.6V

Tri-Stated Output Voltage Applied ..... -0.5 to +5.6V

Storage Temperature ..... -65 to 150°C

Case Temp. with Power Applied ..... -55 to 125°C

Max. Junction Temp. (T_J) with Power Applied ... 150°C

1. Stresses above those listed under the "Absolute Maximum Ratings" may cause permanent damage to the device. Functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied (while programming, follow the programming specifications).
2. Compliance with the Thermal Management section of the Lattice Semiconductor Data Book or CD-ROM is a requirement.

DC Recommended Operating Condition

SYMBOL	PARAMETER			MIN.	MAX.	UNITS
V_{CC}	Supply Voltage	Commercial	T_A = 0°C to +70°C	3.00	3.60	V
		Industrial	T_A = -40°C to +85°C	3.00	3.60	V
V_{CCIO}	I/O Reference Voltage			2.3	3.60	V

Table 2-0005/5KVE

Capacitance (T_A=25°C,f=1.0 MHz)

SYMBOL	PARAMETER	TYPICAL	UNITS	TEST CONDITIONS
C_1	I/O Capacitance	10	pf	V_{CC} = 3.3V, $V_{I/O}$ = 0.0V
C_2	Clock Capacitance	10	pf	V_{CC} = 3.3V, V_{CK} = 0.0V
C_3	Global Input Capacitance	10	pf	V_{CC} = 3.3V, V_G = 0.0V

Table 2-0006/5KVE

Erase Reprogram Specification

PARAMETER	MINIMUM	MAXIMUM	UNITS
ispLSI Erase/Reprogram Cycles	10000	–	Cycles

Table 2-0008/5KVE

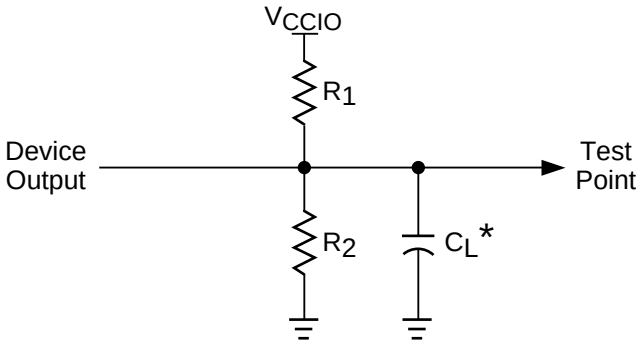
Switching Test Conditions

Input Pulse Levels	GND to $V_{CCIO_{min}}$
Input Rise and Fall Time	≤ 1.5ns 10% to 90%
Input Timing Reference Levels	1.5V
Ouput Timing Reference Levels	1.5V
Output Load	See Figure 9

Table 2-0003/5KVE

3-state levels are measured 0.5V from steady-state active level.

Figure 9. Test Load



*C_L includes Test Fixture and Probe Capacitance.

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Output Load Conditions (See Figure 9)

TEST CONDITION		3.3V R1	3.3V R2	2.5V R1	2.5V R2	CL
A		316Ω	348Ω	511Ω	475Ω	35pF
B	Active High	∞	348Ω	∞	475Ω	35pF
	Active Low	316Ω	∞	511Ω	∞	35pF
C	Active High to Z at V_{OH}-0.5V	∞	348Ω	∞	475Ω	5pF
	Active Low to Z at V_{OL}+0.5V	316Ω	∞	511Ω	∞	5pF
D	Slow Slew	∞	∞	∞	∞	35pF

Table 2-0004A/5KVE

DC Electrical Characteristics for 3.3V Range[1]

Over Recommended Operating Conditions

SYMBOL	PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNITS
V_{CCIO}	I/O Reference Voltage		3.0	–	3.6	V
V_{IL}	Input Low Voltage		-0.3	–	0.8	V
V_{IH}	Input High Voltage		2.0	–	5.25	V
V_{OL}	Output Low Voltage	$V_{CCIO = min}$, I_{OL} = 8 mA	–	–	0.4	V
V_{OH}	Output High Voltage	$V_{CCIO = min}$, I_{OH} = -4 mA	2.4	–	–	V

Table 2-0007/5KVE

1. I/O voltage configuration must be set to VCC.

DC Electrical Characteristics for 2.5V Range[1]

Over Recommended Operating Conditions

SYMBOL	PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNITS
V_{CCIO}	I/O Reference Voltage		2.3	–	2.7	V
V_{IL}	Input Low Voltage		-0.3	–	0.7	V
V_{IH}	Input High Voltage		1.7	–	5.25	V
V_{OL}	Output Low Voltage	$V_{CCIO=min}$, I_{OL}= 100μA	–	–	0.2	V
		$V_{CCIO=min}$, I_{OL}= 2mA	–	–	0.6	V
V_{OH}	Output High Voltage	$V_{CCIO=min}$, I_{OH}= -100μA	2.1	–	–	V
		$V_{CCIO=min}$, I_{OH}= -2mA	1.8	–	–	V

1. I/O voltage configuration must be set to VCCIO.

2.5V/5KVE

DC Electrical Characteristics

Over Recommended Operating Conditions

SYMBOL	PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNITS
I_{IL}	Input or I/O Low Leakage Current	$0V \le V_{IN} \le V_{IL}$(Max.)	–	–	-10	μA
I_{IH}	Input or I/O High Leakage Current	$(V_{CCIO}-0.2)V \le V_{IN} \le V_{CCIO}$	–	–	10	μA
		$V_{CCIO} \le V_{IN} \le 5.25V$	–	–	50	μA
I_{PU}[1]	I/O Active Pullup Current	$0V \le V_{IN} \le V_{IL}$	–	–	-200	μA
I_{BHL}	Bus Hold Low Sustaining Current	$V_{IN} = V_{IL(max)}$	40	–	–	μA
I_{BHH}	Bus Hold High Sustaining Current	$V_{IN} = V_{IH(min)}$	-40	–	–	μA
I_{BHLO}	Bus Hold Low Overdrive Current	$0V \le V_{IN} \le V_{CCIO}$	–	–	550	μA
I_{BHLH}	Bus Hold High Overdrive Current	$0V \le V_{IN} \le V_{CCIO}$	–	–	-550	μA
I_{BHT}	Bus Hold Trip Points		V_{IL}	–	V_{IH}	V
I_{VCCIO}	Current Needed for V_{CCIO} Pin	All I/Os Pulled-up, (Total I/Os * I_{PUmax})	–	–	30	mA

1. Pullup is capable of pulling to a minimum voltage of V_{OH} under no-load conditions.

DC Char_5KVE

External Switching Characteristics

Over Recommended Operating Conditions

PARAM.	TEST[3] COND.	DESCRIPTION [4,5]	-165		-125		UNITS
			MIN.	MAX.	MIN.	MAX.	
tpd1[6]	A	Data Prop. Delay, 5PT Bypass	—	6.0	—	7.5	ns
tpd2[6]	A	Data Propagation Delay	—	7.5	—	9.5	ns
fmax	A	Clock Frequency with Internal Feedback[1]	165	—	125	—	MHz
fmax (Ext.)	—	Clock Freq. with Ext. Feedback,1/(tsu2 + tco1)	118	—	87	—	MHz
fmax (Tog.)	—	Clock Frequency, Max Toggle[2]	200	—	167	—	MHz
tsu1	—	GLB Reg. Setup Time before Clk, 5PT bypass	4.0	—	5.0	—	ns
tco1[6]	A	GLB Reg. Clock to Output Delay	—	3.0	—	4.5	ns
th1	—	GLB Reg. Hold Time after Clock, 5PT bypass	0.0	—	0.0	—	ns
tsu2	—	GLB Reg. Setup Time before Clock	5.5	—	7.0	—	ns
th2	—	GLB Reg. Hold Time after Clock	0.0	—	0.0	—	ns
tsu3	—	GLB Reg. Setup Time before Clock, Input Reg. Path	2.5	—	3.5	—	ns
th3	—	GLB Reg. Hold Time after Clock, Input Reg. Path	0.5	—	0.5	—	ns
tr1	A	Ext. Reset Pin to Output Delay	—	8.0	—	10.0	ns
trw1[7]	—	Ext. Reset Pulse Duration	4.0	—	5.0	—	ns
tpten/dis[6]	B/C	Local Product Term Output Enable/Disable	—	7.0	—	8.5	ns
tgpten/dis[6]	B/C	Global Product Term Output Enable/Disable	—	12.0	—	14.0	ns
tgen/dis[6]	B/C	Global OE Input to Output Enable/Disable	—	4.5	—	5.5	ns
tten/dis[6]	B/C	Test OE Input to Output Enable/Disable	—	7.5	—	10.5	ns
twh	—	Ext. Sync. Clock Pulse Duration, High	2.5	—	3.0	—	ns
twl	—	Ext. Sync. Clock Pulse Duration, Low	2.5	—	3.0	—	ns

1. Standard 16-bit counter using GRP feedback.

Timing Ext.5256ve1.eps

2. fmax (Toggle) may be less than 1/(twh + twl). This is to allow for a clock duty cycle of other than 50%.

Timing v.2.0

3. Reference Switching Test Conditions section.
4. Unless noted otherwise, all timing numbers are taken with worst case PTSA fanout, a GRP load of 1 GLB, CLK0, and high-speed AND array.
5. Timing parameters measured using normal active output driver.
6. The delay parameters are measured with Vcc as I/O voltage reference. An additional 0.5ns delay is incurred when Vccio is used as I/O voltage reference.
7. Pulse widths less than minimum may cause unknown output behavior.

External Switching Characteristics

Over Recommended Operating Conditions

PARAM.	TEST[3] COND.	DESCRIPTION [4,5]	-100		-80		UNITS
			MIN.	MAX.	MIN.	MAX.	
tpd1[6]	A	Data Prop. Delay, 5PT Bypass	—	10.0	—	12.0	ns
tpd2[6]	A	Data Propagation Delay	—	12.0	—	15.0	ns
fmax	A	Clock Frequency with Internal Feedback[1]	100	—	80	—	MHz
fmax (Ext.)	—	Clock Freq. with Ext. Feedback,1/(tsu2 + tco1)	67	—	56	—	MHz
fmax (Tog.)	—	Clock Frequency, Max Toggle[2]	125	—	100	—	MHz
tsu1	—	GLB Reg. Setup Time before Clk, 5PT bypass	7.0	—	8.0	—	ns
tco1[6]	A	GLB Reg. Clock to Output Delay	—	6.0	—	7.0	ns
th1	—	GLB Reg. Hold Time after Clock, 5PT bypass	0.0	—	0.0	—	ns
tsu2	—	GLB Reg. Setup Time before Clock	9.0	—	11.0	—	ns
th2	—	GLB Reg. Hold Time after Clock	0.0	—	0.0	—	ns
tsu3	—	GLB Reg. Setup Time before Clock, Input Reg. Path	4.5	—	5.5	—	ns
th3	—	GLB Reg. Hold Time after Clock, Input Reg. Path	1.0	—	1.0	—	ns
tr1	A	Ext. Reset Pin to Output Delay	—	11.5	—	13.0	ns
trw1[7]	—	Ext. Reset Pulse Duration	6.5	—	8.0	—	ns
tpten/dis[6]	B/C	Local Product Term Output Enable/Disable	—	10.0	—	12.0	ns
tgpten/dis[6]	B/C	Global Product Term Output Enable/Disable	—	15.5	—	17.0	ns
tgen/dis[6]	B/C	Global OE Input to Output Enable/Disable	—	7.5	—	9.0	ns
tten/dis[6]	B/C	Test OE Input to Output Enable/Disable	—	11.5	—	12.5	ns
twh	—	Ext. Sync. Clock Pulse Duration, High	4.0	—	5.0	—	ns
twl	—	Ext. Sync. Clock Pulse Duration, Low	4.0	—	5.0	—	ns

1. Standard 16-bit counter using GRP feedback.

Timing Ext.5256ve2.eps

2. fmax (Toggle) may be less than 1/(twh + twl). This is to allow for a clock duty cycle of other than 50%.

Timing v.2.0

3. Reference Switching Test Conditions section.
4. Unless noted otherwise, all timing numbers are taken with worst case PTSA fanout, a GRP load of 1 GLB, CLK0, and high-speed AND array.
5. Timing parameters measured using normal active output driver.
6. The delay parameters are measured with Vcc as I/O voltage reference. An additional 0.5ns delay is incurred when Vccio is used as I/O reference.
7. Pulse widths less than minimum may cause unknown output behavior.
   used as I/O voltage reference.

Internal Timing Parameters

Over Recommended Operating Conditions

PARAMETER	DESCRIPTION	-165		-125		-100		-80		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
In/Out Delays										
tin	Input Buffer Delay	–	0.6	–	1.3	–	2.3	–	2.3	ns
tgclk_in	Global Clock Buffer Input Delay (clk0)	–	0.7	–	1.3	–	1.8	–	1.8	ns
trst	Global Reset Pin Delay	–	4.9	–	6.6	–	7.1	–	7.1	ns
tgoe	Global OE Pin Delay	–	3.2	–	3.9	–	5.9	–	7.4	ns
tbuf	Output Buffer Delay	–	1.9	–	2.2	–	2.7	–	3.7	ns
ten	Output Enable Delay	–	1.3	–	1.6	–	1.6	–	1.6	ns
tdis	Output Disable Delay	–	1.3	–	1.6	–	1.6	–	1.6	ns
Routing/GLB Delays										
troute	GRP and Logic Delay	–	3.2	–	3.6	–	4.0	–	4.5	ns
tpdb	5-pt Bypass Propagation Delay	–	0.3	–	0.4	–	1.0	–	1.5	ns
tpdi	Combinatorial Propagation Delay	–	0.0	–	0.0	–	0.0	–	0.0	ns
tptsa	Product Term Sharing Array	–	1.8	–	2.4	–	3.0	–	4.5	ns
tfbk	Internal Feedback Delay	–	0.0	–	0.0	–	0.0	–	0.5	ns
tinreg	Input Buffer to Macrocell Register Delay	–	2.0	–	2.5	–	2.5	–	3.5	ns
Register/Latch Delays										
ts	Register Setup Time	0.6	–	1.0	–	1.5	–	1.5	–	ns
ts_pt	Register Setup Time (Product Term Clock)	0.6	–	1.0	–	1.5	–	1.5	–	ns
th	Register Hold Time	2.4	–	3.0	–	4.0	–	5.0	–	ns
tcoi	Register Clock to GLB Output Delay	–	0.4	–	1.0	–	1.5	–	1.5	ns
tsl	Latch Setup Time	0.6	–	1.0	–	1.5	–	1.5	–	ns
thl	Latch Hold Time	2.4	–	3.0	–	4.0	–	5.0	–	ns
tgoi	Latch Gate to GLB Output Delay	–	0.4	–	1.0	–	1.5	–	1.5	ns
tpdli	GLB Latch propagation Delay	–	1.0	–	1.5	–	2.0	–	2.5	ns
tces	Clock Enable Setup Time	4.1	–	4.3	–	5.3	–	6.3	–	ns
tceh	Clock Enable Hold Time	0.9	–	1.7	–	2.7	–	3.7	–	ns
tsri	Asynchronous Set/Reset to GLB Output Delay	–	1.2	–	1.2	–	1.7	–	2.2	ns
tsrr	Asynchronous Set/Reset Recovery Time	0.8	–	1.2	–	1.2	–	2.2	–	ns
Control Delays										
tptclk	Macrocell PT Clock Delay	–	0.4	–	0.4	–	0.5	–	0.5	ns
tbclk	Block PT Clock Delay	–	1.4	–	1.9	–	2.5	–	2.5	ns
tptsr	Macrocell PT Set/Reset Delay	–	2.1	–	3.7	–	4.8	–	4.8	ns
tbsr	Block PT Set/Reset Delay	–	3.1	–	5.7	–	6.8	–	6.8	ns
tptoe	Macrocell PT OE Delay	–	1.9	–	2.0	–	2.1	–	3.6	ns
tgptoe	Global PT OE Delay	–	6.9	–	7.5	–	7.6	–	8.6	ns

Note: Internal Timing Parameters are not tested and are for reference only. Refer to Timing Model in this data sheet for further details.

Timing v.2.0

ispLSI 5256VE Timing Parameters (continued)

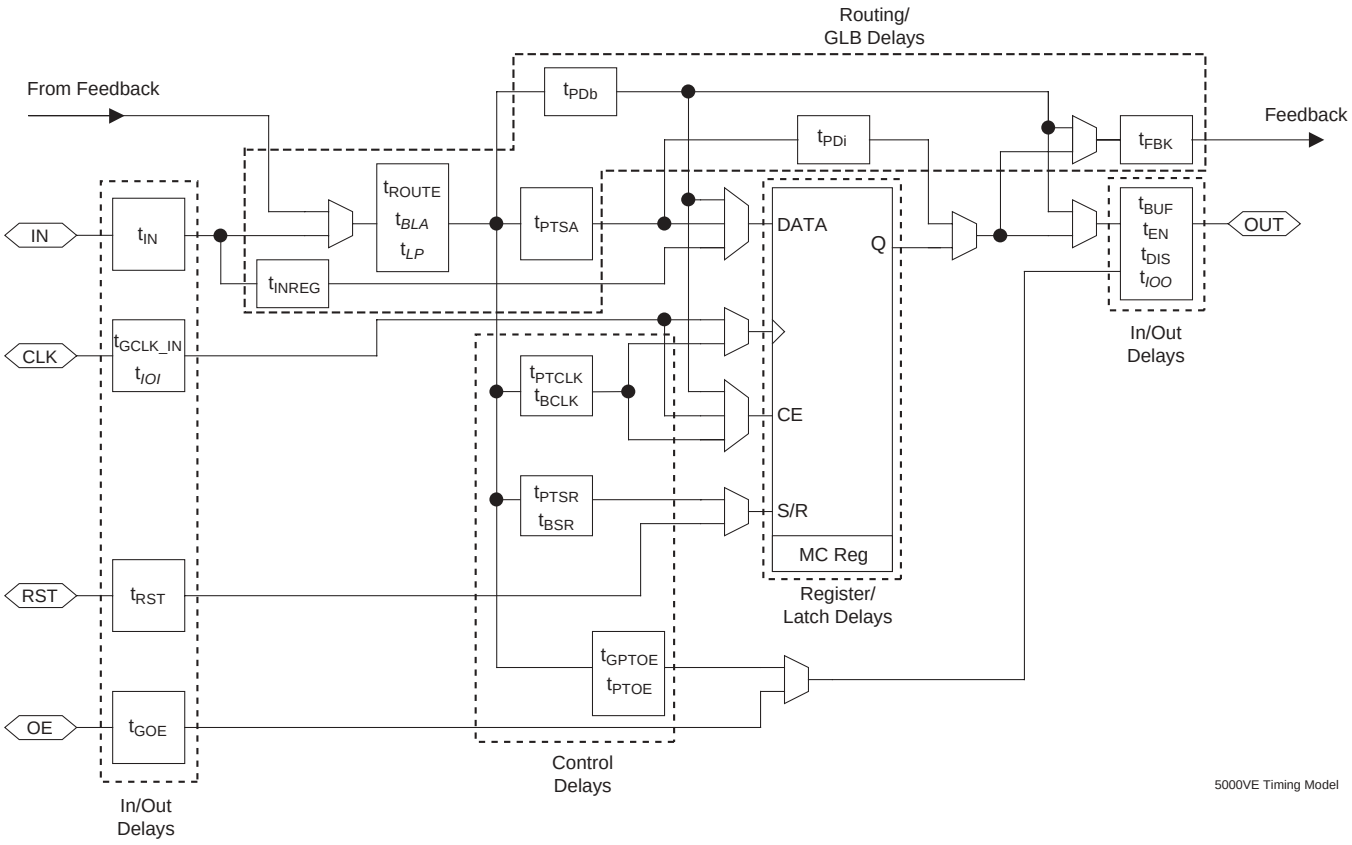
ADDER TYPE	BASE PARAMETER	ADDER				UNITS
		-165	-125	-100	-80	
Routing Adders						
tlp	**t**route	1.0	1.5	1.5	1.5	ns
Tioi Input Adders						
clk1	**t**gclk_in	1.4	1.7	1.7	1.7	ns
clk2	**t**gclk_in	1.4	1.7	1.7	1.7	ns
clk3	**t**gclk_in	1.4	1.7	1.7	1.7	ns
Tioo Output Adders[1]						
Slow Slew I/O	**t**buf, **t**en	4.0	4.0	4.0	4.0	ns
LVTTL_out	**t**buf, **t**en, **t**dis	0.0	0.0	0.0	0.0	ns
LVCMOS25_out	**t**buf, **t**en, **t**dis	0.5	0.5	0.5	0.5	ns
LVCMOS33_out	**t**buf, **t**en, **t**dis	0.0	0.0	0.0	0.0	ns
Tbla Additional Block Loading Adders						
1	**t**route	0.1	0.1	0.1	0.1	ns
2	**t**route	0.1	0.2	0.2	0.2	ns
3	**t**route	0.2	0.3	0.3	0.3	ns
4	**t**route	0.3	0.4	0.4	0.4	ns
5	**t**route	0.4	0.5	0.5	0.5	ns
6	**t**route	0.4	0.6	0.6	0.6	ns
7	**t**route	0.5	0.7	0.7	0.7	ns

[1]Timing for open drain configurations is the same as non-open drain configurations.

Timing Table/5256VE
Timing v.2.0

Note: Internal Timing Parameters are not tested and are for reference only. Refer to Timing Model in this data sheet for details.

ispLSI 5256VE Timing Model

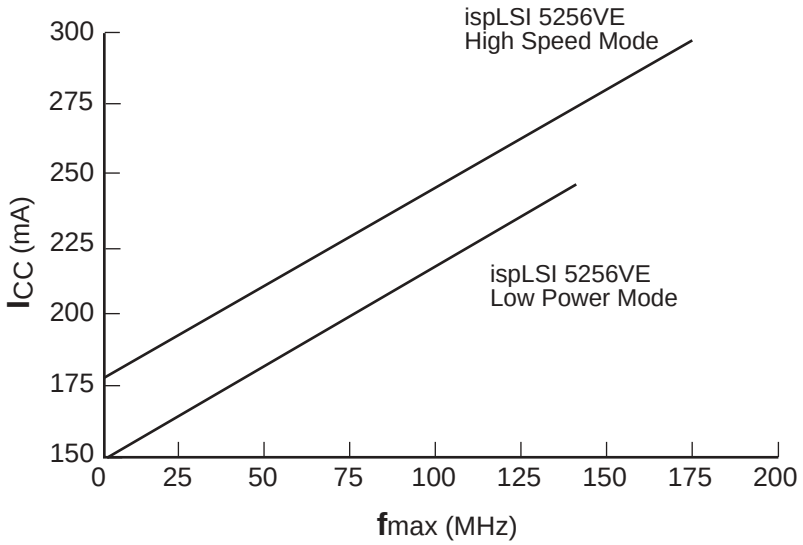


Note: Italicized parameters are delay adders above and beyond default conditions (i.e. GRP load of one GLB, CLK0, high-speed AND Array and VCC I/O option).

Power Consumption

Power consumption in the ispLSI 5256VE device depends on two primary factors: the speed at which the device is operating and the number of product terms used. The product terms have a fuse-selectable speed/power tradeoff setting. Each group of five product terms has a single speed/power tradeoff control fuse that acts on the complete group of five. The fast "high-speed" setting operates product terms at their normal full power consumption. For portions of the logic that can tolerate longer propagation delays, selecting the slower "low-power" setting will reduce the power dissipation for these product terms. Figure 10 shows the relationship between power and operating frequency.

Figure 10. Typical Device Power Consumption vs fmax



Notes: Configuration of 16 16-bit Counters
Typical Current at 3.3V, 25° C

I_{CC} can be estimated for the ispLSI 5256VE using the following equation:

High Speed Mode: ICC = 21 + (# of PTs * 0.313) + (# of nets * Fmax * 0.00282)
Low Power Mode: ICC = 21 + (# of PTs * 0.258) + (# of nets * Fmax * 0.00282)
# of PTs = Number of Product Terms used in design
# of nets = Number of Signals used in device
Fmax = Highest Clock Frequency to the device

The I_{CC} estimate is based on typical conditions (V_{CC} = 3.3V, room temperature) and an assumption of one GLB load on average exists. These values are for estimates only. Since the value of I_{CC} is sensitive to operating conditions and the program in the device, the actual I_{CC} should be verified.

0127/5256VE

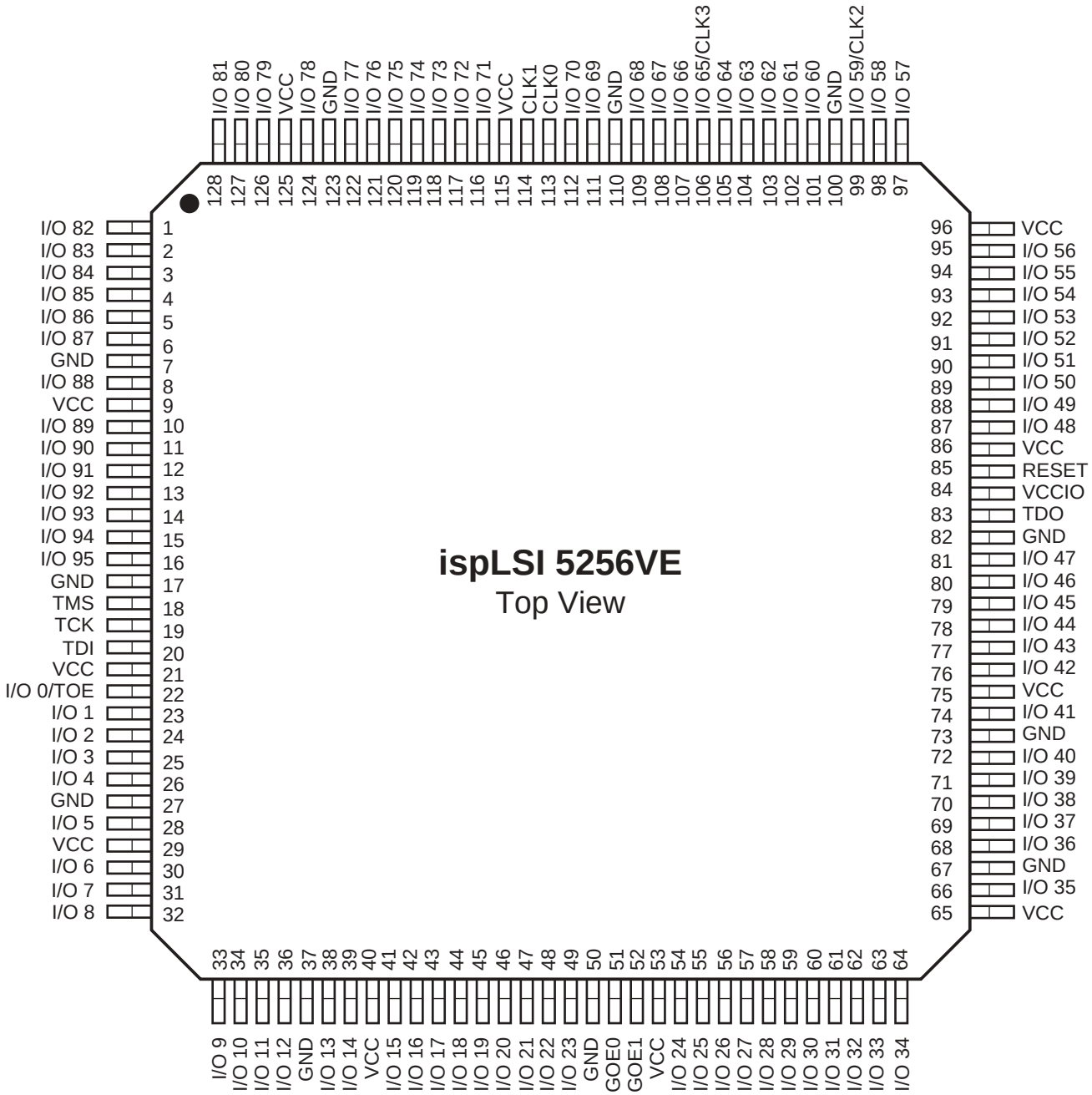
Signal Descriptions

Signal Name	Description
TMS	Input - This pin is the Test Mode Select input, which is used to control the JTAG state machine.
TCK	Input - This pin is the Test Clock input pin used to clock through the JTAG state machine.
TDI	Input - This pin is the JTAG Test Data In pin used to load data.
TDO	Output - This pin is the JTAG Test Data Out pin used to shift data out.
TOE / I/O0	Input/Output - This pin functions as either the Test Output Enable pin or an I/O pin based upon customer's design. TOE tristates all I/O pins when a logic low is driven.
GOE0, GOE1	Input - These two pins are the Global Output Enable input pins.
RESET	Dedicated Reset Input - This pin resets all registers in the device. The global polarity (active high or low input) for this pin is selectable.
I/O	Input/Output – These are the general purpose I/O used by the logic array.
GND	Ground
NC[1]	No connect.
VCC	Vcc
CLK0, CLK1	Dedicated clock inputs for all registers. Both clocks are muxed before being used as the clock input to all registers in the device.
CLK2 / I/O, CLK3 / I/O	Input/Output - These pins share functionality. They can be used as dedicated clock inputs for all registers, as well as I/O pins.
VCCIO	Input - This pin is used for optional 2.5V outputs. Every I/O can independently select either 3.3V or the optional voltage as its output level. If the optional output voltage is not required, this pin must be connected to the Vcc supply. Programmable pull-up resistors and bus-hold latches only draw current from this supply.

1. NC pins are not to be connected to any active signals, VCC or GND.

Pin Configuration

ispLSI 5256VE 128-Pin TQFP (0.4mm Lead Pitch / 14.0mm x 14.0mm Body Size)



128 TQFP/5256VE

Signal Configuration

ispLSI 5256VE 256-Ball fpBGA (1.0mm Ball Pitch / 17.0mm x 17.0mm Body Size)

	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	
A	I/O 113	I/O 116	I/O 121	I/O 125	I/O 126	I/O 131/ CLK3	I/O 133	I/O 139	I/O 140	CLK0	I/O 145	I/O 147	I/O 151	I/O 152	I/O 153	I/O 165	A
B	I/O 108	I/O 115	I/O 117	I/O 119/ CLK2	I/O 124	I/O 129	I/O 132	I/O 136	CLK1	I/O 144	I/O 149	I/O 156	I/O 157	I/O 163	I/O 164	I/O 168	B
C	I/O 106	I/O 114	NC[1]	I/O 120	I/O 123	I/O 128	I/O 135	I/O 138	I/O 141	I/O 143	I/O 148	I/O 155	I/O 159	I/O 160	I/O 161	I/O 172	C
D	I/O 105	I/O 109	I/O 111	GND	GND	VCC	GND	VCC	GND	GND	VCC	GND	VCC	I/O 169	I/O 167	I/O 175	D
E	I/O 104	NC[1]	I/O 101	VCC	NC[1]	NC[1]	NC[1]	NC[1]	NC[1]	NC[1]	NC[1]	NC[1]	GND	I/O 173	I/O 171	I/O 177	E
F	I/O 100	I/O 102	I/O 97	GND	NC[1]	NC[1]	NC[1]	NC[1]	NC[1]	NC[1]	NC[1]	NC[1]	VCC	I/O 181	I/O 176	I/O 179	F
G	I/O 96	I/O 98	TDO	VCC	NC[1]	NC[1]	VCC	GND	GND	VCC	NC[1]	NC[1]	GND	I/O 185	I/O 180	I/O 187	G
H	I/O 94	VCCIO	RESET	GND	NC[1]	NC[1]	GND	VCC	VCC	GND	NC[1]	NC[1]	VCC	I/O 184	I/O 183	I/O 188	H
J	I/O 93	I/O 92	I/O 90	GND	NC[1]	NC[1]	GND	VCC	VCC	GND	NC[1]	NC[1]	GND	I/O 191	I/O 190	TMS	J
K	I/O 89	I/O 88	I/O 86	VCC	NC[1]	NC[1]	VCC	GND	GND	VCC	NC[1]	NC[1]	VCC	TDI	TCK	I/O 0/ TOE	K
L	I/O 85	I/O 84	I/O 82	GND	NC[1]	NC[1]	NC[1]	NC[1]	NC[1]	NC[1]	NC[1]	NC[1]	GND	I/O 4	I/O 1	I/O 2	L
M	I/O 81	I/O 80	I/O 77	GND	NC[1]	NC[1]	NC[1]	NC[1]	NC[1]	NC[1]	NC[1]	NC[1]	VCC	I/O 8	I/O 6	I/O 5	M
N	I/O 78	I/O 74	I/O 76	VCC	GND	VCC	GND	VCC	GND	GND	VCC	GND	GND	I/O 11	I/O 12	I/O 9	N
P	I/O 73	I/O 70	I/O 65	I/O 66	I/O 57	I/O 56	GOE1	GOE0	I/O 41	I/O 42	I/O 36	I/O 26	I/O 22	I/O 20	I/O 13	I/O 14	P
R	I/O 72	I/O 69	I/O 62	I/O 67	I/O 64	I/O 58	I/O 48	I/O 46	I/O 40	I/O 34	I/O 29	I/O 25	I/O 24	I/O 18	I/O 17	I/O 16	R
T	I/O 61	I/O 60	I/O 54	I/O 53	I/O 52	I/O 50	I/O 49	I/O 45	I/O 44	I/O 38	I/O 37	I/O 33	I/O 32	I/O 30	I/O 28	I/O 21	T
	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	

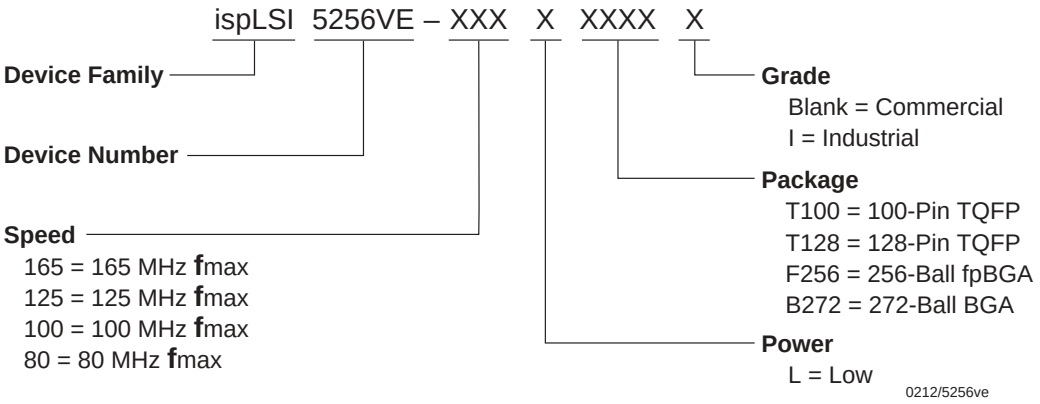
ispLSI 5256VE

Bottom View

1. NCs are not to be connected to any active signals, VCC or GND.

Note: Ball A1 indicator dot on top side of package.

Part Number Description



Ordering Information

COMMERCIAL

FAMILY	fmax (MHz)	tpd (ns)	ORDERING NUMBER	PACKAGE
ispLSI	165	6.0	ispLSI 5256VE-165LT100	100-Pin TQFP
	165	6.0	ispLSI 5256VE-165LT128	128-Pin TQFP
	165	6.0	ispLSI 5256VE-165LF256	256-Ball fpBGA
	165	6.0	ispLSI 5256VE-165LB272	272-Ball BGA
	125	7.5	ispLSI 5256VE-125LT100	100-Pin TQFP
	125	7.5	ispLSI 5256VE-125LT128	128-Pin TQFP
	125	7.5	ispLSI 5256VE-125LF256	256-Ball fpBGA
	125	7.5	ispLSI 5256VE-125LB272	272-Ball BGA
	100	10	ispLSI 5256VE-100LT100	100-Pin TQFP
	100	10	ispLSI 5256VE-100LT128	128-Pin TQFP
	100	10	ispLSI 5256VE-100LF256	256-Ball fpBGA
	100	10	ispLSI 5256VE-100LB272	272-Ball BGA

Table 2-0041A/5256VE

INDUSTRIAL

FAMILY	fmax (MHz)	tpd (ns)	ORDERING NUMBER	PACKAGE
ispLSI	125	7.5	ispLSI 5256VE-125LT100I	100-Pin TQFP
	125	7.5	ispLSI 5256VE-125LT128I	128-Pin TQFP
	125	7.5	ispLSI 5256VE-125LF256I	256-Ball fpBGA
	125	7.5	ispLSI 5256VE-125LB272I	272-Ball BGA
	100	10	ispLSI 5256VE-100LT100I	100-Pin TQFP
	100	10	ispLSI 5256VE-100LT128I	128-Pin TQFP
	100	10	ispLSI 5256VE-100LF256I	256-Ball fpBGA
	100	10	ispLSI 5256VE-100LB272I	272-Ball BGA
	80	12	ispLSI 5256VE-80LT100I	100-Pin TQFP
	80	12	ispLSI 5256VE-80LT128I	128-Pin TQFP
	80	12	ispLSI 5256VE-80LF256I	256-Ball fpBGA
	80	12	ispLSI 5256VE-80LB272I	272-Ball BGA

The ispLSI 5256VE is dual-marked with both Commercial and Industrial grades. The Commercial speed grade is faster (i.e. ispLSI 5256VE-165LF256) than the Industrial speed grade (i.e. ispLSI 5256VE-125LF256I).

Table 2-0041B/5256VE