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## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Active |
| Core Processor | ARM® Cortex®-M0 |
| Core Size | 32-Bit Single-Core |
| Speed | 48MHz |
| Connectivity | CANbus, I²C, IrDA, LINbus, SPI, UART/USART |
| Peripherals | DMA, I²S, POR, PWM, WDT |
| Number of I/O | 37 |
| Program Memory Size | 256KB (256K x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | - |
| RAM Size | 32K x 8 |
| Voltage - Supply (Vcc/Vdd) | 1.65V ~ 3.6V |
| Data Converters | A/D 13x12b; D/A 2x12b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 85°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 48-LQFP |
| Supplier Device Package | 48-LQFP (7x7) |
| Purchase URL | https://www.e-xfl.com/product-detail/stmicroelectronics/stm32f098cct6 |

Table 9. STM32F098CC/RC/VC USART implementation (continued)

| USART modes/features(1) | USART1 USART2 USART3 | USART4 | USART5 USART6 USART7 USART8 |
|---|---|---|---|
| Single-wire half-duplex communication | X | X | X |
| IrDA SIR ENDEC block | X | - | - |
| LIN mode | X | - | - |
| Dual clock domain and wakeup from Stop mode | X | - | - |
| Receiver timeout interrupt | X | - | - |
| Modbus communication | X | - | - |
| Auto baud rate detection | X | - | - |
| Driver Enable | X | X | X |

1. X = supported.

## 3.18 Serial peripheral interface (SPI) / Inter-integrated sound interface ($I^2S$)

Two SPIs are able to communicate up to 18 Mbit/s in slave and master modes in full-duplex and half-duplex communication modes. The 3-bit prescaler gives 8 master mode frequencies and the frame size is configurable from 4 bits to 16 bits.

Two standard $I^2S$ interfaces (multiplexed with SPI1 and SPI2 respectively) supporting four different audio standards can operate as master or slave at half-duplex communication mode. They can be configured to transfer 16 and 24 or 32 bits with 16-bit or 32-bit data resolution and synchronized by a specific signal. Audio sampling frequency from 8 kHz up to 192 kHz can be set by an 8-bit programmable linear prescaler. When operating in master mode, they can output a clock for an external audio component at 256 times the sampling frequency.

Table 10. STM32F098CC/RC/VC SPI/$I^2S$ implementation

| SPI features(1) | SPI1 and SPI2 |
|---|---|
| Hardware CRC calculation | X |
| Rx/Tx FIFO | X |
| NSS pulse mode | X |
| $I^2S$ mode | X |
| TI mode | X |

1. X = supported.

**Table 11. Legend/abbreviations used in the pinout table (continued)**

| Name | | Abbreviation | Definition |
|---|---|---|---|
| Pin functions | Alternate functions | Functions selected through GPIOx_AFR registers | |
| | Additional functions | Functions directly selected/enabled through peripheral registers | |

**Table 12. STM32F098CC/RC/VC pin definitions**

| Pin numbers | | | | | | Pin name (function upon reset) | Pin type | I/O structure | Notes | Pin functions | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| UFBGA100 | LQFP100 | UFBGA64 | LQFP64 | WLCSP64 | LQFP48/UFQFPN48 | | | | | Alternate functions | Additional functions |
| B2 | 1 | - | - | - | - | PE2 | I/O | FT | | TSC_G7_IO1, TIM3_ETR | - |
| A1 | 2 | - | - | - | - | PE3 | I/O | FT | | TSC_G7_IO2, TIM3_CH1 | - |
| B1 | 3 | - | - | - | - | PE4 | I/O | FT | | TSC_G7_IO3, TIM3_CH2 | - |
| C2 | 4 | - | - | - | - | PE5 | I/O | FT | | TSC_G7_IO4, TIM3_CH3 | - |
| D2 | 5 | - | - | - | - | PE6 | I/O | FT | | TIM3_CH4 | WKUP3, RTC_TAMP3 |
| E2 | 6 | B2 | 1 | B8 | 1 | VBAT | S | - | - | Backup power supply | |
| C1 | 7 | A2 | 2 | B7 | 2 | PC13 | I/O | TC | (1) (2) | - | WKUP2, RTC_TAMP1, RTC_TS, RTC_OUT |
| D1 | 8 | A1 | 3 | C8 | 3 | PC14-OSC32_IN (PC14) | I/O | TC | (1) (2) | - | OSC32_IN |
| E1 | 9 | B1 | 4 | C7 | 4 | PC15-OSC32_OUT (PC15) | I/O | TC | (1) (2) | - | OSC32_OUT |
| F2 | 10 | - | - | - | - | PF9 | I/O | FT | | TIM15_CH1, USART6_TX | - |
| G2 | 11 | - | - | - | - | PF10 | I/O | FT | | TIM15_CH2, USART6_RX | - |
| F1 | 12 | C1 | 5 | D8 | 5 | PF0-OSC_IN (PF0) | I/O | FTf | | CRS_ SYNC, I2C1_SDA | OSC_IN |
| G1 | 13 | D1 | 6 | E8 | 6 | PF1-OSC_OUT (PF1) | I/O | FTf | | I2C1_SCL | OSC_OUT |
| H2 | 14 | E1 | 7 | D7 | 7 | NRST | I/O | RST | | Device reset input / internal reset output (active low) | |

Table 12. STM32F098CC/RC/VC pin definitions (continued)

| Pin numbers | | | | | | Pin name (function upon reset) | Pin type | I/O structure | Notes | Pin functions | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| UFBGA100 | LQFP100 | UFBGA64 | LQFP64 | WLCSP64 | LQFP48/UFQFPN48 | | | | | Alternate functions | Additional functions |
| B7 | 85 | - | - | - | - | PD4 | I/O | FT | | SPI2_MOSI, I2S2_SD, USART2_RTS | - |
| A6 | 86 | - | - | - | - | PD5 | I/O | FT | | USART2_TX | - |
| B6 | 87 | - | - | - | - | PD6 | I/O | FT | | USART2_RX | - |
| A5 | 88 | - | - | - | - | PD7 | I/O | FT | | USART2_CK | - |
| A8 | 89 | A5 | 55 | D4 | 39 | PB3 | I/O | FT | | SPI1_SCK, I2S1_CK, TIM2_CH2, TSC_G5_IO1, EVENTOUT, USART5_TX | - |
| A7 | 90 | A4 | 56 | D5 | 40 | PB4 | I/O | FT | | SPI1_MISO, I2S1_MCK, TIM17_BKIN, TIM3_CH1, TSC_G5_IO2, EVENTOUT, USART5_RX | - |
| C5 | 91 | C4 | 57 | C5 | 41 | PB5 | I/O | FT | | SPI1_MOSI, I2S1_SD, I2C1_SMBA, TIM16_BKIN, TIM3_CH2, USART5_CK_RTS | WKUP6 |
| B5 | 92 | D3 | 58 | A5 | 42 | PB6 | I/O | FTf | | I2C1_SCL, USART1_TX, TIM16_CH1N, TSC_G5_I03 | - |
| B4 | 93 | C3 | 59 | B5 | 43 | PB7 | I/O | FTf | | I2C1_SDA, USART1_RX, USART4_CTS, TIM17_CH1N, TSC_G5_IO4 | - |
| A4 | 94 | B4 | 60 | C6 | 44 | PF11-BOOT0 | I/O | FT | | - | Boot memory selection |
| A3 | 95 | B3 | 61 | A6 | 45 | PB8 | I/O | FTf | | I2C1_SCL, CEC, TIM16_CH1, TSC_SYNC, CAN_RX | - |
| B3 | 96 | A3 | 62 | B6 | 46 | PB9 | I/O | FTf | | SPI2_NSS, I2S2_WS, I2C1_SDA, IR_OUT, TIM17_CH1, EVENTOUT, CAN_TX | - |
| C3 | 97 | - | - | - | - | PE0 | I/O | FT | | EVENTOUT, TIM16_CH1 | - |
| A2 | 98 | - | - | - | - | PE1 | I/O | FT | | EVENTOUT, TIM17_CH1 | - |

1. Data based on characterization results, not tested in production unless otherwise specified.

**Table 27. Typical and maximum current consumption in Stop mode**

| Symbol | Parameter | Conditions | Typ @ $V_{DDA}$ ($V_{DD}$ = 1.8 V) | | | | | | | Max | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | = 1.8 V | = 2.0 V | = 2.4 V | = 2.7 V | = 3.0 V | = 3.3 V | = 3.6 V | $T_A$ = 25 °C | $T_A$ = 85 °C | $T_A$ = 105 °C | |
| $I_{DD}$ | Supply current in Stop mode | All oscillators OFF | 0.6 | | | | | | | 2.4 | 33 | 78 | µA |
| $I_{DDA}$ | | | 0.9 | 0.9 | 1.0 | 1.0 | 1.0 | 1.1 | 1.2 | 2.5 | 3.0 | 3.7 | |

**Table 28. Typical and maximum current consumption from the $V_{DDA}$ supply**

| Symbol | Para-meter | Conditions (1) | $f_{HCLK}$ | $V_{DDA}$ = 2.4 V | | | | $V_{DDA}$ = 3.6 V | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | Typ | Max @ $T_A$ (2) | | | Typ | Max @ $T_A$ (2) | | | |
| | | | | | 25 °C | 85 °C | 105 °C | | 25 °C | 85 °C | 105 °C | |
| $I_{DDA}$ | Supply current in Run or Sleep mode, code executing from Flash memory or RAM | HSI48 | 48 MHz | 311 | 332 | 337 | 346 | 315 | 333 | 340 | 349 | µA |
| | | HSE bypass, PLL on | 48 MHz | 146 | 167 | 177 | 180 | 159 | 180 | 191 | 196 | |
| | | | 32 MHz | 100 | 118 | 124 | 126 | 108 | 126 | 134 | 137 | |
| | | | 24 MHz | 79 | 95 | 98 | 99 | 85 | 100 | 105 | 108 | |
| | | HSE bypass, PLL off | 8 MHz | 2 | 3 | 3 | 4 | 3 | 3 | 4 | 4 | |
| | | | 1 MHz | 2 | 2 | 3 | 3 | 2 | 3 | 3 | 4 | |
| | | HSI clock, PLL on | 48 MHz | 212 | 242 | 253 | 257 | 234 | 261 | 274 | 280 | |
| | | | 32 MHz | 165 | 193 | 202 | 203 | 183 | 206 | 215 | 219 | |
| | | | 24 MHz | 143 | 170 | 176 | 177 | 160 | 179 | 186 | 189 | |
| | | HSI clock, PLL off | 8 MHz | 64 | 82 | 84 | 85 | 76 | 88 | 91 | 92 | |

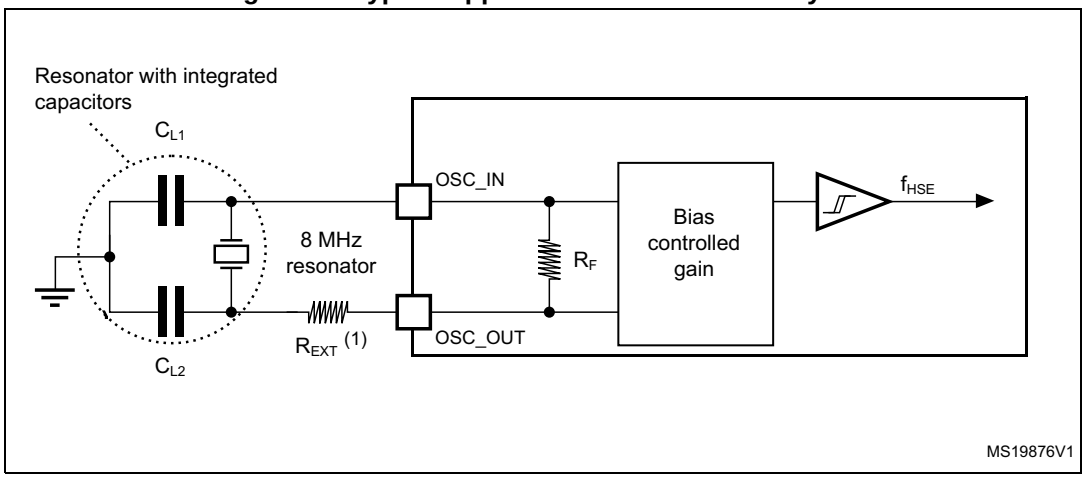
1. Current consumption from the $V_{DDA}$ supply is independent of whether the digital peripherals are enabled or disabled, being in Run or Sleep mode or executing from Flash memory or RAM. Furthermore, when the PLL is off, $I_{DDA}$ is independent from the frequency.
2. Data based on characterization results, not tested in production unless otherwise specified.

**Table 32. Peripheral current consumption (continued)**

| Peripheral | | Typical consumption at 25 °C | Unit |
|---|---|---|---|
| APB | APB-Bridge(2) | 3.6 | µA/MHz |
| | ADC(3) | 4.3 | |
| | CAN | 12.4 | |
| | CEC | 0.4 | |
| | CRS | 0.0 | |
| | DAC(3) | 4.2 | |
| | DBG (MCU Debug Support) | 0.2 | |
| | I2C1 | 2.9 | |
| | I2C2 | 2.4 | |
| | PWR | 0.6 | |
| | SPI1 | 8.8 | |
| | SPI2 | 7.8 | |
| | SYSCFG and COMP | 1.9 | |
| | TIM1 | 15.2 | |
| | TIM14 | 2.6 | |
| | TIM15 | 8.7 | |
| | TIM16 | 5.8 | |
| | TIM17 | 7.0 | |
| | TIM2 | 16.2 | |
| | TIM3 | 11.9 | |
| | TIM6 | 11.8 | |
| | TIM7 | 2.5 | |
| | USART1 | 17.6 | |
| | USART2 | 16.3 | |
| | USART3 | 16.2 | |
| | USART4 | 4.7 | |
| | USART5 | 4.4 | |
| | USART6 | 5.5 | |
| | USART7 | 5.2 | |
| | USART8 | 5.1 | |
| | WWDG | 1.1 | |
| | **All APB peripherals** | **207.2** | |

1. The BusMatrix is automatically active when at least one master is ON (CPU, DMA).
2. The APB Bridge is automatically active when at least one peripheral is ON on the Bus.
3. The power consumption of the analog part ($I_{DDA}$) of peripherals such as ADC, DAC, comparators, is not included. Refer to the tables of characteristics in the subsequent sections.

**Figure 17. Typical application with an 8 MHz crystal**




1. $R_{EXT}$ value depends on the crystal characteristics.

## Low-speed external clock generated from a crystal resonator

The low-speed external (LSE) clock can be supplied with a 32.768 kHz crystal resonator oscillator. All the information given in this paragraph are based on design simulation results obtained with typical external components specified in *Table 37*. In the application, the resonator and the load capacitors have to be placed as close as possible to the oscillator pins in order to minimize output distortion and startup stabilization time. Refer to the crystal resonator manufacturer for more details on the resonator characteristics (frequency, package, accuracy).

**Table 37. LSE oscillator characteristics ($f_{LSE}$ = 32.768 kHz)**

| Symbol | Parameter | Conditions(1) | Min(2) | Typ | Max(2) | Unit |
|---|---|---|---|---|---|---|
| $I_{DD}$ | LSE current consumption | low drive capability | - | 0.5 | 0.9 | µA |
| | | medium-low drive capability | - | - | 1 | |
| | | medium-high drive capability | - | - | 1.3 | |
| | | high drive capability | - | - | 1.6 | |
| $g_m$ | Oscillator transconductance | low drive capability | 5 | - | - | µA/V |
| | | medium-low drive capability | 8 | - | - | |
| | | medium-high drive capability | 15 | - | - | |
| | | high drive capability | 25 | - | - | |
| $t_{SU(LSE)}$(3) | Startup time | $V_{DDIOx}$ is stabilized | - | 2 | - | s |

1. Refer to the note and caution paragraphs below the table, and to the application note AN2867 “Oscillator design guide for ST microcontrollers”.
2. Guaranteed by design, not tested in production.
3. $t_{SU(LSE)}$ is the startup time measured from the moment it is enabled (by software) to a stabilized 32.768 kHz oscillation is reached. This value is measured for a standard crystal and it can vary significantly with the crystal manufacturer

**Table 44. Flash memory endurance and data retention**

| Symbol | Parameter | Conditions | Min(1) | Unit |
|---|---|---|---|---|
| $N_{END}$ | Endurance | $T_A$ = –40 to +105 °C | 10 | kcycle |
| $t_{RET}$ | Data retention | 1 kcycle(2) at $T_A$ = 85 °C | 30 | Year |
| | | 1 kcycle(2) at $T_A$ = 105 °C | 10 | |
| | | 10 kcycle(2) at $T_A$ = 55 °C | 20 | |

1. Data based on characterization results, not tested in production.
2. Cycling performed over the whole temperature range.

## 6.3.10 EMC characteristics

Susceptibility tests are performed on a sample basis during device characterization.

### Functional EMS (electromagnetic susceptibility)

While a simple application is executed on the device (toggling 2 LEDs through I/O ports). the device is stressed by two electromagnetic events until a failure occurs. The failure is indicated by the LEDs:

- **Electrostatic discharge (ESD)** (positive and negative) is applied to all device pins until a functional disturbance occurs. This test is compliant with the IEC 61000-4-2 standard.
- **FTB**: A Burst of Fast Transient voltage (positive and negative) is applied to $V_{DD}$ and $V_{SS}$ through a 100 pF capacitor, until a functional disturbance occurs. This test is compliant with the IEC 61000-4-4 standard.

A device reset allows normal operations to be resumed.

The test results are given in *Table 45*. They are based on the EMS levels and classes defined in application note AN1709.

**Table 45. EMS characteristics**

| Symbol | Parameter | Conditions | Level/ Class |
|---|---|---|---|
| $V_{FESD}$ | Voltage limits to be applied on any I/O pin to induce a functional disturbance | $V_{DD}$ = 1.8 V, LQFP100, $T_A$ = +25 °C, $f_{HCLK}$ = 48 MHz, conforming to IEC 61000-4-2 | 2B |
| $V_{EFTB}$ | Fast transient voltage burst limits to be applied through 100 pF on $V_{DD}$ and $V_{SS}$ pins to induce a functional disturbance | $V_{DD}$ = 1.8 V, LQFP100, $T_A$ = +25°C, $f_{HCLK}$ = 48 MHz, conforming to IEC 61000-4-4 | 4B |

### Designing hardened software to avoid noise problems

EMC characterization and optimization are performed at component level with a typical application environment and simplified MCU software. It should be noted that good EMC performance is highly dependent on the user application and the software in particular.

Therefore it is recommended that the user applies EMC software optimization and prequalification tests in relation with the EMC level requested for his application.

**Table 49. I/O current injection susceptibility**

| Symbol | Description | Functional susceptibility | | Unit |
|---|---|---|---|---|
| | | Negative injection | Positive injection | |
| $I_{INJ}$ | Injected current on BOOT0 | -0 | NA | mA |
| | Injected current on PF1 pin (FTf pin) | -0 | NA | |
| | Injected current on PC0 pin (TTA pin) | -0 | +5 | |
| | Injected current on PA4, PA5 pins with induced leakage current on adjacent pins less than -20 µA | -5 | NA | |
| | Injected current on other FT and FTf pins, and on NPOR pin | -5 | NA | |
| | Injected current on all other TC, TTa and RST pins | -5 | +5 | |

## 6.3.13 I/O port characteristics

### General input/output characteristics

Unless otherwise specified, the parameters given in *Table 50* are derived from tests performed under the conditions summarized in *Table 23: General operating conditions*. All I/Os are designed as CMOS- and TTL-compliant.

**Table 50. I/O static characteristics**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{IL}$ | Low level input voltage | TC and TTa I/O | - | - | $0.3\ V_{DDIOx}+0.07^{(1)}$ | V |
| | | FT and FTf I/O | - | - | $0.475\ V_{DDIOx}-0.2^{(1)}$ | |
| | | All I/Os | - | - | $0.3\ V_{DDIOx}$ | |
| $V_{IH}$ | High level input voltage | TC and TTa I/O | $0.445\ V_{DDIOx}+0.398^{(1)}$ | - | - | V |
| | | FT and FTf I/O | $0.5\ V_{DDIOx}+0.2^{(1)}$ | - | - | |
| | | All I/Os | $0.7\ V_{DDIOx}$ | - | - | |
| $V_{hys}$ | Schmitt trigger hysteresis | TC and TTa I/O | - | $200^{(1)}$ | - | mV |
| | | FT and FTf I/O | - | $100^{(1)}$ | - | |
| $I_{lkg}$ | Input leakage current(2) | TC, FT and FTf I/O TTa in digital mode $V_{SS} \le V_{IN} \le V_{DDIOx}$ | - | - | ± 0.1 | µA |
| | | TTa in digital mode $V_{DDIOx} \le V_{IN} \le V_{DDA}$ | - | - | 1 | |
| | | TTa in analog mode $V_{SS} \le V_{IN} \le V_{DDA}$ | - | - | ± 0.2 | |
| | | FT and FTf I/O $V_{DDIOx} \le V_{IN} \le 5$ V | - | - | 10 | |

### Output driving current

The GPIOs (general purpose input/outputs) can sink or source up to +/-8 mA, and sink or source up to +/- 20 mA (with a relaxed $V_{OL}/V_{OH}$).

In the user application, the number of I/O pins which can drive current must be limited to respect the absolute maximum rating specified in *Section 6.2*:

- The sum of the currents sourced by all the I/Os on $V_{DDIOx}$, plus the maximum consumption of the MCU sourced on $V_{DD}$, cannot exceed the absolute maximum rating $\Sigma I_{VDD}$ (see *Table 20: Voltage characteristics*).
- The sum of the currents sunk by all the I/Os on $V_{SS}$, plus the maximum consumption of the MCU sunk on $V_{SS}$, cannot exceed the absolute maximum rating $\Sigma I_{VSS}$ (see *Table 20: Voltage characteristics*).

### Output voltage levels

Unless otherwise specified, the parameters given in the table below are derived from tests performed under the ambient temperature and supply voltage conditions summarized in *Table 23: General operating conditions*. All I/Os are CMOS- and TTL-compliant (FT, TTa or TC unless otherwise specified).

**Table 51. Output voltage characteristics(1)**

| Symbol | Parameter | Conditions | Min | Max | Unit |
|---|---|---|---|---|---|
| $V_{OL}$ | Output low level voltage for an I/O pin | CMOS port(2) $\|I_{IO}\|$ = 8 mA $V_{DDIOx} \geq 2.7$ V | - | 0.4 | V |
| $V_{OH}$ | Output high level voltage for an I/O pin | | $V_{DDIOx}$–0.4 | - | |
| $V_{OL}$ | Output low level voltage for an I/O pin | TTL port(2) $\|I_{IO}\|$ = 8 mA $V_{DDIOx} \geq 2.7$ V | - | 0.4 | V |
| $V_{OH}$ | Output high level voltage for an I/O pin | | 2.4 | - | |
| $V_{OL}$(3) | Output low level voltage for an I/O pin | $\|I_{IO}\|$ = 20 mA $V_{DDIOx} \geq 2.7$ V | - | 1.3 | V |
| $V_{OH}$(3) | Output high level voltage for an I/O pin | | $V_{DDIOx}$–1.3 | - | |
| $V_{OL}$(3) | Output low level voltage for an I/O pin | $\|I_{IO}\|$ = 6 mA $V_{DDIOx} \geq 2$ V | - | 0.4 | V |
| $V_{OH}$(3) | Output high level voltage for an I/O pin | | $V_{DDIOx}$–0.4 | - | |
| $V_{OL}$(4) | Output low level voltage for an I/O pin | $\|I_{IO}\|$ = 4 mA | - | 0.4 | V |
| $V_{OH}$(4) | Output high level voltage for an I/O pin | | $V_{DDIOx}$–0.4 | - | V |
| $V_{OLFm+}$(3) | Output low level voltage for an FTf I/O pin in Fm+ mode | $\|I_{IO}\|$ = 20 mA $V_{DDIOx} \geq 2.7$ V | - | 0.4 | V |
| | | $\|I_{IO}\|$ = 10 mA | - | 0.4 | V |

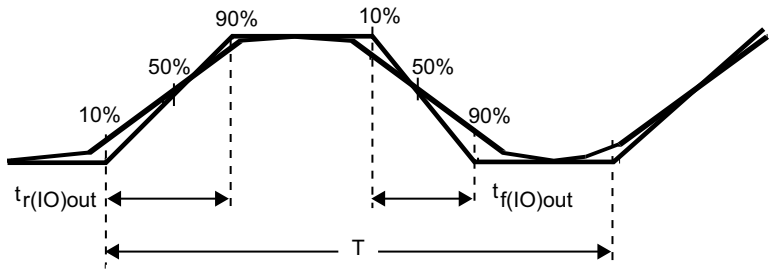
1. The $I_{IO}$ current sourced or sunk by the device must always respect the absolute maximum rating specified in *Table 20: Voltage characteristics*, and the sum of the currents sourced or sunk by all the I/Os (I/O ports and control pins) must always respect the absolute maximum ratings $\Sigma I_{IO}$.
2. TTL and CMOS outputs are compatible with JEDEC standards JESD36 and JESD52.
3. Data based on characterization results. Not tested in production.
4. Data based on characterization results. Not tested in production.

**Table 52. I/O AC characteristics(1)(2) (continued)**

| OSPEEDRy [1:0] value(1) | Symbol | Parameter | Conditions | Min | Max | Unit |
|---|---|---|---|---|---|---|
| Fm+ configuration (4) | $f_{max(IO)out}$ | Maximum frequency(3) | $C_L$ = 50 pF, $V_{DDIOx}$ ≥ 2 V | - | 2 | MHz |
| | $t_{f(IO)out}$ | Output fall time | | - | 12 | ns |
| | $t_{r(IO)out}$ | Output rise time | | - | 34 | |
| | $f_{max(IO)out}$ | Maximum frequency(3) | $C_L$ = 50 pF, $V_{DDIOx}$ < 2 V | - | 0.5 | MHz |
| | $t_{f(IO)out}$ | Output fall time | | - | 16 | ns |
| | $t_{r(IO)out}$ | Output rise time | | - | 44 | |
| - | $t_{EXTIpw}$ | Pulse width of external signals detected by the EXTI controller | - | 10 | - | ns |

1. The I/O speed is configured using the OSPEEDRx[1:0] bits. Refer to the STM32F0xxxx RM0091 reference manual for a description of GPIO Port configuration register.
2. Guaranteed by design, not tested in production.
3. The maximum frequency is defined in *Figure 24*.
4. When Fm+ configuration is set, the I/O speed control is bypassed. Refer to the STM32F0xxxx reference manual RM0091 for a detailed description of Fm+ I/O configuration.

**Figure 24. I/O AC characteristics definition**




Maximum frequency is achieved if $(t_r + t_f) \le \frac{2}{3}T$ and if the duty cycle is (45-55%)
when loaded by $C_L$ (see the table *I/O AC characteristics definition*)

MS32132V3

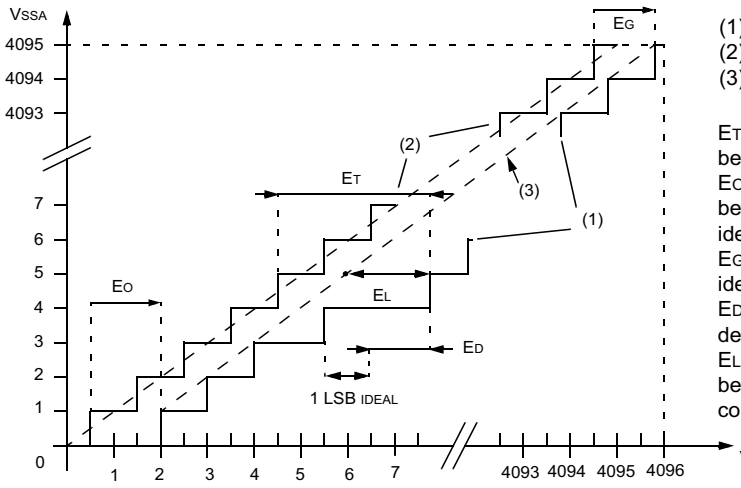
## 6.3.14 NRST and NPOR pin characteristics

### NRST pin characteristics

The NRST pin input driver uses the CMOS technology. It is connected to a permanent pull-up resistor, $R_{PU}$.

Unless otherwise specified, the parameters given in the table below are derived from tests performed under the ambient temperature and supply voltage conditions summarized in *Table 23: General operating conditions*.

**Figure 26. ADC accuracy characteristics**

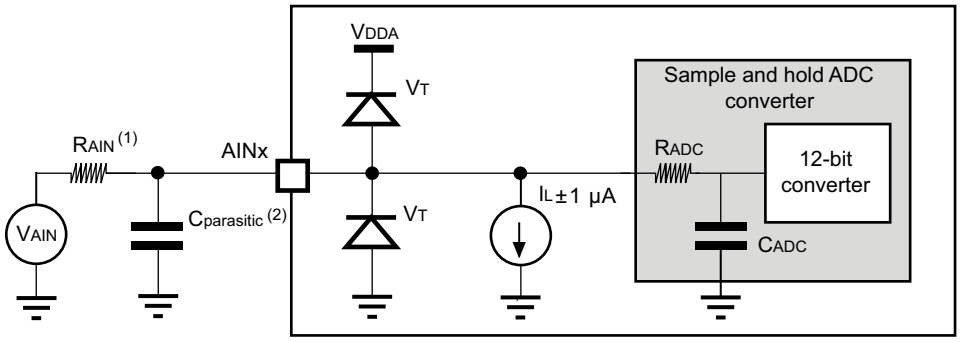



(1) Example of an actual transfer curve
(2) The ideal transfer curve
(3) End point correlation line

$E_T$ = Total Unajusted Error: maximum deviation between the actual and ideal transfer curves.
$E_O$ = Offset Error: maximum deviation between the first actual transition and the first ideal one.
$E_G$ = Gain Error: deviation between the last ideal transition and the last actual one.
$E_D$ = Differential Linearity Error: maximum deviation between actual steps and the ideal ones.
$E_L$ = Integral Linearity Error: maximum deviation between any actual transition and the end point correlation line.

MS19880V2

**Figure 27. Typical connection diagram using the ADC**




MS33900V2

1. Refer to *Table 55: ADC characteristics* for the values of $R_{AIN}$, $R_{ADC}$ and $C_{ADC}$.
2. $C_{parasitic}$ represents the capacitance of the PCB (dependent on soldering and PCB layout quality) plus the pad capacitance (roughly 7 pF). A high $C_{parasitic}$ value will downgrade conversion accuracy. To remedy this, $f_{ADC}$ should be reduced.

## General PCB design guidelines

Power supply decoupling should be performed as shown in *Figure 13: Power supply scheme*. The 10 nF capacitor should be ceramic (good quality) and it should be placed as close as possible to the chip.

### 6.3.17 Comparator characteristics

**Table 59. Comparator characteristics**

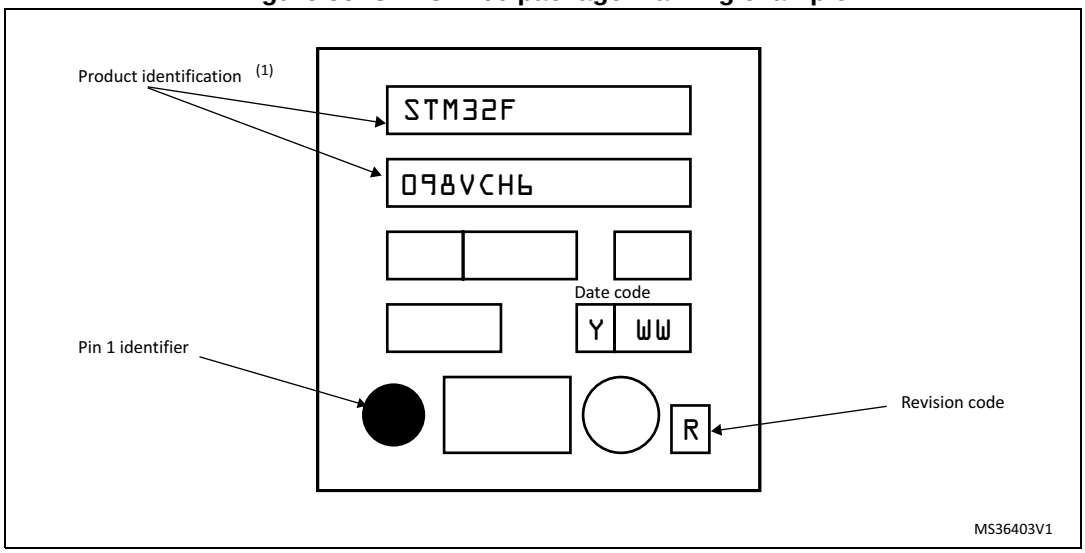
| Symbol | Parameter | Conditions | | Min(1) | Typ | Max(1) | Unit |
|---|---|---|---|---|---|---|---|
| $V_{DDA}$ | Analog supply voltage | - | | $V_{DD}$ | - | 3.6 | V |
| $V_{IN}$ | Comparator input voltage range | - | | 0 | - | $V_{DDA}$ | - |
| $V_{SC}$ | $V_{REFINT}$ scaler offset voltage | - | | - | ±5 | ±10 | mV |
| $t_{S\_SC}$ | $V_{REFINT}$ scaler startup time from power down | - | | - | - | 0.2 | ms |
| $t_{START}$ | Comparator startup time | Startup time to reach propagation delay specification | | - | - | 60 | µs |
| $t_D$ | Propagation delay for 200 mV step with 100 mV overdrive | Ultra-low power mode | | - | 2 | 4.5 | µs |
| | | Low power mode | | - | 0.7 | 1.5 | |
| | | Medium power mode | | - | 0.3 | 0.6 | |
| | | High speed mode | $V_{DDA} \geq 2.7$ V | - | 50 | 100 | ns |
| | | | $V_{DDA} < 2.7$ V | - | 100 | 240 | |
| | Propagation delay for full range step with 100 mV overdrive | Ultra-low power mode | | - | 2 | 7 | µs |
| | | Low power mode | | - | 0.7 | 2.1 | |
| | | Medium power mode | | - | 0.3 | 1.2 | |
| | | High speed mode | $V_{DDA} \geq 2.7$ V | - | 90 | 180 | ns |
| | | | $V_{DDA} < 2.7$ V | - | 110 | 300 | |
| $V_{offset}$ | Comparator offset error | - | | - | ±4 | ±10 | mV |
| $dV_{offset}/dT$ | Offset error temperature coefficient | - | | - | 18 | - | µV/°C |
| $I_{DD(COMP)}$ | COMP current consumption | Ultra-low power mode | | - | 1.2 | 1.5 | µA |
| | | Low power mode | | - | 3 | 5 | |
| | | Medium power mode | | - | 10 | 15 | |
| | | High speed mode | | - | 75 | 100 | |

### Device marking

The following figure gives an example of topside marking orientation versus pin 1 identifier location.

Other optional marking or inset/upset marks, which identify the parts throughout supply chain operations, are not indicated below.

**Figure 35. UFBGA100 package marking example**



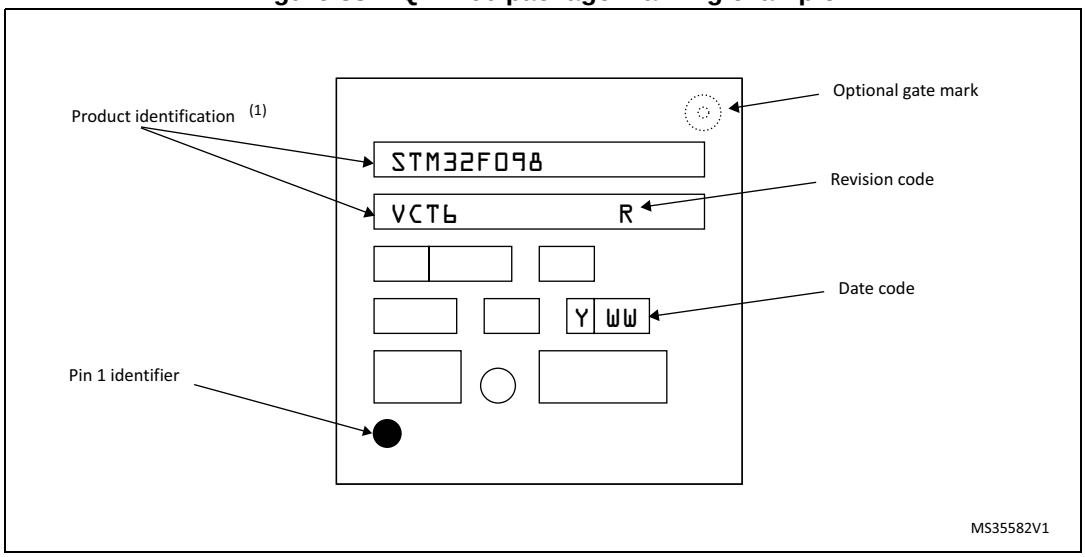

1. Parts marked as "ES", "E" or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering Samples to run qualification activity.

### Device marking

The following figure gives an example of topside marking orientation versus pin 1 identifier location.

Other optional marking or inset/upset marks, which identify the parts throughout supply chain operations, are not indicated below.

**Figure 38. LQFP100 package marking example**

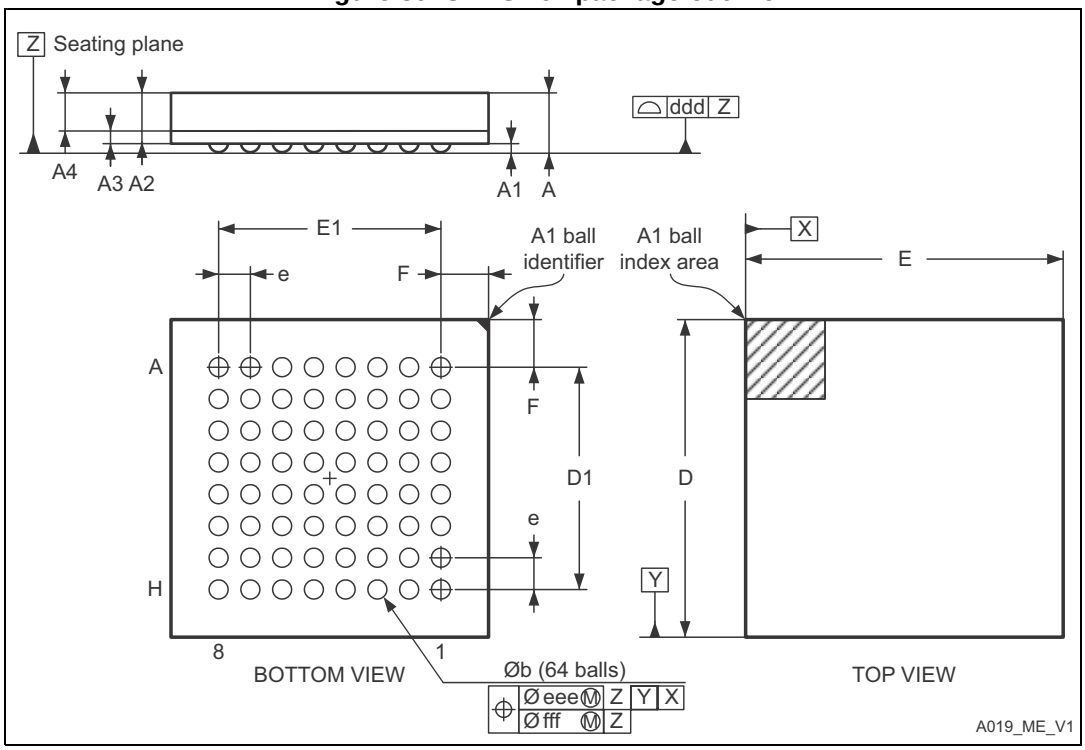



1. Parts marked as "ES", "E" or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering Samples to run qualification activity.

## 7.3 UFBGA64 package information

**UFBGA64 is a 64-ball, 5 x 5 mm, 0.5 mm pitch ultra-fine-profile ball grid array package.**

**Figure 39. UFBGA64 package outline**




1. Drawing is not to scale.

**Table 71. UFBGA64 package mechanical data**

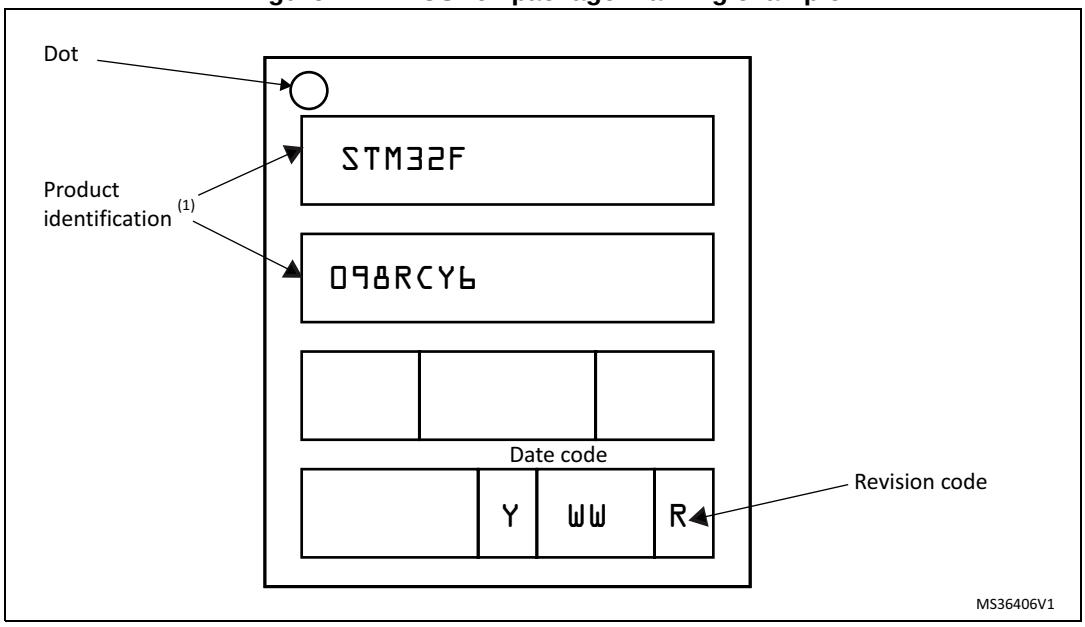
| Symbol | millimeters | | | inches[1] | | |
|---|---|---|---|---|---|---|
| | Min | Typ | Max | Min | Typ | Max |
| A | 0.460 | 0.530 | 0.600 | 0.0181 | 0.0209 | 0.0236 |
| A1 | 0.050 | 0.080 | 0.110 | 0.0020 | 0.0031 | 0.0043 |
| A2 | 0.400 | 0.450 | 0.500 | 0.0157 | 0.0177 | 0.0197 |
| A3 | 0.080 | 0.130 | 0.180 | 0.0031 | 0.0051 | 0.0071 |
| A4 | 0.270 | 0.320 | 0.370 | 0.0106 | 0.0126 | 0.0146 |
| b | 0.170 | 0.280 | 0.330 | 0.0067 | 0.0110 | 0.0130 |
| D | 4.850 | 5.000 | 5.150 | 0.1909 | 0.1969 | 0.2028 |
| D1 | 3.450 | 3.500 | 3.550 | 0.1358 | 0.1378 | 0.1398 |
| E | 4.850 | 5.000 | 5.150 | 0.1909 | 0.1969 | 0.2028 |
| E1 | 3.450 | 3.500 | 3.550 | 0.1358 | 0.1378 | 0.1398 |
| e | - | 0.500 | - | - | 0.0197 | - |
| F | 0.700 | 0.750 | 0.800 | 0.0276 | 0.0295 | 0.0315 |

### Device marking

The following figure gives an example of topside marking orientation versus ball A1 identifier location.

Other optional marking or inset/upset marks, which identify the parts throughout supply chain operations, are not indicated below.

**Figure 44. WLCSP64 package marking example**



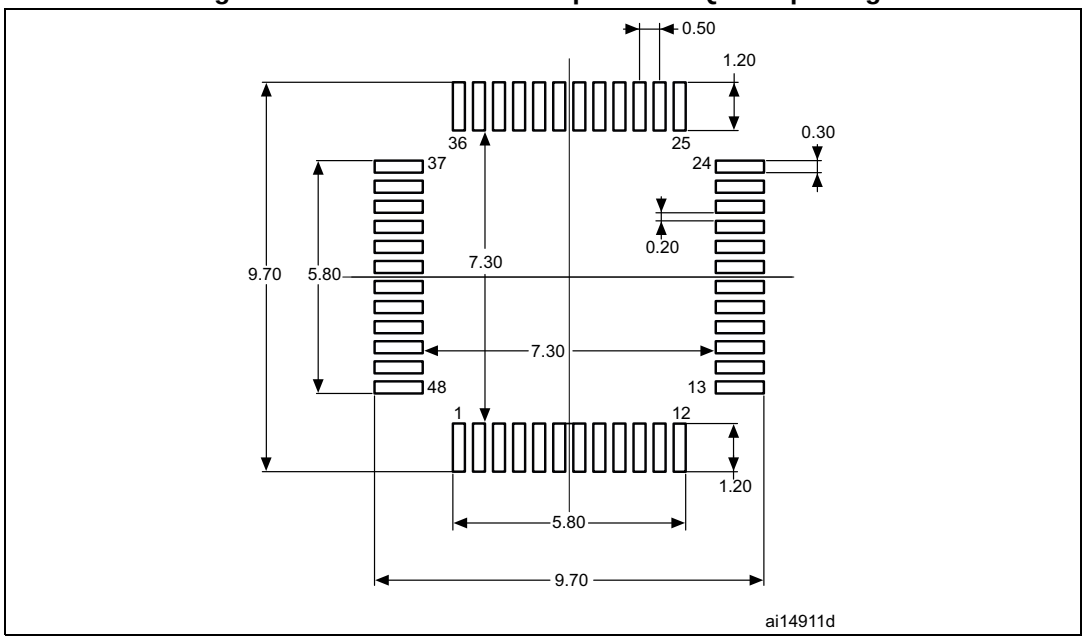

1. Parts marked as "ES", "E" or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering Samples to run qualification activity.

**Table 76. LQFP48 package mechanical data**

| Symbol | millimeters | | | inches[1] | | |
|---|---|---|---|---|---|---|
| | Min | Typ | Max | Min | Typ | Max |
| A | - | - | 1.600 | - | - | 0.0630 |
| A1 | 0.050 | - | 0.150 | 0.0020 | - | 0.0059 |
| A2 | 1.350 | 1.400 | 1.450 | 0.0531 | 0.0551 | 0.0571 |
| b | 0.170 | 0.220 | 0.270 | 0.0067 | 0.0087 | 0.0106 |
| c | 0.090 | - | 0.200 | 0.0035 | - | 0.0079 |
| D | 8.800 | 9.000 | 9.200 | 0.3465 | 0.3543 | 0.3622 |
| D1 | 6.800 | 7.000 | 7.200 | 0.2677 | 0.2756 | 0.2835 |
| D3 | - | 5.500 | - | - | 0.2165 | - |
| E | 8.800 | 9.000 | 9.200 | 0.3465 | 0.3543 | 0.3622 |
| E1 | 6.800 | 7.000 | 7.200 | 0.2677 | 0.2756 | 0.2835 |
| E3 | - | 5.500 | - | - | 0.2165 | - |
| e | - | 0.500 | - | - | 0.0197 | - |
| L | 0.450 | 0.600 | 0.750 | 0.0177 | 0.0236 | 0.0295 |
| L1 | - | 1.000 | - | - | 0.0394 | - |
| k | 0° | 3.5° | 7° | 0° | 3.5° | 7° |
| ccc | - | - | 0.080 | - | - | 0.0031 |

1. Values in inches are converted from mm and rounded to 4 decimal digits.

**Figure 49. Recommended footprint for LQFP48 package**



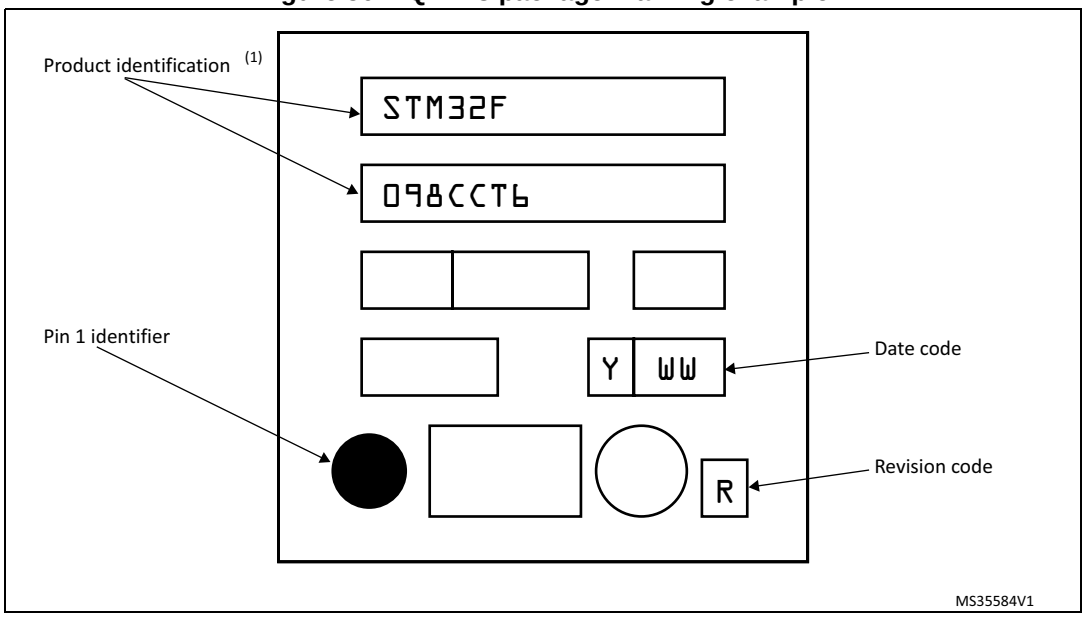

1. Dimensions are expressed in millimeters.

### Device marking

The following figure gives an example of topside marking orientation versus pin 1 identifier location.

Other optional marking or inset/upset marks, which identify the parts throughout supply chain operations, are not indicated below.

**Figure 50. LQFP48 package marking example**




1. Parts marked as "ES", "E" or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering Samples to run qualification activity.

Each temperature range suffix corresponds to a specific guaranteed ambient temperature at maximum dissipation and, to a specific maximum junction temperature.

As applications do not commonly use the STM32F098CC/RC/VC at maximum dissipation, it is useful to calculate the exact power consumption and junction temperature to determine which temperature range will be best suited to the application.

The following examples show how to calculate the temperature range needed for a given application.

### Example 1: High-performance application

Assuming the following application conditions:

Maximum temperature $T_{Amax}$ = 82 °C (measured according to JESD51-2), $I_{DDmax}$ = 50 mA, $V_{DD}$ = 3.5 V, maximum 20 I/Os used at the same time in output at low level with $I_{OL}$ = 8 mA, $V_{OL}$= 0.4 V and maximum 8 I/Os used at the same time in output at low level with $I_{OL}$ = 20 mA, $V_{OL}$= 1.3 V

$P_{INTmax}$ = 50 mA × 3.5 V= 175 mW

$P_{IOmax}$ = 20 × 8 mA × 0.4 V + 8 × 20 mA × 1.3 V = 272 mW

This gives: $P_{INTmax}$ = 175 mW and $P_{IOmax}$ = 272 mW:

$P_{Dmax}$ = 175 + 272 = 447 mW

Using the values obtained in *Table 78* $T_{Jmax}$ is calculated as follows:

– For LQFP64, 45 °C/W

$T_{Jmax}$ = 82 °C + (45 °C/W × 447 mW) = 82 °C + 20.115 °C = 102.115 °C

This is within the range of the suffix 6 version parts (–40 < $T_J$ < 105 °C).

In this case, parts must be ordered at least with the temperature range suffix 6 (see *Section 8: Ordering information*).

*Note: With this given $P_{Dmax}$ we can find the $T_{Amax}$ allowed for a given device temperature range (order code suffix 6 or 7).*

*Suffix 6: $T_{Amax} = T_{Jmax}$ - (45°C/W × 447 mW) = 105-20.115 = 84.885 °C*

*Suffix 7: $T_{Amax} = T_{Jmax}$ - (45°C/W × 447 mW) = 125-20.115 = 104.885 °C*

### Example 2: High-temperature application

Using the same rules, it is possible to address applications that run at high temperatures with a low dissipation, as long as junction temperature $T_J$ remains within the specified range.

Assuming the following application conditions:

Maximum temperature $T_{Amax}$ = 100 °C (measured according to JESD51-2), $I_{DDmax}$ = 20 mA, $V_{DD}$ = 3.5 V, maximum 20 I/Os used at the same time in output at low level with $I_{OL}$ = 8 mA, $V_{OL}$= 0.4 V

$P_{INTmax}$ = 20 mA × 3.5 V= 70 mW

$P_{IOmax}$ = 20 × 8 mA × 0.4 V = 64 mW

This gives: $P_{INTmax}$ = 70 mW and $P_{IOmax}$ = 64 mW:

$P_{Dmax}$ = 70 + 64 = 134 mW

Thus: $P_{Dmax}$ = 134 mW

**Table 80. Document revision history (continued)**

| Date | Revision | Changes |
|---|---|---|
| 17-Dec-2015 | 3 (continued) | ***Section 6: Electrical characteristics*:**<br>– footnote for $V_{IN}$ max value in *Table 20: Voltage characteristics*<br>– footnote for $V_{IN}$ max value in *Table 23: General operating conditions*<br>– *Table 25: Embedded internal reference voltage*: added $t_{START}$ parameter and removal of -40°-to-85° condition for $V_{REFINT}$ and associated note<br>– *Figure 18: Typical application with a 32.768 kHz crystal* - correction of OSC_IN and OSC_OUT to OSC32_IN and OSC32_OUT and $f_{HSE}$ to $f_{LSE}$<br>– *Table 47: ESD absolute maximum ratings* updated<br>– $V_{DDIOx}$ replaced $V_{DD}$ in *Figure 22: TC and TTa I/O input characteristics* and *Figure 23: Five volt tolerant (FT and FTf) I/O input characteristics*<br>– *Table 50: I/O static characteristics*- note removed<br>– *Table 55: ADC characteristics* - updated some parameter values, test conditions and added footnotes (3) and (4)<br>– $I_{DDA}$ max value (DAC DC current consumption) in *Table 58: DAC characteristics*<br>– *Table 59: Comparator characteristics* - min value added for $V_{DDA}$<br>– *Table 60: TS characteristics*: removed the minimum value for $t_{START}$ symbol and updated parameter name<br>– R parameter typical. value in *Table 61: $V_{BAT}$ monitoring characteristics*<br>– *Table 62: TIMx characteristics*: removed $Res_{TM}$ parameter line and all values put in new Typ column, $t_{COUNTER}$ substituted with $t_{MAX\_COUNT}$, values defined as powers of two<br>– *Table 67: $I^2S$ characteristics* reorganized and max value added for $t_{v(SD\_ST)}$<br>– *Figure 32: $I^2S$ master timing diagram (Philips protocol)* added definition of edge level references<br>***Section 7: Package information*:**<br>– *Figure 33: UFBGA100 package outline* and associated *Table 68* updated<br>– *Figure 34* and associated *Table 69* updated<br>– *Figure 35: UFBGA100 package marking example* and associated text updated<br>– *Figure 38: LQFP100 package marking example* and associated text updated<br>– *Table 72: UFBGA64 recommended PCB design rules* added<br>– *Figure 41: UFBGA64 package marking example* added<br>***Section 8: Part numbering*:**<br>– added tray packing to options |