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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M0
Core Size	32-Bit Single-Core
Speed	48MHz
Connectivity	CANbus, I²C, IrDA, LINbus, SPI, UART/USART
Peripherals	DMA, I²S, POR, PWM, WDT
Number of I/O	51
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	32K x 8
Voltage - Supply (Vcc/Vdd)	1.65V ~ 3.6V
Data Converters	A/D 19x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-LQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32f098rct6

4 Pinouts and pin descriptions

Figure 3. UFBGA100 package pinout

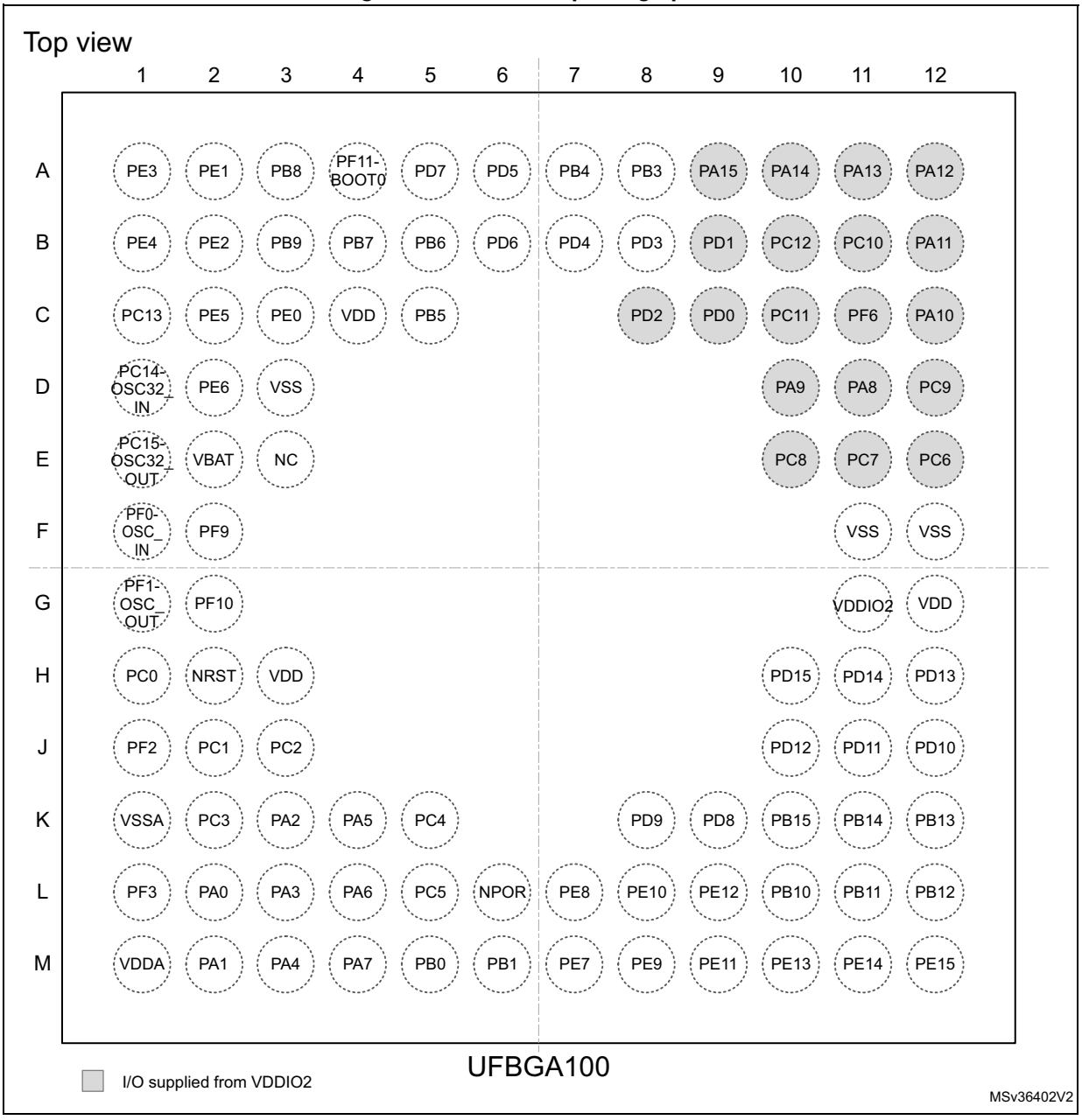
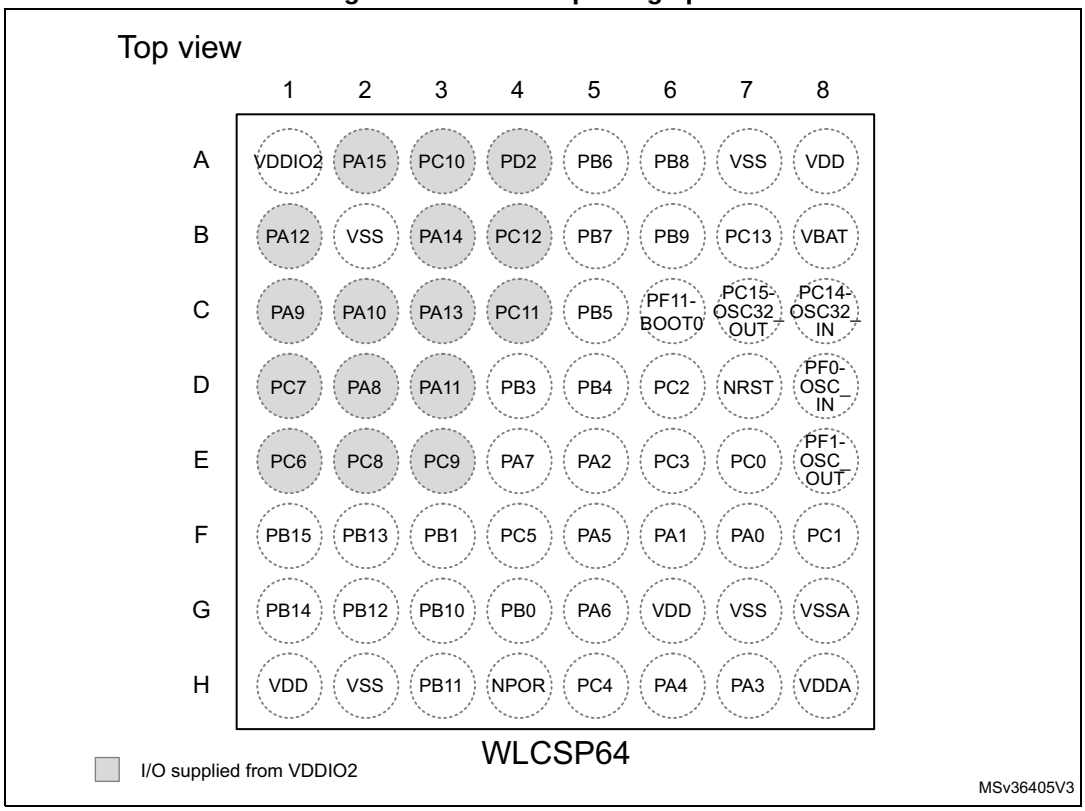


Figure 7. WLCSP64 package pinout



1. The above figure shows the package in top view, changing from bottom view in the previous document versions.

Figure 8. LQFP48 package pinout

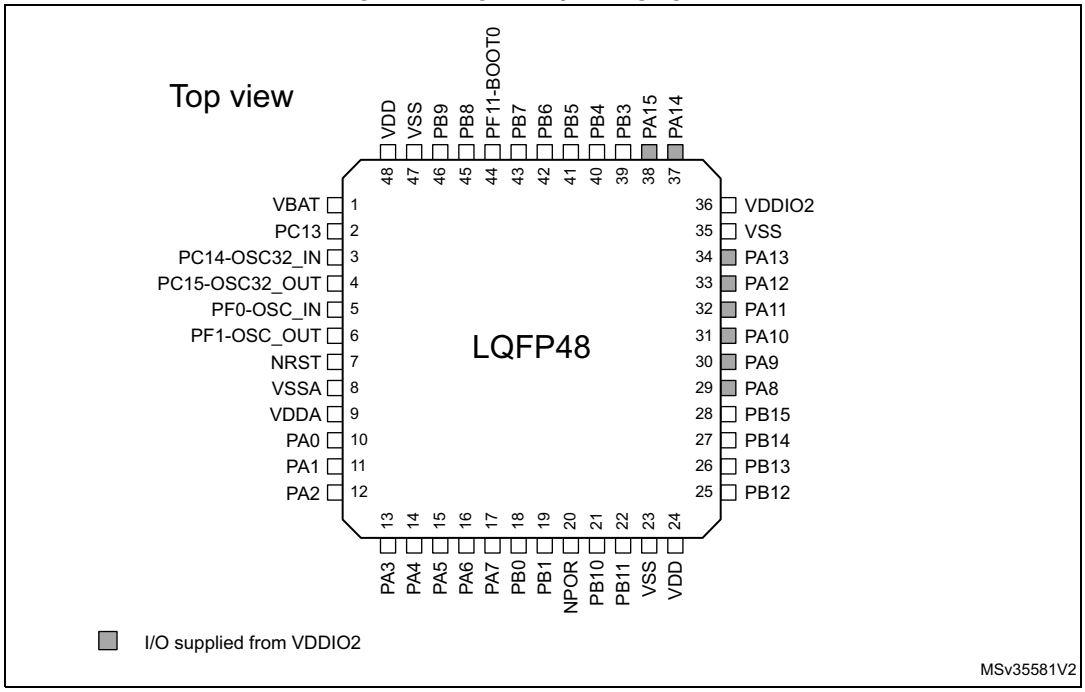


Table 11. Legend/abbreviations used in the pinout table (continued)

Name		Abbreviation	Definition
Pin functions	Alternate functions	Functions selected through GPIOx_AFR registers	
	Additional functions	Functions directly selected/enabled through peripheral registers	

Table 12. STM32F098CC/RC/VC pin definitions

Pin numbers						Pin name (function upon reset)	Pin type	I/O structure	Notes	Pin functions	
UFBGA100	LQFP100	UFBGA64	LQFP64	WLCSP64	LQFP48/UFQFPN48					Alternate functions	Additional functions
B2	1	-	-	-	-	PE2	I/O	FT		TSC_G7_IO1, TIM3_ETR	-
A1	2	-	-	-	-	PE3	I/O	FT		TSC_G7_IO2, TIM3_CH1	-
B1	3	-	-	-	-	PE4	I/O	FT		TSC_G7_IO3, TIM3_CH2	-
C2	4	-	-	-	-	PE5	I/O	FT		TSC_G7_IO4, TIM3_CH3	-
D2	5	-	-	-	-	PE6	I/O	FT		TIM3_CH4	WKUP3, RTC_TAMP3
E2	6	B2	1	B8	1	VBAT	S	-	-	Backup power supply	
C1	7	A2	2	B7	2	PC13	I/O	TC	(1) (2)	-	WKUP2, RTC_TAMP1, RTC_TS, RTC_OUT
D1	8	A1	3	C8	3	PC14-OSC32_IN (PC14)	I/O	TC	(1) (2)	-	OSC32_IN
E1	9	B1	4	C7	4	PC15-OSC32_OUT (PC15)	I/O	TC	(1) (2)	-	OSC32_OUT
F2	10	-	-	-	-	PF9	I/O	FT		TIM15_CH1, USART6_TX	-
G2	11	-	-	-	-	PF10	I/O	FT		TIM15_CH2, USART6_RX	-
F1	12	C1	5	D8	5	PF0-OSC_IN (PF0)	I/O	FTf		CRS_ SYNC, I2C1_SDA	OSC_IN
G1	13	D1	6	E8	6	PF1-OSC_OUT (PF1)	I/O	FTf		I2C1_SCL	OSC_OUT
H2	14	E1	7	D7	7	NRST	I/O	RST		Device reset input / internal reset output (active low)	

Table 12. STM32F098CC/RC/VC pin definitions (continued)

Pin numbers						Pin name (function upon reset)	Pin type	I/O structure	Notes	Pin functions	
UFBGA100	LQFP100	UFBGA64	LQFP64	WLCSP64	LQFP48/UFQFPN48					Alternate functions	Additional functions
H3	28	D2	19	G6	-	VDD	S	-		Digital power supply	
M3	29	H3	20	H6	14	PA4	I/O	TTa		SPI1_NSS, I2S1_WS, TIM14_CH1, TSC_G2_IO1, USART2_CK, USART6_TX	COMP1_INM4, COMP2_INM4, ADC_IN4, DAC_OUT1
K4	30	F4	21	F5	15	PA5	I/O	TTa		SPI1_SCK, I2S1_CK, CEC, TIM2_CH1_ETR, TSC_G2_IO2, USART6_RX	COMP1_INM5, COMP2_INM5, ADC_IN5, DAC_OUT2
L4	31	G4	22	G5	16	PA6	I/O	TTa		SPI1_MISO, I2S1_MCK, TIM3_CH1, TIM1_BKIN, TIM16_CH1, COMP1_OUT, TSC_G2_IO3, EVENTOUT, USART3_CTS	ADC_IN6
M4	32	H4	23	E4	17	PA7	I/O	TTa		SPI1_MOSI, I2S1_SD, TIM3_CH2, TIM14_CH1, TIM1_CH1N, TIM17_CH1, COMP2_OUT, TSC_G2_IO4, EVENTOUT	ADC_IN7
K5	33	H5	24	H5	-	PC4	I/O	TTa		EVENTOUT, USART3_TX	ADC_IN14
L5	34	H6	25	F4	-	PC5	I/O	TTa		TSC_G3_IO1, USART3_RX	ADC_IN15, WKUP5
M5	35	F5	26	G4	18	PB0	I/O	TTa		TIM3_CH3, TIM1_CH2N, TSC_G3_IO2, EVENTOUT, USART3_CK	ADC_IN8
M6	36	G5	27	F3	19	PB1	I/O	TTa		TIM3_CH4, USART3_RTS, TIM14_CH1, TIM1_CH3N, TSC_G3_IO3	ADC_IN9
L6	37	G6	28	H4	20	NPOR	I	POR	(3)	Device power-on reset input (active low)	
M7	38	-	-	-	-	PE7	I/O	FT		TIM1_ETR, USART5_CK_RTS	-

Table 17. Alternate functions selected through GPIOE_AFR registers for port E

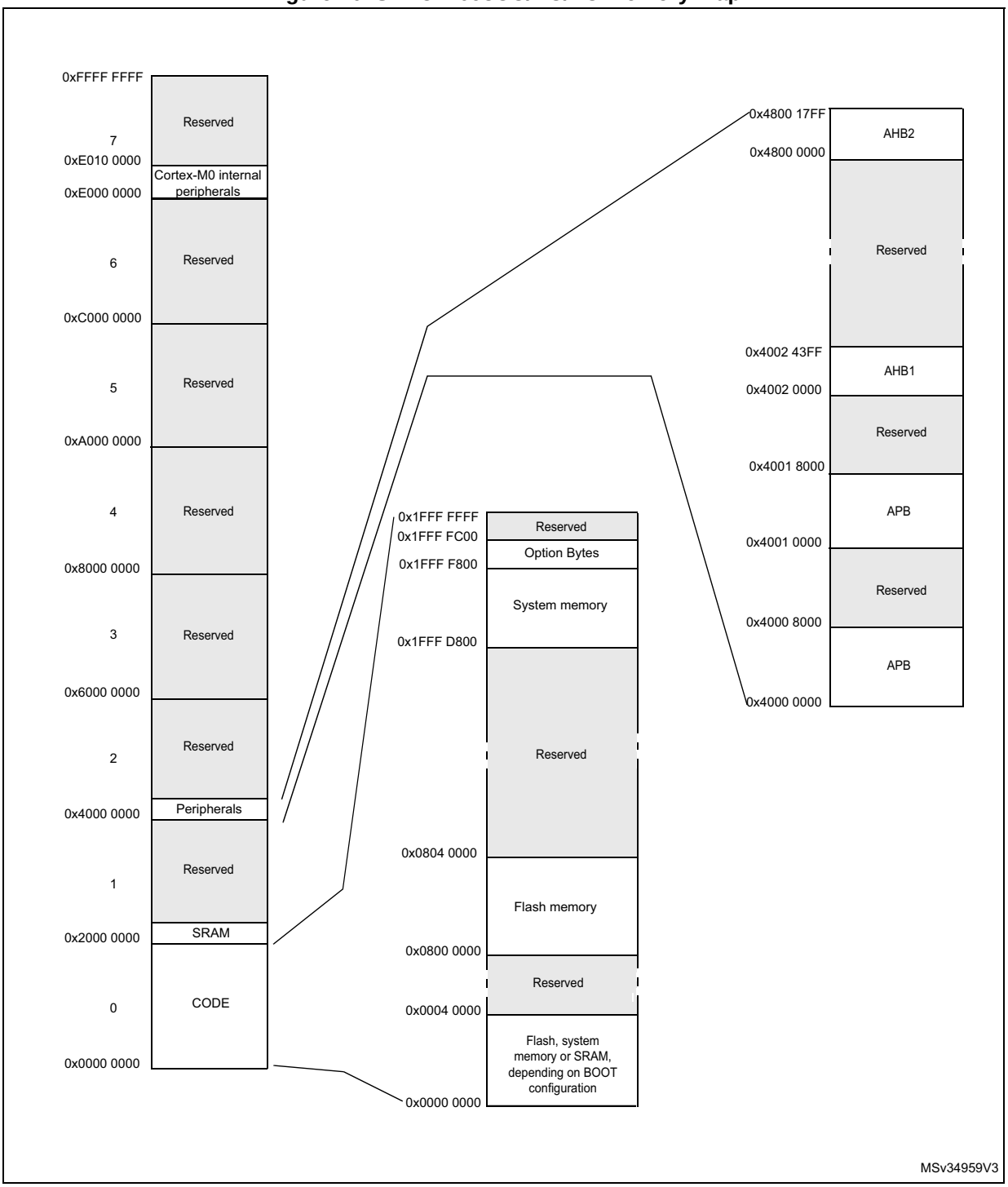
Pin name	AF0	AF1
PE0	TIM16_CH1	EVENTOUT
PE1	TIM17_CH1	EVENTOUT
PE2	TIM3_ETR	TSC_G7_IO1
PE3	TIM3_CH1	TSC_G7_IO2
PE4	TIM3_CH2	TSC_G7_IO3
PE5	TIM3_CH3	TSC_G7_IO4
PE6	TIM3_CH4	-
PE7	TIM1_ETR	USART5_CK_RTS
PE8	TIM1_CH1N	USART4_TX
PE9	TIM1_CH1	USART4_RX
PE10	TIM1_CH2N	USART5_TX
PE11	TIM1_CH2	USART5_RX
PE12	TIM1_CH3N	SPI1_NSS, I2S1_WS
PE13	TIM1_CH3	SPI1_SCK, I2S1_CK
PE14	TIM1_CH4	SPI1_MISO, I2S1_MCK
PE15	TIM1_BKIN	SPI1_MOSI, I2S1_SD

Table 18. Alternate functions selected through GPIOF_AFR registers for port F

Pin name	AF0	AF1	AF2
PF0	CRS_SYNC	I2C1_SDA	-
PF1	-	I2C1_SCL	-
PF2	EVENTOUT	USART7_TX	USART7_CK_RTS
PF3	EVENTOUT	USART7_RX	USART6_CK_RTS
PF6	-	-	-
PF9	TIM15_CH1	USART6_TX	-
PF10	TIM15_CH2	USART6_RX	-

5 Memory mapping

Figure 10. STM32F098CC/RC/VC memory map



6 Electrical characteristics

6.1 Parameter conditions

Unless otherwise specified, all voltages are referenced to V_{SS}.

6.1.1 Minimum and maximum values

Unless otherwise specified, the minimum and maximum values are guaranteed in the worst conditions of ambient temperature, supply voltage and frequencies by tests in production on 100% of the devices with an ambient temperature at T_A = 25 °C and T_A = $T_A$max (given by the selected temperature range).

Data based on characterization results, design simulation and/or technology characteristics are indicated in the table footnotes and are not tested in production. Based on characterization, the minimum and maximum values refer to sample tests and represent the mean value plus or minus three times the standard deviation (mean ±3σ).

6.1.2 Typical values

Unless otherwise specified, typical data are based on T_A = 25 °C, V_{DD} = 1.8 V and V_{DDA} = 3.3 V. They are given only as design guidelines and are not tested.

Typical ADC accuracy values are determined by characterization of a batch of samples from a standard diffusion lot over the full temperature range, where 95% of the devices have an error less than or equal to the value indicated (mean ±2σ).

6.1.3 Typical curves

Unless otherwise specified, all typical curves are given only as design guidelines and are not tested.

6.1.4 Loading capacitor

The loading conditions used for pin parameter measurement are shown in *Figure 11*.

6.1.5 Pin input voltage

The input voltage measurement on a pin of the device is described in *Figure 12*.

Figure 11. Pin loading conditions

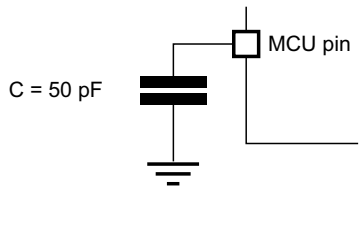


Figure 12. Pin input voltage

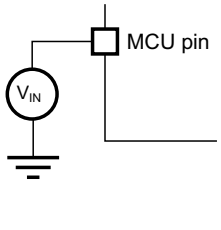
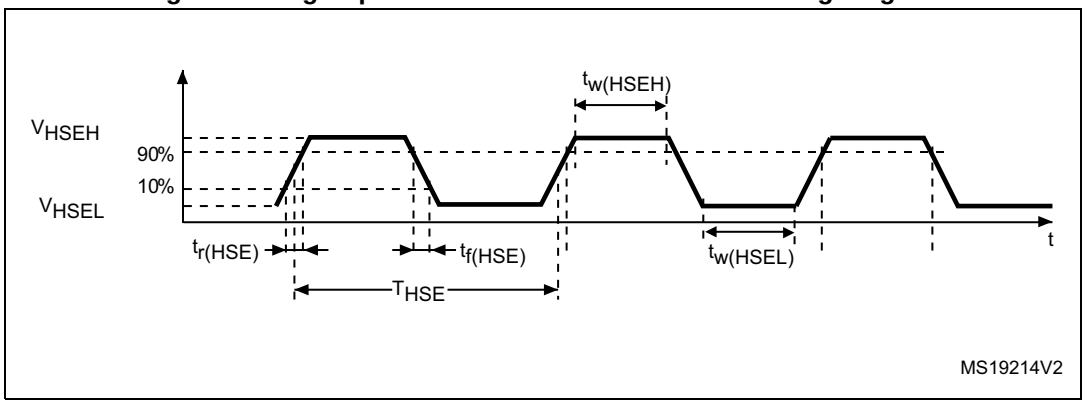


Table 32. Peripheral current consumption (continued)

Peripheral		Typical consumption at 25 °C	Unit
APB	APB-Bridge(2)	3.6	µA/MHz
	ADC(3)	4.3	
	CAN	12.4	
	CEC	0.4	
	CRS	0.0	
	DAC(3)	4.2	
	DBG (MCU Debug Support)	0.2	
	I2C1	2.9	
	I2C2	2.4	
	PWR	0.6	
	SPI1	8.8	
	SPI2	7.8	
	SYSCFG and COMP	1.9	
	TIM1	15.2	
	TIM14	2.6	
	TIM15	8.7	
	TIM16	5.8	
	TIM17	7.0	
	TIM2	16.2	
	TIM3	11.9	
	TIM6	11.8	
	TIM7	2.5	
	USART1	17.6	
	USART2	16.3	
	USART3	16.2	
	USART4	4.7	
	USART5	4.4	
	USART6	5.5	
	USART7	5.2	
	USART8	5.1	
	WWDG	1.1	
	All APB peripherals	**207.2**	

1. The BusMatrix is automatically active when at least one master is ON (CPU, DMA).
2. The APB Bridge is automatically active when at least one peripheral is ON on the Bus.
3. The power consumption of the analog part (I_{DDA}) of peripherals such as ADC, DAC, comparators, is not included. Refer to the tables of characteristics in the subsequent sections.

Figure 15. High-speed external clock source AC timing diagram



Low-speed external user clock generated from an external source

In bypass mode the LSE oscillator is switched off and the input pin is a standard GPIO.

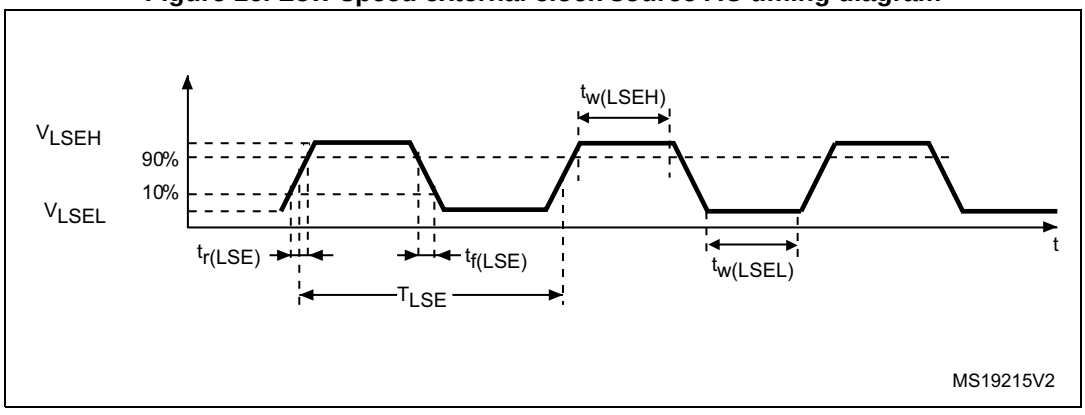
The external clock signal has to respect the I/O characteristics in *Section 6.3.13*. However, the recommended clock input waveform is shown in *Figure 16*.

Table 35. Low-speed external user clock characteristics

Symbol	Parameter(1)	Min	Typ	Max	Unit
f_{LSE_ext}	User external clock source frequency	-	32.768	1000	kHz
V_{LSEH}	OSC32_IN input pin high level voltage	0.7 V_{DDIOx}	-	V_{DDIOx}	V
V_{LSEL}	OSC32_IN input pin low level voltage	V_{SS}	-	0.3 V_{DDIOx}	
$t_{w(LSEH)}$ $t_{w(LSEL)}$	OSC32_IN high or low time	450	-	-	ns
$t_{r(LSE)}$ $t_{f(LSE)}$	OSC32_IN rise or fall time	-	-	50	

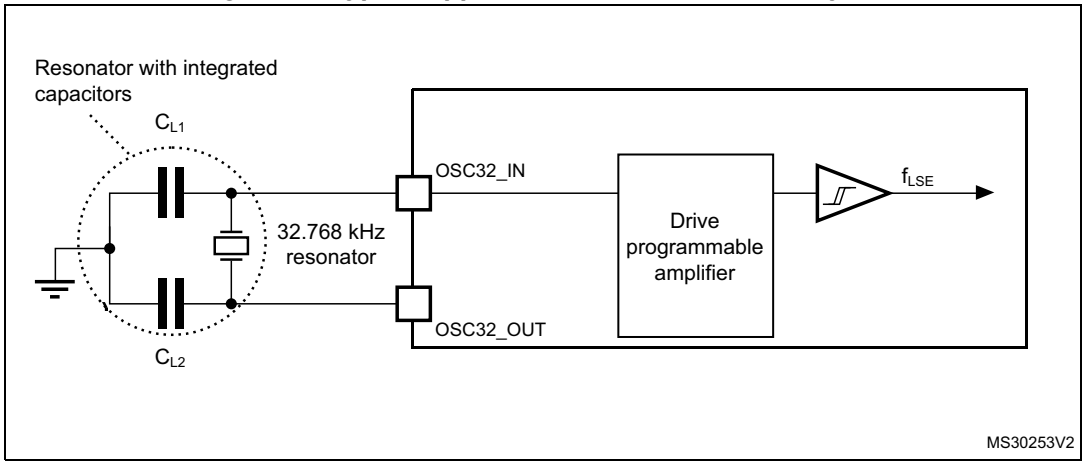
1. Guaranteed by design, not tested in production.

Figure 16. Low-speed external clock source AC timing diagram



Note: For information on selecting the crystal, refer to the application note AN2867 "Oscillator design guide for ST microcontrollers" available from the ST website www.st.com.

Figure 18. Typical application with a 32.768 kHz crystal



Note: An external resistor is not required between OSC32_IN and OSC32_OUT and it is forbidden to add one.

6.3.7 Internal clock source characteristics

The parameters given in *Table 38* are derived from tests performed under ambient temperature and supply voltage conditions summarized in *Table 23: General operating conditions*. The provided curves are characterization results, not tested in production.

Table 50. I/O static characteristics (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
R_{PU}	Weak pull-up equivalent resistor (3)	$V_{IN} = V_{SS}$	25	40	55	kΩ
R_{PD}	Weak pull-down equivalent resistor(3)	$V_{IN} = - V_{DDIOx}$	25	40	55	kΩ
C_{IO}	I/O pin capacitance	-	-	5	-	pF

1. Data based on design simulation only. Not tested in production.
2. The leakage could be higher than the maximum value, if negative current is injected on adjacent pins. Refer to *Table 49: I/O current injection susceptibility*.
3. Pull-up and pull-down resistors are designed with a true resistance in series with a switchable PMOS/NMOS. This PMOS/NMOS contribution to the series resistance is minimal (~10% order).

All I/Os are CMOS- and TTL-compliant (no software configuration required). Their characteristics cover more than the strict CMOS-technology or TTL parameters. The coverage of these requirements is shown in *Figure 22* for standard I/Os, and in *Figure 23* for 5 V-tolerant I/Os. The following curves are design simulation results, not tested in production.

Input/output AC characteristics

The definition and values of input/output AC characteristics are given in *Figure 24* and *Table 52*, respectively. Unless otherwise specified, the parameters given are derived from tests performed under the ambient temperature and supply voltage conditions summarized in *Table 23: General operating conditions*.

Table 52. I/O AC characteristics(1)(2)

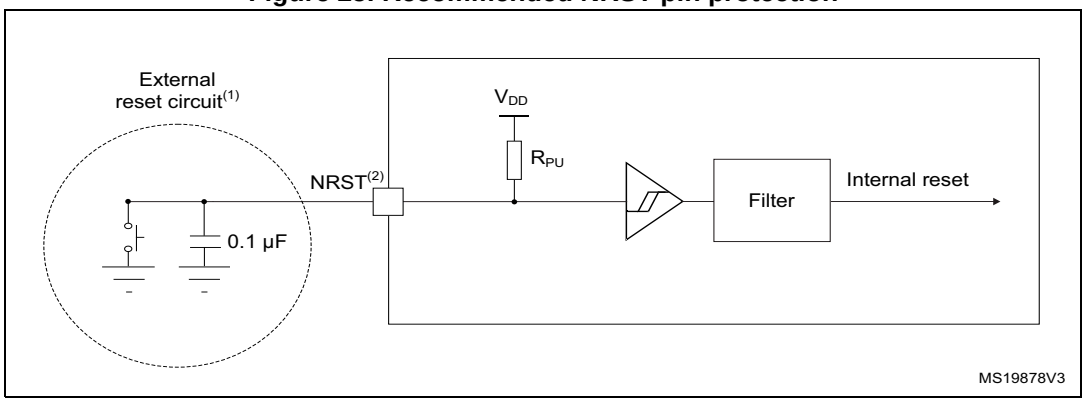
OSPEEDRy [1:0] value(1)	Symbol	Parameter	Conditions	Min	Max	Unit
x0	$f_{max(IO)out}$	Maximum frequency(3)	C_L = 50 pF, $V_{DDIOx} \geq 2$ V	-	2	MHz
	$t_{f(IO)out}$	Output fall time		-	125	ns
	$t_{r(IO)out}$	Output rise time		-	125	
	$f_{max(IO)out}$	Maximum frequency(3)	C_L = 50 pF, $V_{DDIOx} < 2$ V	-	1	MHz
	$t_{f(IO)out}$	Output fall time		-	125	ns
	$t_{r(IO)out}$	Output rise time		-	125	
01	$f_{max(IO)out}$	Maximum frequency(3)	C_L = 50 pF, $V_{DDIOx} \geq 2$ V	-	10	MHz
	$t_{f(IO)out}$	Output fall time		-	25	ns
	$t_{r(IO)out}$	Output rise time		-	25	
	$f_{max(IO)out}$	Maximum frequency(3)	C_L = 50 pF, $V_{DDIOx} < 2$ V	-	4	MHz
	$t_{f(IO)out}$	Output fall time		-	62.5	ns
	$t_{r(IO)out}$	Output rise time		-	62.5	
11	$f_{max(IO)out}$	Maximum frequency(3)	C_L = 30 pF, $V_{DDIOx} \geq 2.7$ V	-	50	MHz
			C_L = 50 pF, $V_{DDIOx} \geq 2.7$ V	-	30	
			C_L = 50 pF, 2 V ≤ V_{DDIOx} < 2.7 V	-	20	
			C_L = 50 pF, $V_{DDIOx} < 2$ V	-	10	
	$t_{f(IO)out}$	Output fall time	C_L = 30 pF, $V_{DDIOx} \geq 2.7$ V	-	5	ns
			C_L = 50 pF, $V_{DDIOx} \geq 2.7$ V	-	8	
			C_L = 50 pF, 2 V ≤ V_{DDIOx} < 2.7 V	-	12	
			C_L = 50 pF, $V_{DDIOx} < 2$ V	-	25	
	$t_{r(IO)out}$	Output rise time	C_L = 30 pF, $V_{DDIOx} \geq 2.7$ V	-	5	
			C_L = 50 pF, $V_{DDIOx} \geq 2.7$ V	-	8	
			C_L = 50 pF, 2 V ≤ V_{DDIOx} < 2.7 V	-	12	
			C_L = 50 pF, $V_{DDIOx} < 2$ V	-	25	

Table 53. NRST pin characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{IL(NRST)}$	NRST input low level voltage	-	-	-	0.3 V_{DD}+0.07(1)	V
$V_{IH(NRST)}$	NRST input high level voltage	-	0.445 V_{DD}+0.398(1)	-	-	
$V_{hys(NRST)}$	NRST Schmitt trigger voltage hysteresis	-	-	200	-	mV
R_{PU}	Weak pull-up equivalent resistor(2)	$V_{IN} = V_{SS}$	25	40	55	kΩ
$V_{F(NRST)}$	NRST input filtered pulse	-	-	-	100(1)	ns
$V_{NF(NRST)}$	NRST input not filtered pulse	-	700(1)	-	-	ns

1. Data based on design simulation only. Not tested in production.
2. The pull-up is designed with a true resistance in series with a switchable PMOS. This PMOS contribution to the series resistance is minimal (~10% order).

Figure 25. Recommended NRST pin protection



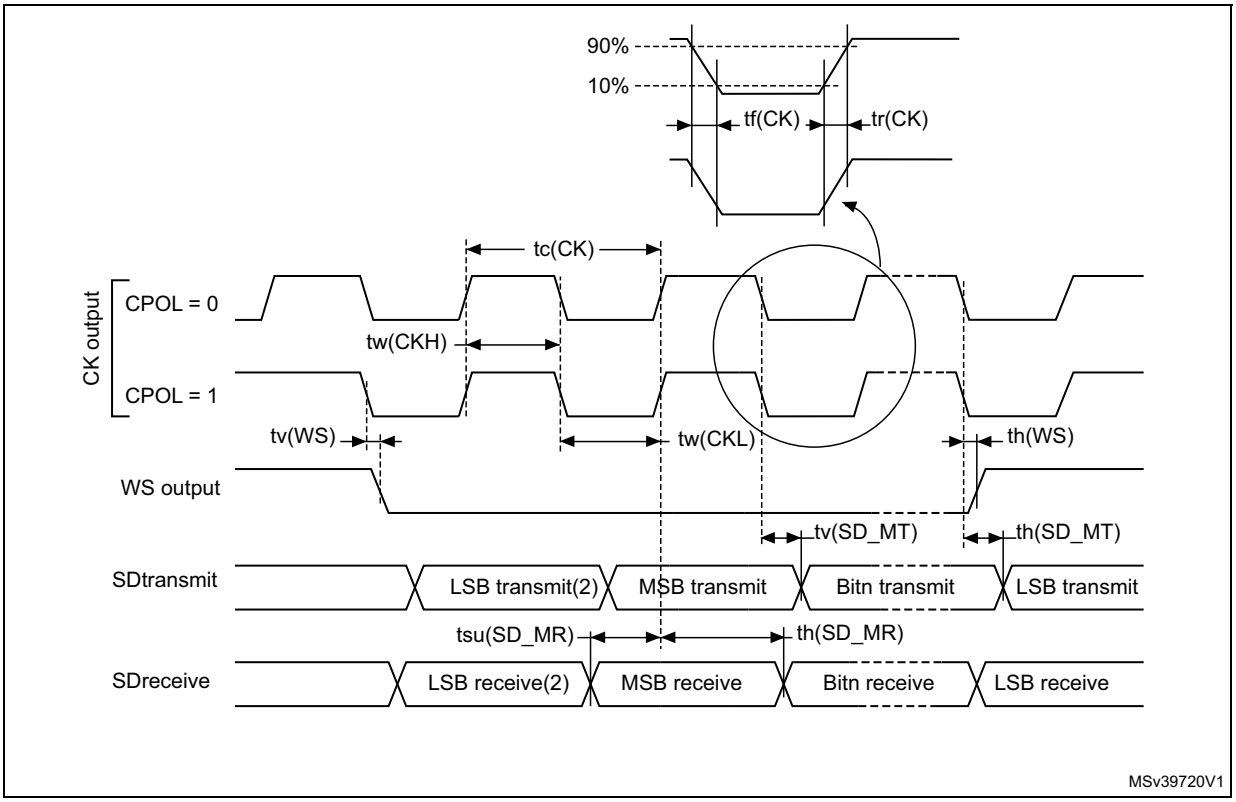
1. The external capacitor protects the device against parasitic resets.
2. The user must ensure that the level on the NRST pin can go below the $V_{IL(NRST)}$ max level specified in *Table 53: NRST pin characteristics*. Otherwise the reset will not be taken into account by the device.

NPOR pin characteristics

The NPOR pin input driver uses the CMOS technology. It is connected to a permanent pull-up resistor to the V_{DDA}, R_{PU}.

Unless otherwise specified, the parameters given in *Table 54* below are derived from tests performed under ambient temperature and supply voltage conditions summarized in *Table 23: General operating conditions*.

Figure 32. I²S master timing diagram (Philips protocol)



1. Data based on characterization results, not tested in production.
2. LSB transmit/receive of the previously transmitted byte. No LSB transmit/receive is sent before the first byte.

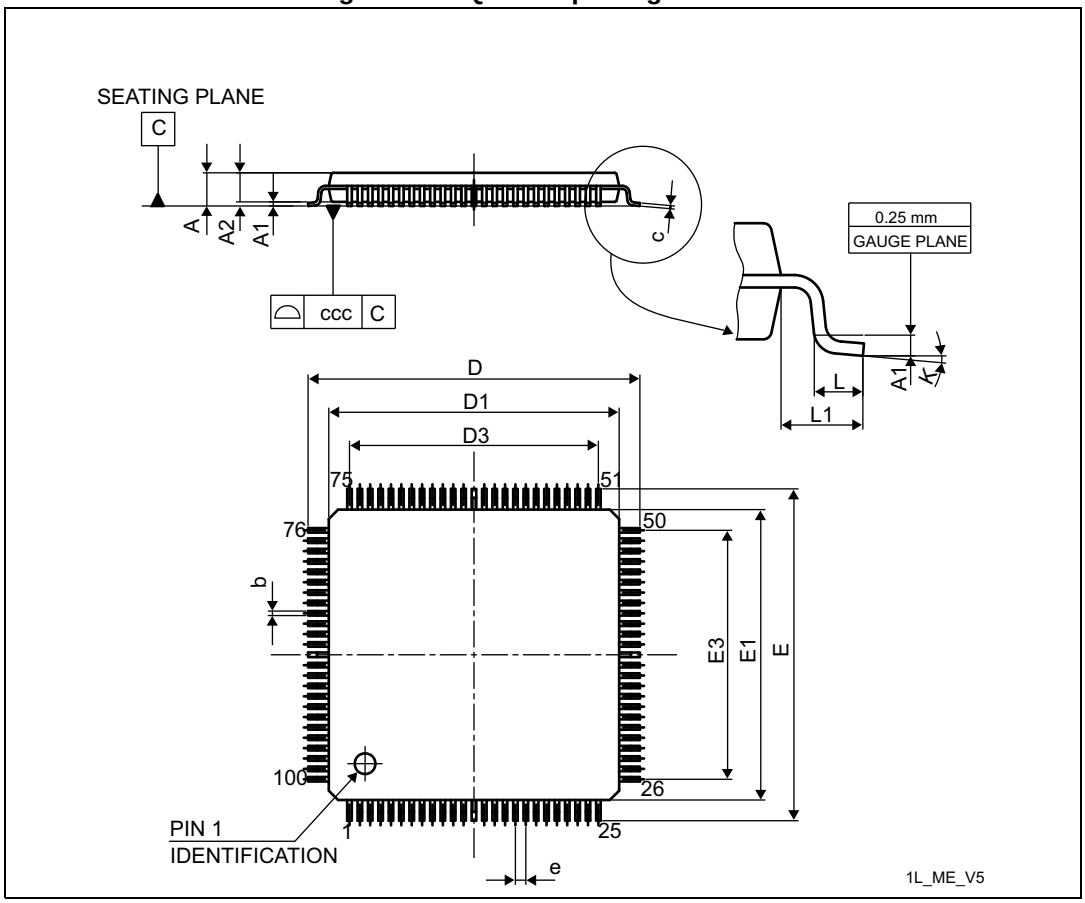
CAN (controller area network) interface

Refer to *Section 6.3.13: I/O port characteristics* for more details on the input/output alternate function characteristics (CAN_TX and CAN_RX).

7.2 LQFP100 package information

LQFP100 is a100-pin, 14 x 14 mm low-profile quad flat package.

Figure 36. LQFP100 package outline



1. Drawing is not to scale.

Table 70. LQPF100 package mechanical data

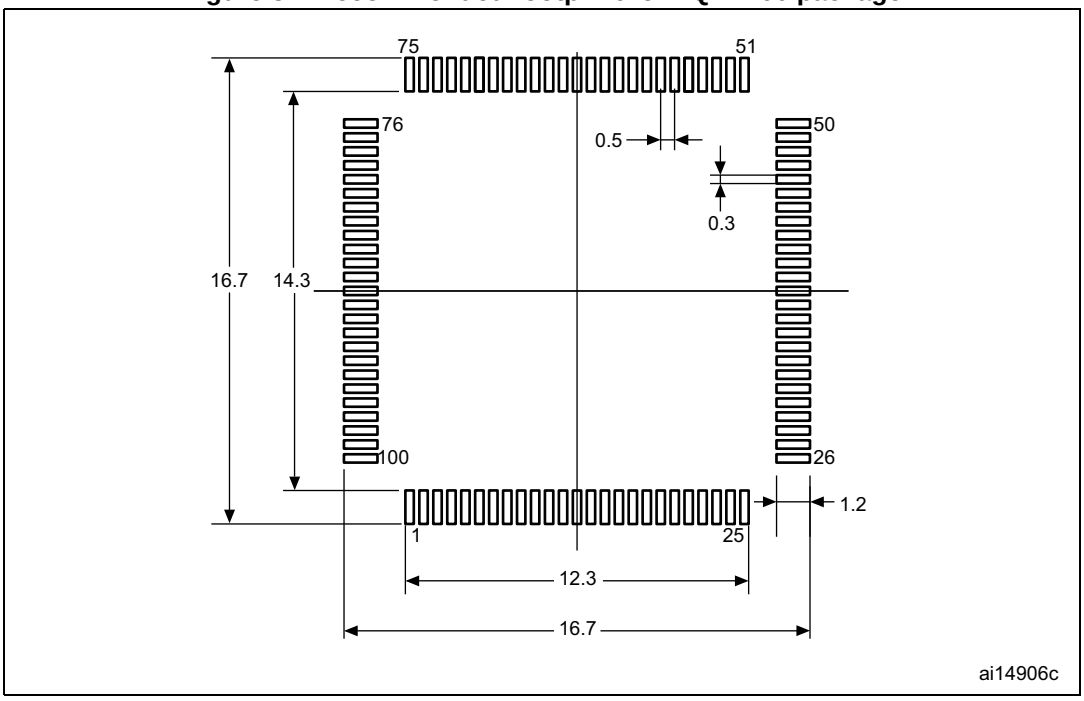
Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A	-	-	1.600	-	-	0.0630
A1	0.050	-	0.150	0.0020	-	0.0059
A2	1.350	1.400	1.450	0.0531	0.0551	0.0571
b	0.170	0.220	0.270	0.0067	0.0087	0.0106
c	0.090	-	0.200	0.0035	-	0.0079
D	15.800	16.000	16.200	0.6220	0.6299	0.6378
D1	13.800	14.000	14.200	0.5433	0.5512	0.5591
D3	-	12.000	-	-	0.4724	-
E	15.800	16.000	16.200	0.6220	0.6299	0.6378

Table 70. LQPF100 package mechanical data (continued)

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
E1	13.800	14.000	14.200	0.5433	0.5512	0.5591
E3	-	12.000	-	-	0.4724	-
e	-	0.500	-	-	0.0197	-
L	0.450	0.600	0.750	0.0177	0.0236	0.0295
L1	-	1.000	-	-	0.0394	-
k	0.0°	3.5°	7.0°	0.0°	3.5°	7.0°
ccc	-	-	0.080	-	-	0.0031

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Figure 37. Recommended footprint for LQFP100 package



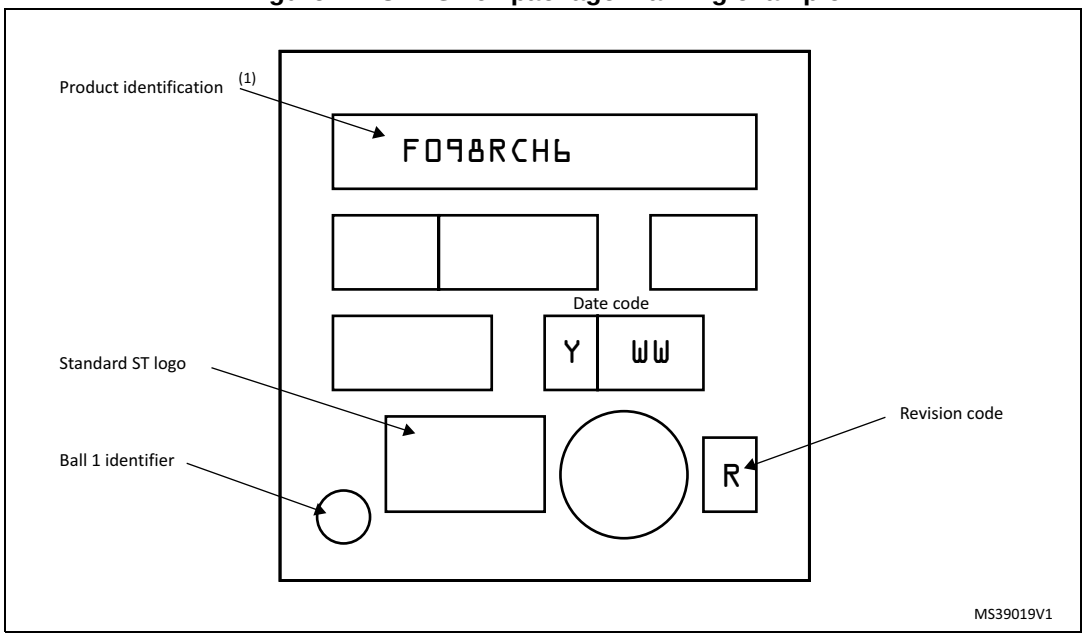
1. Dimensions are expressed in millimeters.

Device marking

The following figure gives an example of topside marking orientation versus ball A1 identifier location.

Other optional marking or inset/upset marks, which identify the parts throughout supply chain operations, are not indicated below.

Figure 41. UFBGA64 package marking example



1. Parts marked as "ES", "E" or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering Samples to run qualification activity.

7.8 Thermal characteristics

The maximum chip junction temperature ($T_J$max) must never exceed the values given in *Table 23: General operating conditions*.

The maximum chip-junction temperature, T_J max, in degrees Celsius, may be calculated using the following equation:

$$T_J \text{ max} = T_A \text{ max} + (P_D \text{ max} \times \Theta_{JA})$$

Where:

- T_A max is the maximum ambient temperature in °C,
- Θ_{JA} is the package junction-to-ambient thermal resistance, in °C/W,
- P_D max is the sum of P_{INT} max and $P_{I/O}$ max (P_D max = P_{INT} max + $P_{I/O}$max),
- P_{INT} max is the product of I_{DD} and V_{DD}, expressed in Watts. This is the maximum chip internal power.

$P_{I/O}$ max represents the maximum power dissipation on output pins where:

$$P_{I/O} \text{ max} = \Sigma (V_{OL} \times I_{OL}) + \Sigma ((V_{DDIOx} - V_{OH}) \times I_{OH}),$$

taking into account the actual V_{OL} / I_{OL} and V_{OH} / I_{OH} of the I/Os at low and high level in the application.

Table 78. Package thermal characteristics

Symbol	Parameter	Value	Unit
Θ_{JA}	**Thermal resistance junction-ambient** UFBGA100 - 7 × 7 mm	55	°C/W
	Thermal resistance junction-ambient LQFP100 - 14 × 14 mm	42	
	Thermal resistance junction-ambient UFBGA64 - 5 × 5 mm / 0.5 mm pitch	65	
	Thermal resistance junction-ambient LQFP64 - 10 × 10 mm / 0.5 mm pitch	44	
	Thermal resistance junction-ambient WLCSP64 - 0.4 mm pitch	53	
	Thermal resistance junction-ambient LQFP48 - 7 × 7 mm	54	
	Thermal resistance junction-ambient UFQFPN48 - 7 × 7 mm	32	

7.8.1 Reference document

JESD51-2 Integrated Circuits Thermal Test Method Environment Conditions - Natural Convection (Still Air). Available from www.jedec.org

7.8.2 Selecting the product temperature range

When ordering the microcontroller, the temperature range is specified in the ordering information scheme shown in *Section 8: Ordering information*.

9 Revision history

Table 80. Document revision history

Date	Revision	Changes
10-Nov-2014	1	Initial release.
19-Nov-2014	2	Updated: – *Section: Features* on the cover page: changed the number of capacitive sensing channels. – *Table: STM32F098xC family device features and peripheral counts*: changed the number of GPIOs and capacitive sensing channels.
17-Dec-2015	3	**Cover page:** – the document status to Datasheet - Production data – Fast Mode Plus current sink corrected from 20 mA to “extra” ***Section 2: Description*:** – *Table 1: STM32F098CC/RC/VC family device features and peripheral counts*- I/O and capacitive channel numbers corrected ***Section 3: Functional overview*:** – updated *Figure 1: Block diagram* (number of AF) and *Figure 2: Clock tree* – *Section 3.5.3: Low-power modes* - added info. on comm. peripherals configurable to operate with HSI – *Section 3.9.2: Extended interrupt/event controller (EXTI)* - number of GPIOs corrected – added number of complementary outputs for the general purpose and for the advance control timers in *Table 6: Timer feature comparison* – *Section 3.14.3: Basic timersTIM6 and TIM7* - corrected from plain text to numbered title ***Section 4: Pinouts and pin descriptions*:** – Package pinout figures updated (look and feel) – *Figure 7: WLCSP64 package pinout* - **now presented in top view** – *Table 12: STM32F098CC/RC/VC pin definitions* - MCO moved from additional to alternate functions column – *Table 14: Alternate functions selected through GPIOB_AFR registers for port B*- CAN_RX and CAN-TX added as AF4 for PB8 and PB9, respectively – *Table 18: Alternate functions selected through GPIOF_AFR registers for port F*- lines PF4 and PF5 removed ***Section 5: Memory mapping*:** – updated *Figure 10: STM32F098CC/RC/VC memory map*