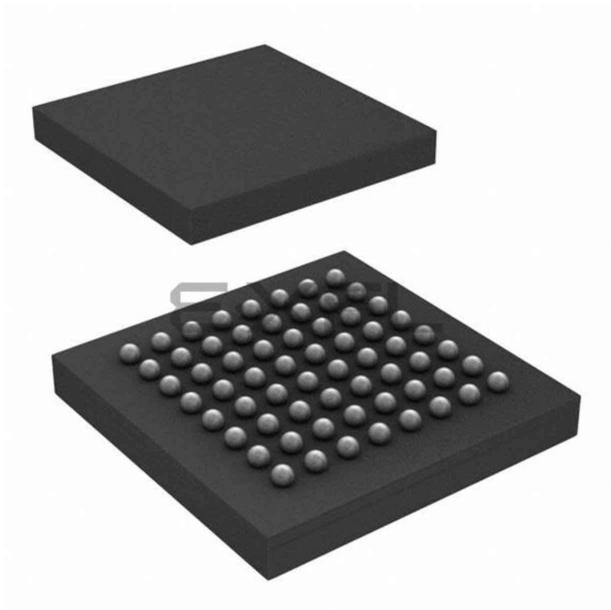

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M0
Core Size	32-Bit Single-Core
Speed	48MHz
Connectivity	CANbus, I²C, IrDA, LINbus, SPI, UART/USART
Peripherals	DMA, I²S, POR, PWM, WDT
Number of I/O	51
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	32K x 8
Voltage - Supply (Vcc/Vdd)	1.65V ~ 3.6V
Data Converters	A/D 19x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-UFBGA, WLCSP
Supplier Device Package	64-WLCSP (3.35x3.59)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32f098rcy6tr

introduced by the finger (or any conductive object) is measured using a proven implementation based on a surface charge transfer acquisition principle. It consists in charging the sensor capacitance and then transferring a part of the accumulated charges into a sampling capacitor until the voltage across this capacitor has reached a specific threshold. To limit the CPU bandwidth usage, this acquisition is directly managed by the hardware touch sensing controller and only requires few external components to operate. For operation, one capacitive sensing GPIO in each group is connected to an external capacitor and cannot be used as effective touch sensing channel.

The touch sensing controller is fully supported by the STMTouch touch sensing firmware library, which is free to use and allows touch sensing functionality to be implemented reliably in the end application.

Table 4. Capacitive sensing GPIOs available on STM32F098CC/RC/VC devices

Group	Capacitive sensing signal name	Pin name	Group	Capacitive sensing signal name	Pin name
1	TSC_G1_IO1	PA0	5	TSC_G5_IO1	PB3
	TSC_G1_IO2	PA1		TSC_G5_IO2	PB4
	TSC_G1_IO3	PA2		TSC_G5_IO3	PB6
	TSC_G1_IO4	PA3		TSC_G5_IO4	PB7
2	TSC_G2_IO1	PA4	6	TSC_G6_IO1	PB11
	TSC_G2_IO2	PA5		TSC_G6_IO2	PB12
	TSC_G2_IO3	PA6		TSC_G6_IO3	PB13
	TSC_G2_IO4	PA7		TSC_G6_IO4	PB14
3	TSC_G3_IO1	PC5	7	TSC_G7_IO1	PE2
	TSC_G3_IO2	PB0		TSC_G7_IO2	PE3
	TSC_G3_IO3	PB1		TSC_G7_IO3	PE4
4	TSC_G4_IO1	PA9		TSC_G7_IO4	PE5
	TSC_G4_IO2	PA10	8	TSC_G8_IO1	PD12
	TSC_G4_IO3	PA11		TSC_G8_IO2	PD13
	TSC_G4_IO4	PA12		TSC_G8_IO3	PD14
				TSC_G8_IO4	PD15

Table 5. Number of capacitive sensing channels available on STM32F098CC/RC/VC devices

Analog I/O group	Number of capacitive sensing channels		
	STM32F098Vx	STM32F098Rx	STM32F098Cx
G1	3	3	3
G2	3	3	3
G3	2	2	1
G4	3	3	3

verifications and ALERT protocol management. I2C1 also has a clock domain independent from the CPU clock, allowing the I2C1 to wake up the MCU from Stop mode on address match.

The I2C peripherals can be served by the DMA controller.

Refer to *Table 8* for the differences between I2C1 and I2C2.

Table 8. STM32F098CC/RC/VC I^2C implementation

I^2C features(1)	I2C1	I2C2
7-bit addressing mode	X	X
10-bit addressing mode	X	X
Standard mode (up to 100 kbit/s)	X	X
Fast mode (up to 400 kbit/s)	X	X
Fast Mode Plus (up to 1 Mbit/s) with extra output drive I/Os	X	X
Independent clock	X	-
SMBus	X	-
Wakeup from STOP	X	-

1. X = supported.

3.17 Universal synchronous/asynchronous receiver/transmitter (USART)

The device embeds up to eight universal synchronous/asynchronous receivers/transmitters (USART1, USART2, USART3, USART4, USART5, USART6, USART7, USART8) which communicate at speeds of up to 6 Mbit/s.

They provide hardware management of the CTS, RTS and RS485 DE signals, multiprocessor communication mode, master synchronous communication and single-wire half-duplex communication mode. USART1, USART2 and USART3 support also SmartCard communication (ISO 7816), IrDA SIR ENDEC, LIN Master/Slave capability and auto baud rate feature, and have a clock domain independent of the CPU clock, allowing to wake up the MCU from Stop mode.

The USART interfaces can be served by the DMA controller.

Table 9. STM32F098CC/RC/VC USART implementation

USART modes/features(1)	USART1 USART2 USART3	USART4	USART5 USART6 USART7 USART8
Hardware flow control for modem	X	X	-
Continuous communication using DMA	X	X	X
Multiprocessor communication	X	X	X
Synchronous mode	X	X	X
Smartcard mode	X	-	-

3.19 High-definition multimedia interface (HDMI) - consumer electronics control (CEC)

The device embeds a HDMI-CEC controller that provides hardware support for the Consumer Electronics Control (CEC) protocol (Supplement 1 to the HDMI standard).

This protocol provides high-level control functions between all audiovisual products in an environment. It is specified to operate at low speeds with minimum processing and memory overhead. It has a clock domain independent from the CPU clock, allowing the HDMI_CEC controller to wakeup the MCU from Stop mode on data reception.

3.20 Controller area network (CAN)

The CAN is compliant with specifications 2.0A and B (active) with a bit rate up to 1 Mbit/s. It can receive and transmit standard frames with 11-bit identifiers as well as extended frames with 29-bit identifiers. It has three transmit mailboxes, two receive FIFOs with 3 stages and 14 scalable filter banks.

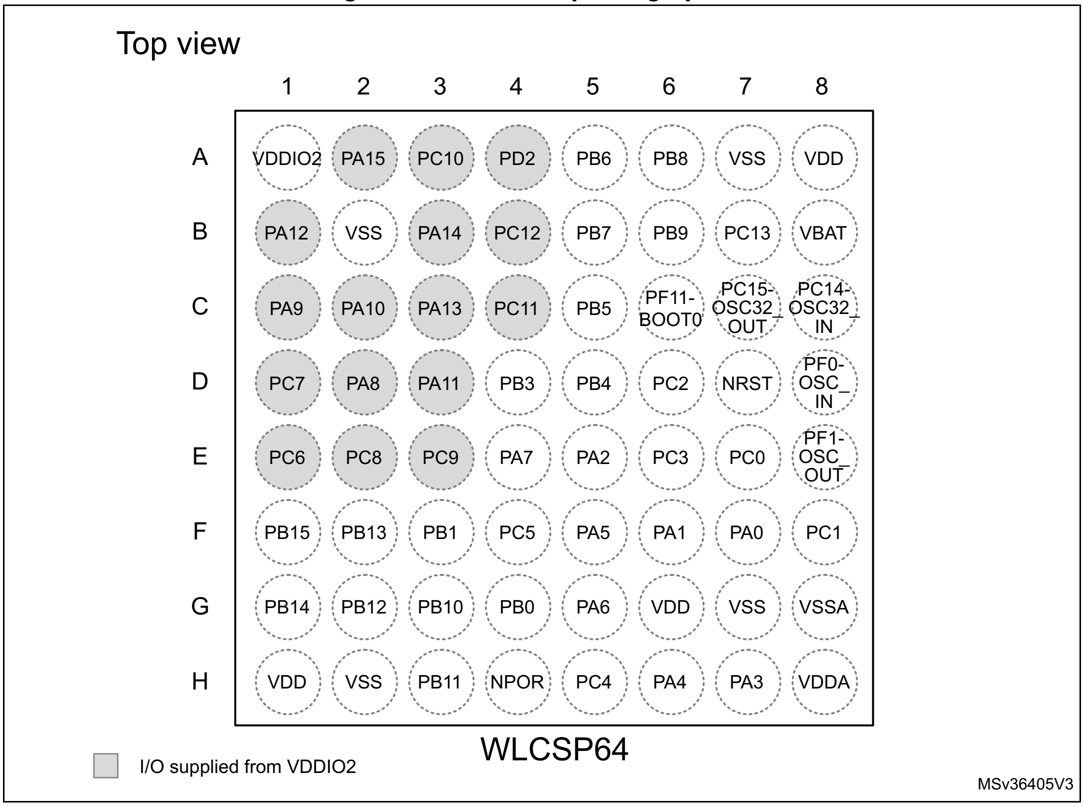
3.21 Clock recovery system (CRS)

The STM32F098CC/RC/VC embeds a special block which allows automatic trimming of the internal 48 MHz oscillator to guarantee its optimal accuracy over the whole device operational range. This automatic trimming is based on the external synchronization signal, which could be either derived from LSE oscillator, from an external signal on CRS_SYNC pin or generated by user software. For faster lock-in during startup it is also possible to combine automatic trimming with manual trimming action.

3.22 Serial wire debug port (SW-DP)

An ARM SW-DP interface is provided to allow a serial wire debugging tool to be connected to the MCU.

Figure 7. WLCSP64 package pinout



1. The above figure shows the package in top view, changing from bottom view in the previous document versions.

Figure 8. LQFP48 package pinout

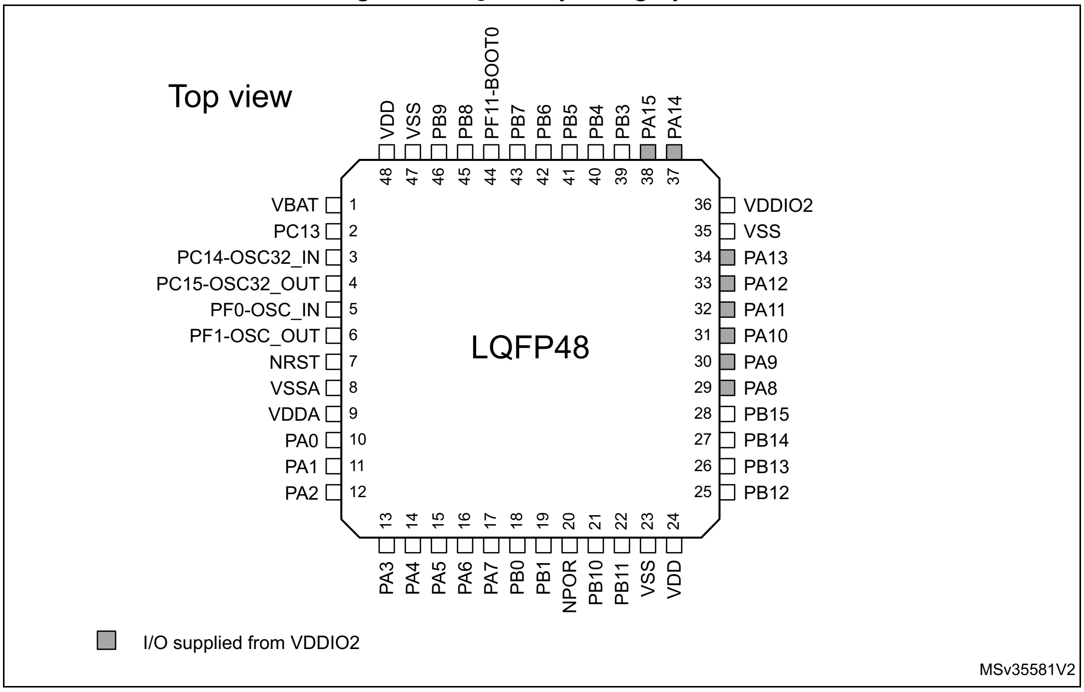


Figure 9. UFQFPN48 package pinout

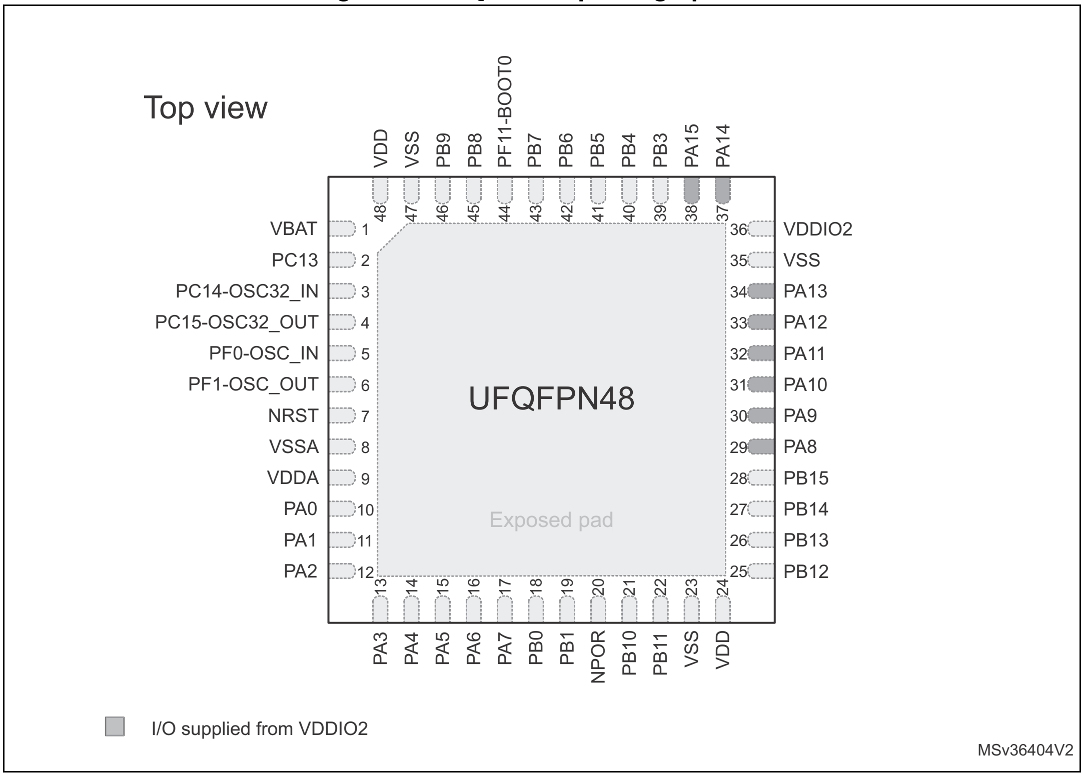


Table 11. Legend/abbreviations used in the pinout table

Name	Abbreviation	Definition
Pin name	Unless otherwise specified in brackets below the pin name, the pin function during and after reset is the same as the actual pin name	
Pin type	S	Supply pin
	I	Input-only pin
	I/O	Input / output pin
I/O structure	FT	5 V-tolerant I/O
	FTf	5 V-tolerant I/O, FM+ capable
	TTa	3.3 V-tolerant I/O directly connected to ADC
	POR	External power on reset pin with embedded weak pull-up resistor, powered from V_{DDA}
	TC	Standard 3.3 V I/O
	B	Dedicated BOOT0 pin
	RST	Bidirectional reset pin with embedded weak pull-up resistor
Notes	Unless otherwise specified by a note, all I/Os are set as floating inputs during and after reset.	

Table 15. Alternate functions selected through GPIOC_AFR registers for port C

Pin name	AF0	AF1	AF2
PC0	EVENTOUT	USART7_TX	USART6_TX
PC1	EVENTOUT	USART7_RX	USART6_RX
PC2	EVENTOUT	SPI2_MISO, I2S2_MCK	USART8_TX
PC3	EVENTOUT	SPI2_MOSI, I2S2_SD	USART8_RX
PC4	EVENTOUT	USART3_TX	-
PC5	TSC_G3_IO1	USART3_RX	-
PC6	TIM3_CH1	USART7_TX	-
PC7	TIM3_CH2	USART7_RX	-
PC8	TIM3_CH3	USART8_TX	-
PC9	TIM3_CH4	USART8_RX	-
PC10	USART4_TX	USART3_TX	-
PC11	USART4_RX	USART3_RX	-
PC12	USART4_CK	USART3_CK	USART5_TX
PC13	-	-	-
PC14	-	-	-
PC15	-	-	-

Table 16. Alternate functions selected through GPIOD_AFR registers for port D

Pin name	AF0	AF1	AF2
PD0	CAN_RX	SPI2_NSS, I2S2_WS	-
PD1	CAN_TX	SPI2_SCK, I2S2_CK	-
PD2	TIM3_ETR	USART3_RTS	USART5_RX
PD3	USART2_CTS	SPI2_MISO, I2S2_MCK	-
PD4	USART2_RTS	SPI2_MOSI, I2S2_SD	-
PD5	USART2_TX	-	-
PD6	USART2_RX	-	-
PD7	USART2_CK	-	-
PD8	USART3_TX	-	-
PD9	USART3_RX	-	-
PD10	USART3_CK	-	-
PD11	USART3_CTS	-	-
PD12	USART3_RTS	TSC_G8_IO1	USART8_CK_RTS
PD13	USART8_TX	TSC_G8_IO2	-
PD14	USART8_RX	TSC_G8_IO3	-
PD15	CRS_SYNC	TSC_G8_IO4	USART7_CK_RTS

On-chip peripheral current consumption

The current consumption of the on-chip peripherals is given in *Table 32*. The MCU is placed under the following conditions:

- All I/O pins are in analog mode
- All peripherals are disabled unless otherwise mentioned
- The given value is calculated by measuring the current consumption
  - with all peripherals clocked off
  - with only one peripheral clocked on
- Ambient operating temperature and supply voltage conditions summarized in *Table 20: Voltage characteristics*

Table 32. Peripheral current consumption

Peripheral		Typical consumption at 25 °C	Unit
AHB	BusMatrix(1)	3.1	µA/MHz
	CRC	2.0	
	DMA1	5.5	
	DMA2	5.1	
	Flash memory interface	15.4	
	GPIOA	5.5	
	GPIOB	5.4	
	GPIOC	3.2	
	GPIOD	3.1	
	GPIOE	4.0	
	GPIOF	2.5	
	SRAM	0.8	
	TSC	5.5	
	All AHB peripherals	**61.0**	

6.3.5 Wakeup time from low-power mode

The wakeup times given in *Table 33* are the latency between the event and the execution of the first user instruction. The device goes in low-power mode after the WFE (Wait For Event) instruction, in the case of a WFI (Wait For Interruption) instruction, 16 CPU cycles must be added to the following timings due to the interrupt latency in the Cortex M0 architecture.

The SYSCLK clock source setting is kept unchanged after wakeup from Sleep mode. During wakeup from Stop mode, SYSCLK takes the default setting: HSI 8 MHz.

The wakeup source from Sleep and Stop mode is an EXTI line configured in event mode.

All timings are derived from tests performed under the ambient temperature and supply voltage conditions summarized in *Table 23: General operating conditions*.

Table 33. Low-power mode wakeup timings

Symbol	Parameter	Typ @ V_{DDA}		Max	Unit
		= 1.8 V	= 3.3 V		
t_{WUSTOP}	Wakeup from Stop mode	3.5	2.8	5.3	µs
$t_{WUSLEEP}$	Wakeup from Sleep mode	4 SYSCLK cycles		-	µs

6.3.6 External clock source characteristics

High-speed external user clock generated from an external source

In bypass mode the HSE oscillator is switched off and the input pin is a standard GPIO.

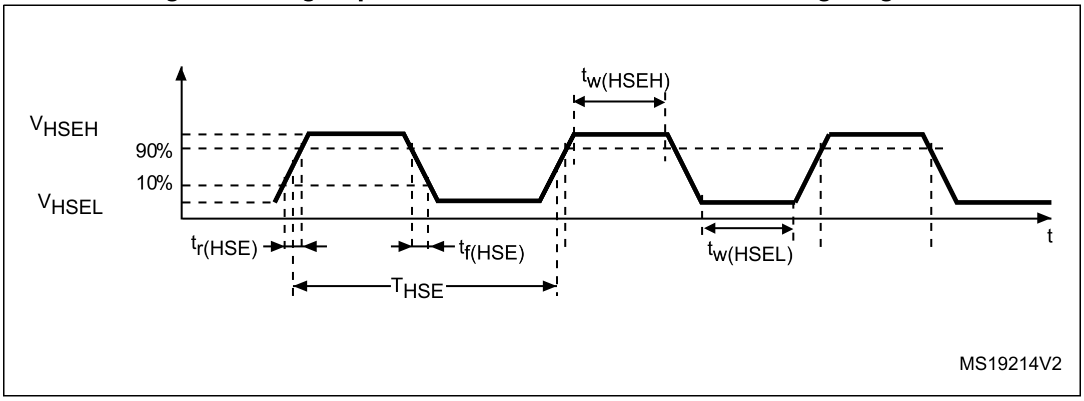
The external clock signal has to respect the I/O characteristics in *Section 6.3.13*. However, the recommended clock input waveform is shown in *Figure 15: High-speed external clock source AC timing diagram*.

Table 34. High-speed external user clock characteristics

Symbol	Parameter(1)	Min	Typ	Max	Unit
f_{HSE_ext}	User external clock source frequency	-	8	32	MHz
V_{HSEH}	OSC_IN input pin high level voltage	0.7 V_{DDIOx}	-	V_{DDIOx}	V
V_{HSEL}	OSC_IN input pin low level voltage	V_{SS}	-	0.3 V_{DDIOx}	V
$t_{w(HSEH)}$ $t_{w(HSEL)}$	OSC_IN high or low time	15	-	-	ns
$t_{r(HSE)}$ $t_{f(HSE)}$	OSC_IN rise or fall time	-	-	20	ns

1. Guaranteed by design, not tested in production.

Figure 15. High-speed external clock source AC timing diagram



Low-speed external user clock generated from an external source

In bypass mode the LSE oscillator is switched off and the input pin is a standard GPIO.

The external clock signal has to respect the I/O characteristics in *Section 6.3.13*. However, the recommended clock input waveform is shown in *Figure 16*.

Table 35. Low-speed external user clock characteristics

Symbol	Parameter(1)	Min	Typ	Max	Unit
f_{LSE_ext}	User external clock source frequency	-	32.768	1000	kHz
V_{LSEH}	OSC32_IN input pin high level voltage	0.7 V_{DDIOx}	-	V_{DDIOx}	V
V_{LSEL}	OSC32_IN input pin low level voltage	V_{SS}	-	0.3 V_{DDIOx}	
$t_{w(LSEH)}$ $t_{w(LSEL)}$	OSC32_IN high or low time	450	-	-	ns
$t_{r(LSE)}$ $t_{f(LSE)}$	OSC32_IN rise or fall time	-	-	50	

1. Guaranteed by design, not tested in production.

Figure 16. Low-speed external clock source AC timing diagram

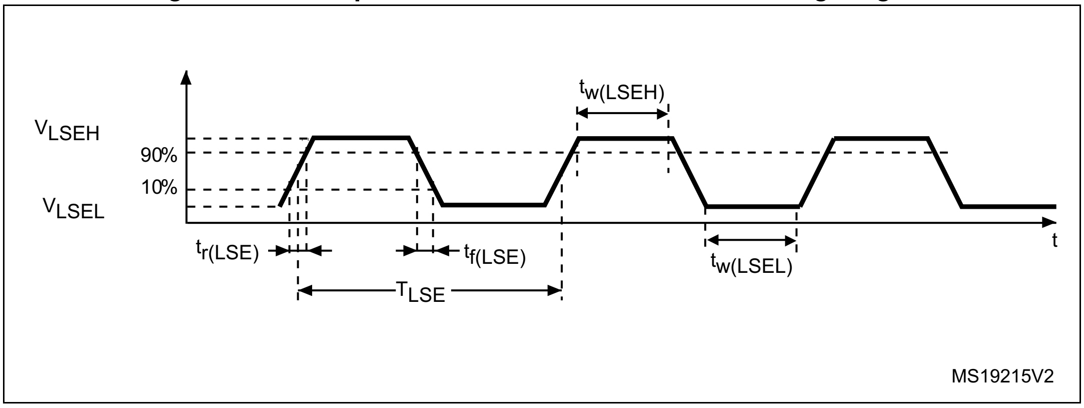
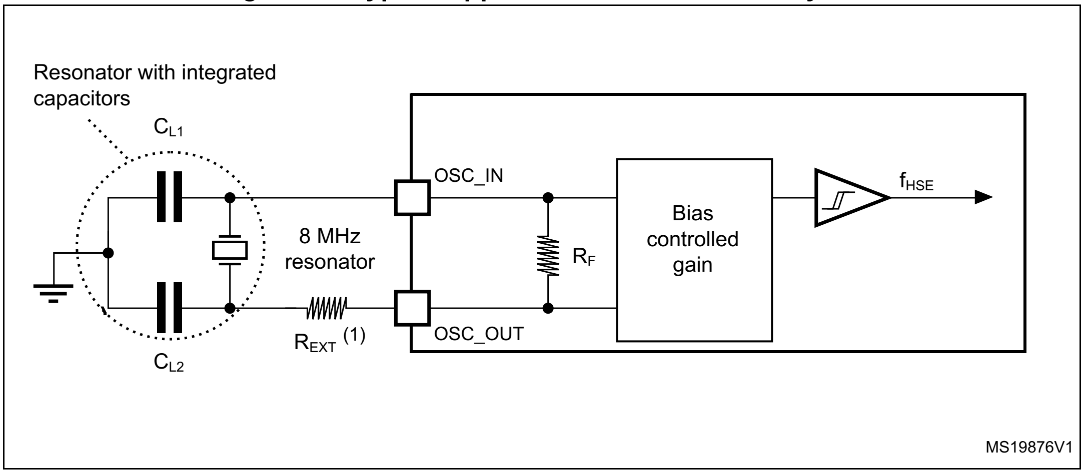


Figure 17. Typical application with an 8 MHz crystal



1. R_{EXT} value depends on the crystal characteristics.

Low-speed external clock generated from a crystal resonator

The low-speed external (LSE) clock can be supplied with a 32.768 kHz crystal resonator oscillator. All the information given in this paragraph are based on design simulation results obtained with typical external components specified in *Table 37*. In the application, the resonator and the load capacitors have to be placed as close as possible to the oscillator pins in order to minimize output distortion and startup stabilization time. Refer to the crystal resonator manufacturer for more details on the resonator characteristics (frequency, package, accuracy).

Table 37. LSE oscillator characteristics (f_{LSE} = 32.768 kHz)

Symbol	Parameter	Conditions[1]	Min[2]	Typ	Max[2]	Unit
I_{DD}	LSE current consumption	low drive capability	-	0.5	0.9	µA
		medium-low drive capability	-	-	1	
		medium-high drive capability	-	-	1.3	
		high drive capability	-	-	1.6	
g_m	Oscillator transconductance	low drive capability	5	-	-	µA/V
		medium-low drive capability	8	-	-	
		medium-high drive capability	15	-	-	
		high drive capability	25	-	-	
$t_{SU(LSE)}$[3]	Startup time	V_{DDIOx} is stabilized	-	2	-	s

1. Refer to the note and caution paragraphs below the table, and to the application note AN2867 “Oscillator design guide for ST microcontrollers”.
2. Guaranteed by design, not tested in production.
3. $t_{SU(LSE)}$ is the startup time measured from the moment it is enabled (by software) to a stabilized 32.768 kHz oscillation is reached. This value is measured for a standard crystal and it can vary significantly with the crystal manufacturer

Figure 22. TC and TTa I/O input characteristics

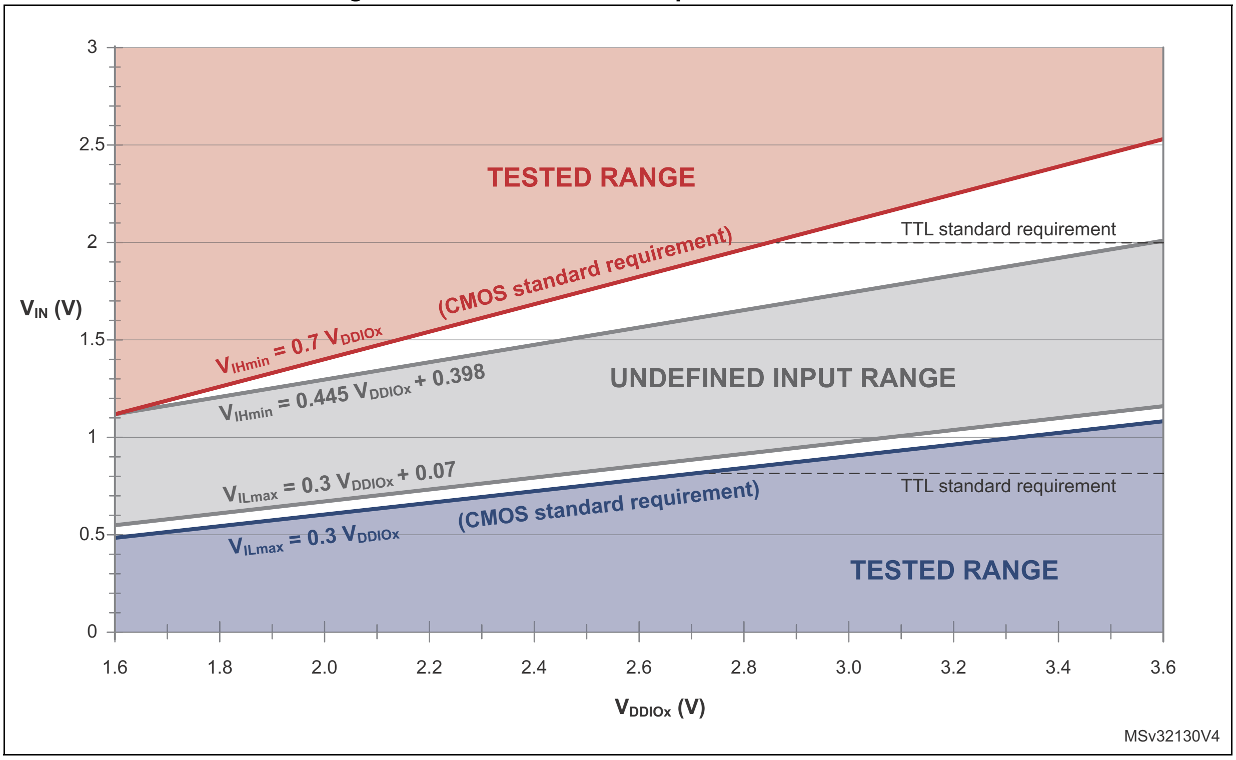


Figure 23. Five volt tolerant (FT and FTf) I/O input characteristics

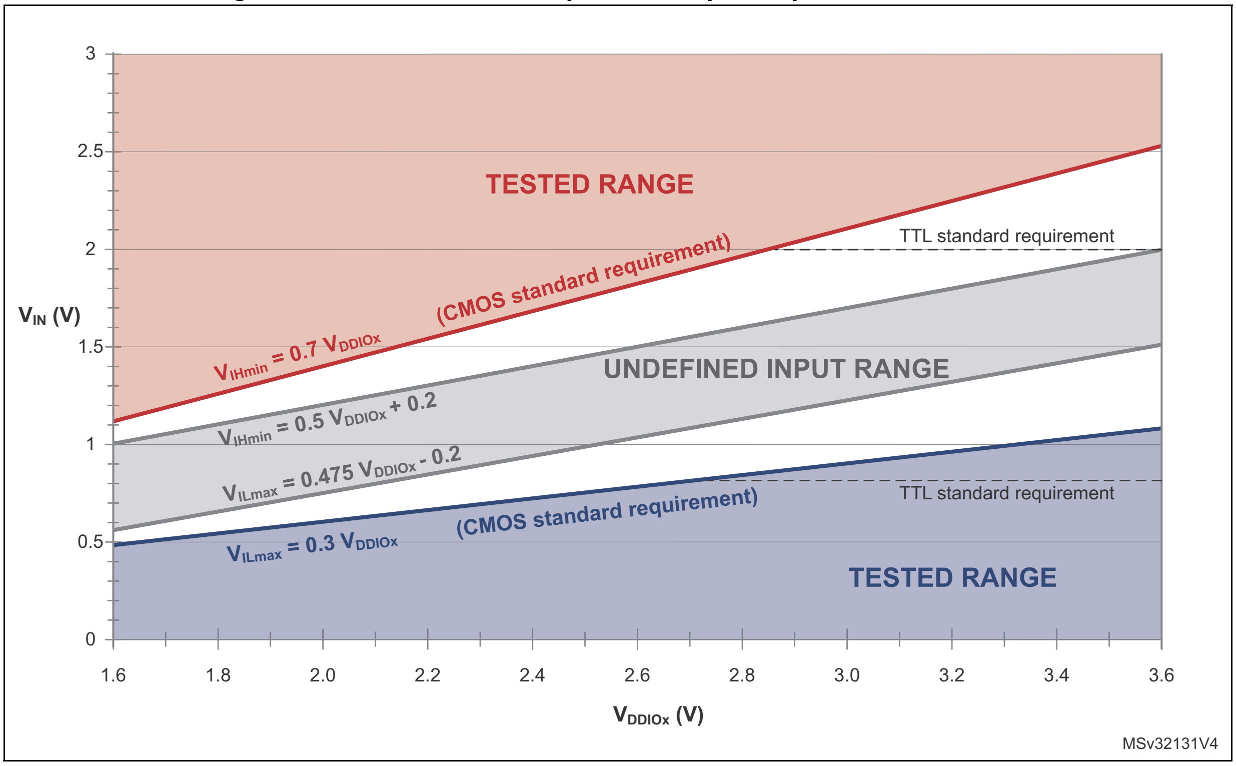


Table 54. NPOR pin characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{IL(NPOR)}$	NPOR Input low level voltage	-	-	-	0.475 V_{DDA} - 0.2(1)	V
$V_{IH(NPOR)}$	NPOR Input high level voltage	-	0.5 V_{DDA} + 0.2(1)	-	-	
$V_{hys(NPOR)}$	NPOR Schmitt trigger voltage hysteresis	-	-	100(1)	-	mV
R_{PU}	Weak pull-up equivalent resistor(2)	$V_{IN} = V_{SS}$	25	40	55	kΩ

1. Guaranteed by design, not tested in production.
2. The pull-up is designed with a true resistance in series with a switchable PMOS. This PMOS contribution to the series resistance is minimal (~10% order).

6.3.15 12-bit ADC characteristics

Unless otherwise specified, the parameters given in *Table 55* are derived from tests performed under the conditions summarized in *Table 23: General operating conditions*.

Note: It is recommended to perform a calibration after each power-up.

Table 55. ADC characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DDA}	Analog supply voltage for ADC ON	-	2.4	-	3.6	V
$I_{DDA (ADC)}$	Current consumption of the ADC(1)	V_{DDA} = 3.3 V	-	0.9	-	mA
f_{ADC}	ADC clock frequency	-	0.6	-	14	MHz
f_S(2)	Sampling rate	12-bit resolution	0.043	-	1	MHz
f_{TRIG}(2)	External trigger frequency	f_{ADC} = 14 MHz, 12-bit resolution	-	-	823	kHz
		12-bit resolution	-	-	17	$1/f_{ADC}$
V_{AIN}	Conversion voltage range	-	0	-	V_{DDA}	V
R_{AIN}(2)	External input impedance	See *Equation 1* and *Table 56* for details	-	-	50	kΩ
R_{ADC}(2)	Sampling switch resistance	-	-	-	1	kΩ
C_{ADC}(2)	Internal sample and hold capacitor	-	-	-	8	pF
t_{CAL}(2)(3)	Calibration time	f_{ADC} = 14 MHz	5.9			µs
		-	83			$1/f_{ADC}$

Table 56. R_{AIN} max for f_{ADC} = 14 MHz (continued)

T_S (cycles)	t_S (µs)	R_{AIN} max (kΩ)(1)
28.5	2.04	25.2
41.5	2.96	37.2
55.5	3.96	50
71.5	5.11	NA
239.5	17.1	NA

1. Guaranteed by design, not tested in production.

Table 57. ADC accuracy(1)(2)(3)

Symbol	Parameter	Test conditions	Typ	Max(4)	Unit
ET	Total unadjusted error	f_{PCLK} = 48 MHz, f_{ADC} = 14 MHz, R_{AIN} < 10 kΩ V_{DDA} = 3 V to 3.6 V T_A = 25 °C	±1.3	±2	LSB
EO	Offset error		±1	±1.5	
EG	Gain error		±0.5	±1.5	
ED	Differential linearity error		±0.7	±1	
EL	Integral linearity error		±0.8	±1.5	
ET	Total unadjusted error	f_{PCLK} = 48 MHz, f_{ADC} = 14 MHz, R_{AIN} < 10 kΩ V_{DDA} = 2.7 V to 3.6 V T_A = - 40 to 105 °C	±3.3	±4	LSB
EO	Offset error		±1.9	±2.8	
EG	Gain error		±2.8	±3	
ED	Differential linearity error		±0.7	±1.3	
EL	Integral linearity error		±1.2	±1.7	
ET	Total unadjusted error	f_{PCLK} = 48 MHz, f_{ADC} = 14 MHz, R_{AIN} < 10 kΩ V_{DDA} = 2.4 V to 3.6 V T_A = 25 °C	±3.3	±4	LSB
EO	Offset error		±1.9	±2.8	
EG	Gain error		±2.8	±3	
ED	Differential linearity error		±0.7	±1.3	
EL	Integral linearity error		±1.2	±1.7	

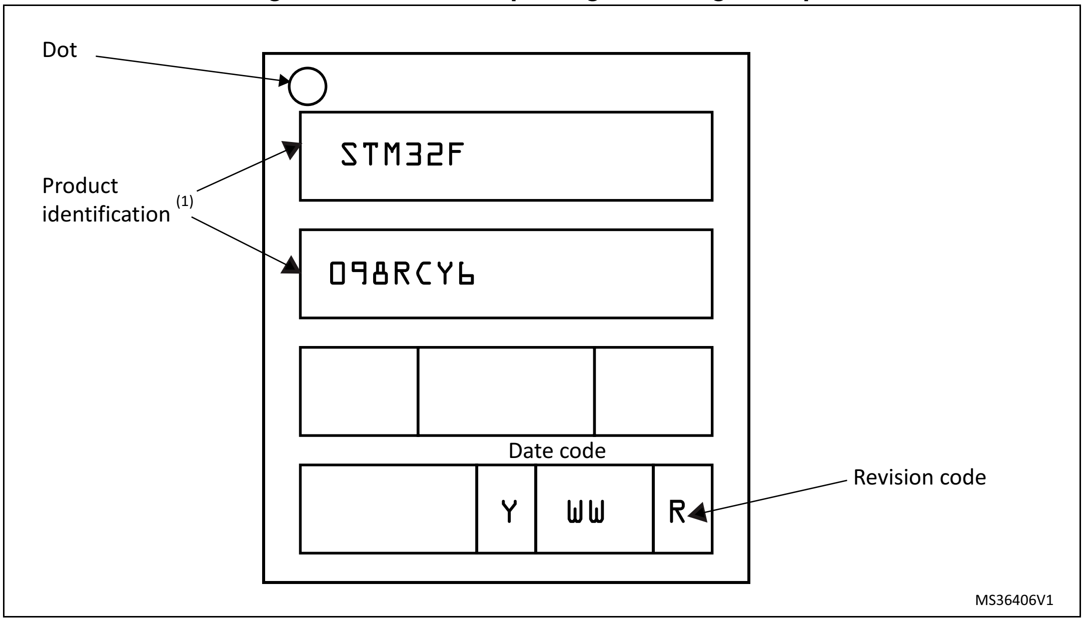
1. ADC DC accuracy values are measured after internal calibration.
2. ADC Accuracy vs. Negative Injection Current: Injecting negative current on any of the standard (non-robust) analog input pins should be avoided as this significantly reduces the accuracy of the conversion being performed on another analog input. It is recommended to add a Schottky diode (pin to ground) to standard analog pins which may potentially inject negative current.
Any positive injection current within the limits specified for $I_{INJ(PIN)}$ and $\Sigma I_{INJ(PIN)}$ in *Section 6.3.13* does not affect the ADC accuracy.
3. Better performance may be achieved in restricted V_{DDA}, frequency and temperature ranges.
4. Data based on characterization results, not tested in production.

Device marking

The following figure gives an example of topside marking orientation versus ball A1 identifier location.

Other optional marking or inset/upset marks, which identify the parts throughout supply chain operations, are not indicated below.

Figure 44. WLCSP64 package marking example

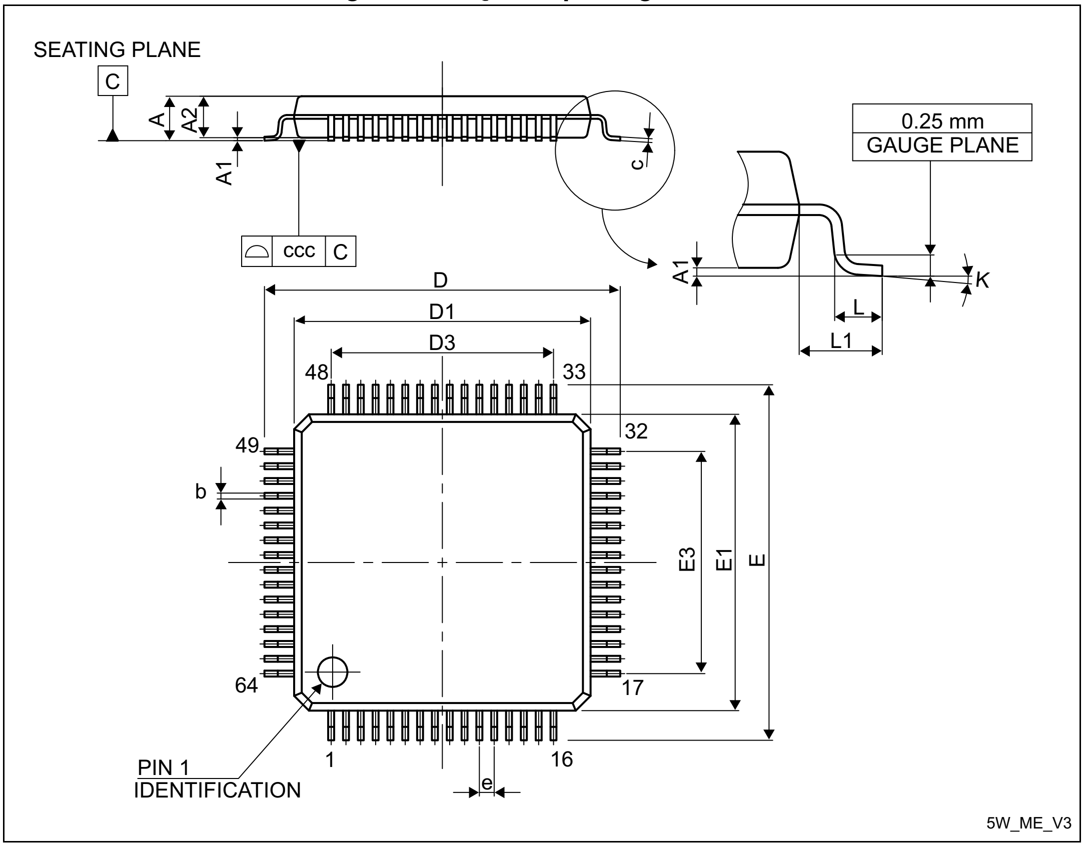


1. Parts marked as "ES", "E" or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering Samples to run qualification activity.

7.5 LQFP64 package information

LQFP64 is a 64-pin, 10 x 10 mm low-profile quad flat package.

Figure 45. LQFP64 package outline



1. Drawing is not to scale.

Table 75. LQFP64 package mechanical data

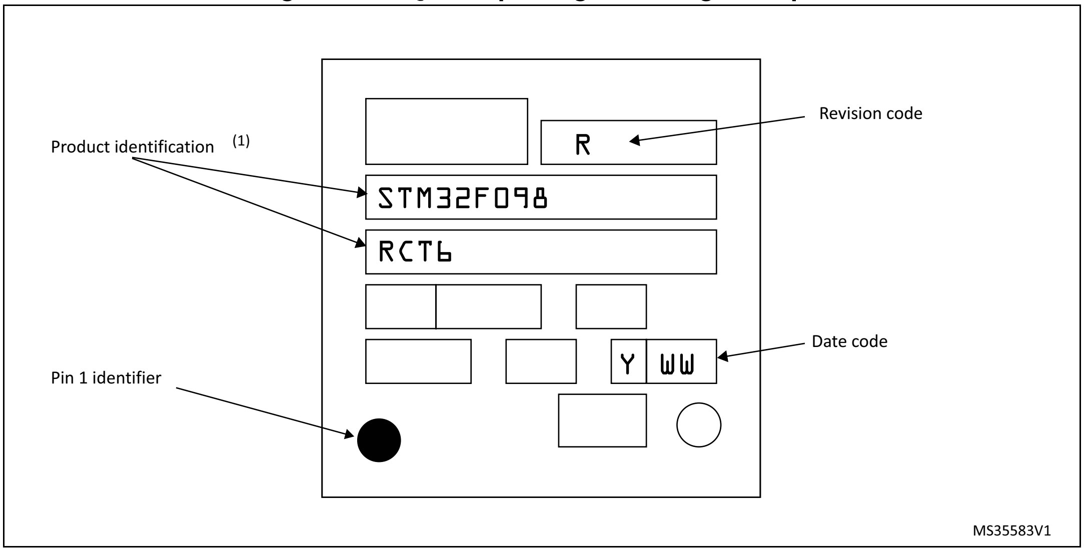
Symbol	millimeters			inches(1)		
	Min	Typ	Max	Min	Typ	Max
A	-	-	1.600	-	-	0.0630
A1	0.050	-	0.150	0.0020	-	0.0059
A2	1.350	1.400	1.450	0.0531	0.0551	0.0571
b	0.170	0.220	0.270	0.0067	0.0087	0.0106
c	0.090	-	0.200	0.0035	-	0.0079
D	-	12.000	-	-	0.4724	-
D1	-	10.000	-	-	0.3937	-
D3	-	7.500	-	-	0.2953	-
E	-	12.000	-	-	0.4724	-
E1	-	10.000	-	-	0.3937	-

Device marking

The following figure gives an example of topside marking orientation versus pin 1 identifier location.

Other optional marking or inset/upset marks, which identify the parts throughout supply chain operations, are not indicated below.

Figure 47. LQFP64 package marking example



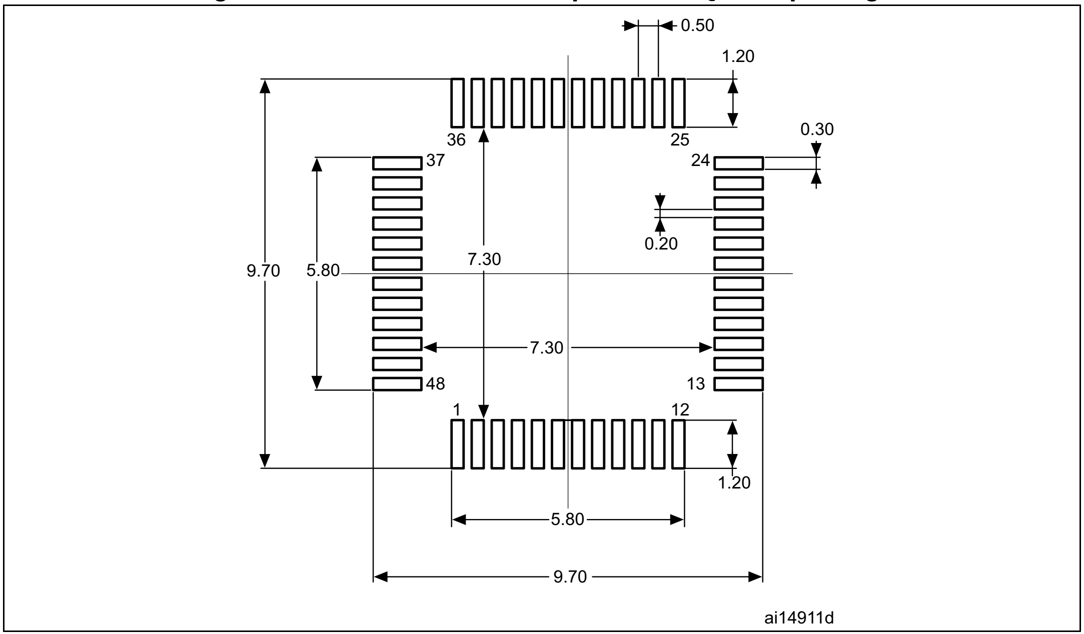
1. Parts marked as "ES", "E" or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering Samples to run qualification activity.

Table 76. LQFP48 package mechanical data

Symbol	millimeters			inches[(1)]		
	Min	Typ	Max	Min	Typ	Max
A	-	-	1.600	-	-	0.0630
A1	0.050	-	0.150	0.0020	-	0.0059
A2	1.350	1.400	1.450	0.0531	0.0551	0.0571
b	0.170	0.220	0.270	0.0067	0.0087	0.0106
c	0.090	-	0.200	0.0035	-	0.0079
D	8.800	9.000	9.200	0.3465	0.3543	0.3622
D1	6.800	7.000	7.200	0.2677	0.2756	0.2835
D3	-	5.500	-	-	0.2165	-
E	8.800	9.000	9.200	0.3465	0.3543	0.3622
E1	6.800	7.000	7.200	0.2677	0.2756	0.2835
E3	-	5.500	-	-	0.2165	-
e	-	0.500	-	-	0.0197	-
L	0.450	0.600	0.750	0.0177	0.0236	0.0295
L1	-	1.000	-	-	0.0394	-
k	0°	3.5°	7°	0°	3.5°	7°
ccc	-	-	0.080	-	-	0.0031

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Figure 49. Recommended footprint for LQFP48 package



1. Dimensions are expressed in millimeters.

7.8 Thermal characteristics

The maximum chip junction temperature ($T_J$max) must never exceed the values given in *Table 23: General operating conditions*.

The maximum chip-junction temperature, T_J max, in degrees Celsius, may be calculated using the following equation:

$$T_J \text{ max} = T_A \text{ max} + (P_D \text{ max} \times \Theta_{JA})$$

Where:

- T_A max is the maximum ambient temperature in °C,
- Θ_{JA} is the package junction-to-ambient thermal resistance, in °C/W,
- P_D max is the sum of P_{INT} max and $P_{I/O}$ max (P_D max = P_{INT} max + $P_{I/O}$max),
- P_{INT} max is the product of I_{DD} and V_{DD}, expressed in Watts. This is the maximum chip internal power.

$P_{I/O}$ max represents the maximum power dissipation on output pins where:

$P_{I/O}$ max = $\Sigma (V_{OL} \times I_{OL}) + \Sigma ((V_{DDIOx} - V_{OH}) \times I_{OH})$,

taking into account the actual V_{OL} / I_{OL} and V_{OH} / I_{OH} of the I/Os at low and high level in the application.

Table 78. Package thermal characteristics

Symbol	Parameter	Value	Unit
Θ_{JA}	**Thermal resistance junction-ambient** UFBGA100 - 7 × 7 mm	55	°C/W
	Thermal resistance junction-ambient LQFP100 - 14 × 14 mm	42	
	Thermal resistance junction-ambient UFBGA64 - 5 × 5 mm / 0.5 mm pitch	65	
	Thermal resistance junction-ambient LQFP64 - 10 × 10 mm / 0.5 mm pitch	44	
	Thermal resistance junction-ambient WLCSP64 - 0.4 mm pitch	53	
	Thermal resistance junction-ambient LQFP48 - 7 × 7 mm	54	
	Thermal resistance junction-ambient UFQFPN48 - 7 × 7 mm	32	

7.8.1 Reference document

JESD51-2 Integrated Circuits Thermal Test Method Environment Conditions - Natural Convection (Still Air). Available from www.jedec.org

7.8.2 Selecting the product temperature range

When ordering the microcontroller, the temperature range is specified in the ordering information scheme shown in *Section 8: Ordering information*.

Each temperature range suffix corresponds to a specific guaranteed ambient temperature at maximum dissipation and, to a specific maximum junction temperature.

As applications do not commonly use the STM32F098CC/RC/VC at maximum dissipation, it is useful to calculate the exact power consumption and junction temperature to determine which temperature range will be best suited to the application.

The following examples show how to calculate the temperature range needed for a given application.

Example 1: High-performance application

Assuming the following application conditions:

Maximum temperature T_{Amax} = 82 °C (measured according to JESD51-2), I_{DDmax} = 50 mA, V_{DD} = 3.5 V, maximum 20 I/Os used at the same time in output at low level with I_{OL} = 8 mA, V_{OL}= 0.4 V and maximum 8 I/Os used at the same time in output at low level with I_{OL} = 20 mA, V_{OL}= 1.3 V

P_{INTmax} = 50 mA × 3.5 V= 175 mW

P_{IOmax} = 20 × 8 mA × 0.4 V + 8 × 20 mA × 1.3 V = 272 mW

This gives: P_{INTmax} = 175 mW and P_{IOmax} = 272 mW:

P_{Dmax} = 175 + 272 = 447 mW

Using the values obtained in *Table 78* T_{Jmax} is calculated as follows:

– For LQFP64, 45 °C/W

T_{Jmax} = 82 °C + (45 °C/W × 447 mW) = 82 °C + 20.115 °C = 102.115 °C

This is within the range of the suffix 6 version parts (–40 < T_J < 105 °C).

In this case, parts must be ordered at least with the temperature range suffix 6 (see *Section 8: Ordering information*).

Note: With this given P_{Dmax} we can find the T_{Amax} allowed for a given device temperature range (order code suffix 6 or 7).

Suffix 6: T_{Amax} = T_{Jmax} - (45°C/W × 447 mW) = 105-20.115 = 84.885 °C

Suffix 7: T_{Amax} = T_{Jmax} - (45°C/W × 447 mW) = 125-20.115 = 104.885 °C

Example 2: High-temperature application

Using the same rules, it is possible to address applications that run at high temperatures with a low dissipation, as long as junction temperature T_J remains within the specified range.

Assuming the following application conditions:

Maximum temperature T_{Amax} = 100 °C (measured according to JESD51-2), I_{DDmax} = 20 mA, V_{DD} = 3.5 V, maximum 20 I/Os used at the same time in output at low level with I_{OL} = 8 mA, V_{OL}= 0.4 V

P_{INTmax} = 20 mA × 3.5 V= 70 mW

P_{IOmax} = 20 × 8 mA × 0.4 V = 64 mW

This gives: P_{INTmax} = 70 mW and P_{IOmax} = 64 mW:

P_{Dmax} = 70 + 64 = 134 mW

Thus: P_{Dmax} = 134 mW

Table 80. Document revision history (continued)

Date	Revision	Changes
10-Jan-2017	4	***Section 6: Electrical characteristics***: – *Table 37: LSE oscillator characteristics (f_{LSE} = 32.768 kHz)* - information on configuring different drive capabilities removed. See the corresponding reference manual. – *Table 25: Embedded internal reference voltage* - V_{REFINT} values – *Table 58: DAC characteristics* - min. R_{LOAD} to V_{DDA} defined – *Figure 28: SPI timing diagram - slave mode and CPHA = 0* and *Figure 29: SPI timing diagram - slave mode and CPHA = 1* enhanced and corrected ***Section 8: Ordering information***: – The name of the section changed from the previous “Part numbering”