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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Discontinued at Digi-Key
Core Processor	ARM® Cortex®-M3
Core Size	32-Bit Single-Core
Speed	100MHz
Connectivity	CANbus, I²C, IrDA, Microwire, SPI, SSI, SSP, UART/USART, USB
Peripherals	Brown-out Detect/Reset, DMA, Motor Control PWM, POR, PWM, WDT
Number of I/O	52
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	2.4V ~ 3.6V
Data Converters	A/D 6x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	80-LQFP
Supplier Device Package	80-LQFP (12x12)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/lpc1751fbd80-551

- Eight channel General Purpose DMA controller (GPDMA) on the AHB multilayer matrix that can be used with the SSP, I^2S-bus, UART, the Analog-to-Digital and Digital-to-Analog converter peripherals, timer match signals, and for memory-to-memory transfers.
- Multilayer AHB matrix interconnect provides a separate bus for each AHB master. AHB masters include the CPU, General Purpose DMA controller, Ethernet MAC (LPC1758 only), and the USB interface. This interconnect provides communication with no arbitration delays.
- Split APB bus allows high throughput with few stalls between the CPU and DMA.
- Serial interfaces:
  - On the LPC1758 only, Ethernet MAC with RMII interface and dedicated DMA controller.
  - USB 2.0 full-speed device/Host/OTG controller with dedicated DMA controller and on-chip PHY for device, Host, and OTG functions. The LPC1752/51 include a USB device controller only.
  - Four UARTs with fractional baud rate generation, internal FIFO, and DMA support. One UART has modem control I/O and RS-485/EIA-485 support, and one UART has IrDA support.
  - CAN 2.0B controller with two (LPC1759/58/56) or one (LPC1754/52/51) channels.
  - SPI controller with synchronous, serial, full duplex communication and programmable data length.
  - Two SSP controllers with FIFO

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4. Ordering information

Table 1. Ordering information

Type number	Package		
	Name	Description	Version
LPC1759FBD80	LQFP80	plastic low-profile quad package; 80 leads; body 12 u12 u1.4 mm	SOT315-1
LPC1758FBD80	LQFP80	plastic low-profile quad package; 80 leads; body 12 u12 u1.4 mm	SOT315-1
LPC1756FBD80	LQFP80	plastic low-profile quad package; 80 leads; body 12 u12 u1.4 mm	SOT315-1
LPC1754FBD80	LQFP80	plastic low-profile quad package; 80 leads; body 12 u12 u1.4 mm	SOT315-1
LPC1752FBD80	LQFP80	plastic low-profile quad package; 80 leads; body 12 u12 u1.4 mm	SOT315-1
LPC1751FBD80	LQFP80	plastic low-profile quad package; 80 leads; body 12 u12 u1.4 mm	SOT315-1

4.1 Ordering options

Table 2. Ordering options

Type number	Device order part number	Flash (kB)	SRAM in kB				Ethernet	USB	CAN	I^2S-bus	DAC	GPIO	Maximum CPU operating frequency (MHz)
			CPU	AHB SRAM0	AHB SRAM1	Total							
LPC1759FBD80	LPC1759FBD80,551	512	32	16	16	64	no	Device/Host/OTG	2	yes	yes	52	120
LPC1758FBD80	LPC1758FBD80Y	512	32	16	16	64	yes	Device/Host/OTG	2	yes	yes	52	100
LPC1756FBD80	LPC1756FBD80/CP327	256	16	16	-	32	no	Device/Host/OTG	2	yes	yes	52	100
LPC1754FBD80	LPC1754FBD80,551	128	16	16	-	32	no	Device/Host/OTG	1	no	yes	52	100
LPC1752FBD80	LPC1752FBD80,551	64	16	-	-	16	no	Device only	1	no	no	52	100
LPC1751FBD80	LPC1751FBD80,551	32	8	-	-	8	no	Device only	1	no	no	52	100

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7. Pinning information

7.1 Pinning

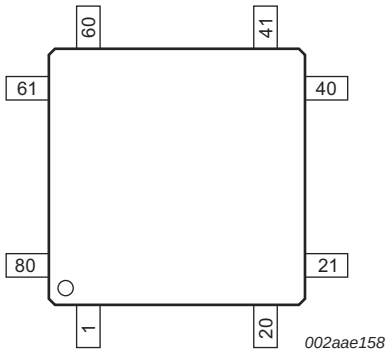

Fig 2. Pin configuration LQFP80 package

7.2 Pin description

Table 4. Pin description

Symbol	Pin	Type	Description
P0[0] to P0[31]		I/O	Port 0: Port 0 is a 32-bit I/O port with individual direction controls for each bit. The operation of Port 0 pins depends upon the pin function selected via the pin connect block. Some port pins are not available on the LQFP80 package.
P0[0]/RD1/TXD3/ SDA1	37[1]	I/O	P0[0] — General purpose digital input/output pin.
		I	RD1 — CAN1 receiver input.
		O	TXD3 — Transmitter output for UART3.
		I/O	SDA1 — I^2C1 data input/output (this is not an I^2C-bus compliant open-drain pin).
P0[1]/TD1/RXD3/ SCL1	38[1]	I/O	P0[1] — General purpose digital input/output pin.
		O	TD1 — CAN1 transmitter output.
		I	RXD3 — Receiver input for UART3.
		I/O	SCL1 — I^2C1 clock input/output (this is not an I^2C-bus compliant open-drain pin).
P0[2]/TXD0/AD0[7]	79[2]	I/O	P0[2] — General purpose digital input/output pin.
		O	TXD0 — Transmitter output for UART0.
		I	AD0[7] — A/D converter 0, input 7.
P0[3]/RXD0/AD0[6]	80[2]	I/O	P0[3] — General purpose digital input/output pin.
		I	RXD0 — Receiver input for UART0.
		I	AD0[6] — A/D converter 0, input 6.
P0[6]/ I2SRX_SDA/ SSEL1/MAT2[0]	64[1]	I/O	P0[6] — General purpose digital input/output pin.
		I/O	I2SRX_SDA — Receive data. It is driven by the transmitter and read by the receiver. Corresponds to the signal SD in the I^2S-bus specification. (LPC1759/58/56 only).
		I/O	SSEL1 — Slave Select for SSP1.
		O	MAT2[0] — Match output for Timer 2, channel 0.

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- While USB is in the Suspend mode, the LPC1759/58/56/54/52/51 can enter one of the reduced power modes and wake up on USB activity.
- Supports DMA transfers with all on-chip SRAM blocks on all non-control endpoints.
- Allows dynamic switching between CPU-controlled slave and DMA modes.
- Double buffer implementation for Bulk and Isochronous endpoints.

8.12.2 USB host controller (LPC1759/58/56/54 only).

The host controller enables full- and low-speed data exchange with USB devices attached to the bus. It consists of a register interface, a serial interface engine, and a DMA controller. The register interface complies with the Open Host Controller Interface (OHCI) specification.

8.12.2.1 Features

- OHCI compliant.
- One downstream port.
- Supports port power switching.

8.12.3 USB OTG controller (LPC1759/58/56/54 only).

USB OTG is a supplement to the USB 2.0 specification that augments the capability of existing mobile devices and USB peripherals by adding host functionality for connection to USB peripherals.

The OTG Controller integrates the host controller, device controller, and a master-only I^2C-bus interface to implement OTG dual-role device functionality. The dedicated I^2C-bus interface controls an external OTG transceiver.

8.12.3.1 Features

- Fully compliant with On-The-Go supplement to the USB 2.0 Specification, Revision 1.0a.
- Hardware support for Host Negotiation Protocol (HNP).
- Includes a programmable timer required for HNP and Session Request Protocol (SRP).
- Supports any OTG transceiver compliant with the OTG Transceiver Specification (CEA-2011), Rev. 1.0.

8.13 CAN controller and acceptance filters

The Controller Area Network (CAN) is a serial communications protocol which efficiently supports distributed real-time control with a very high level of security. Its domain of application ranges from high-speed networks to low cost multiplex wiring.

The CAN block is intended to support multiple CAN buses simultaneously, allowing the device to be used as a gateway, switch, or router among a number of CAN buses in industrial or automotive applications.

Remark: LPC1754/52/51 have only one CAN bus.

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8.16 UARTs

The LPC1759/58/56/54/52/51 each contain four UARTs. In addition to standard transmit and receive data lines, UART1 also provides a full modem control handshake interface and support for RS-485/9-bit mode allowing both software address detection and automatic address detection using 9-bit mode.

The UARTs include a fractional baud rate generator. Standard baud rates such as 115200 Bd can be achieved with any crystal frequency above 2 MHz.

8.16.1 Features

- Maximum UART data bit rate of 6.25 Mbit/s.
- 16 B Receive and Transmit FIFOs.
- Register locations conform to 16C550 industry standard.
- Receiver FIFO trigger points at 1 B, 4 B, 8 B, and 14 B.
- Built-in fractional baud rate generator covering wide range of baud rates without a need for external crystals of particular values.
- Fractional divider for baud rate control, auto baud capabilities and FIFO control mechanism that enables software flow control implementation.
- UART1 equipped with standard modem interface signals. This module also provides full support for hardware flow control (auto-CTS/RTS).
- Support for RS-485/9-bit/EIA-485 mode (UART1).
- UART3 includes an IrDA mode to support infrared communication.
- All UARTs have DMA support.

8.17 SPI serial I/O controller

The LPC1759/58/56/54/52/51 contain one SPI controller. SPI is a full duplex serial interface designed to handle multiple masters and slaves connected to a given bus. Only a single master and a single slave can communicate on the interface during a given data transfer. During a data transfer the master always sends 8 bits to 16 bits of data to the slave, and the slave always sends 8 bits to 16 bits of data to the master.

8.17.1 Features

- Maximum SPI data bit rate of 12.5 Mbit/s
- Compliant with SPI specification
- Synchronous, serial, full duplex communication
- Combined SPI master and slave
- Maximum data bit rate of one eighth of the input clock rate
- 8 bits to 16 bits per transfer

8.18 SSP serial I/O controller

The LPC1759/58/56/54/52/51 contain two SSP controllers. The SSP controller is capable of operation on a SPI, 4-wire SSI, or Microwire bus. It can interact with multiple masters and slaves on the bus. Only a single master and a single slave can communicate on the

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12.8 USB interface

Table 16. Dynamic characteristics: USB pins (full-speed)
C_L = 50 pF; R_{pu} = 1.5 kΩ on D+ to $V_{DD(3V3)}$; 3.0 V ≤ $V_{DD(3V3)}$ ≤ 3.6 V.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
t_r	rise time	10 % to 90 %		8.5	-	13.8	ns
t_f	fall time	10 % to 90 %		7.7	-	13.7	ns
t_{FRFM}	differential rise and fall time matching	t_r / t_f		-	-	109	%
V_{CRS}	output signal crossover voltage			1.3	-	2.0	V
t_{FEOPT}	source SE0 interval of EOP	see Figure 21		160	-	175	ns
t_{FDEOP}	source jitter for differential transition to SE0 transition	see Figure 21		2	-	+5	ns
t_{JR1}	receiver jitter to next transition			18.5	-	+18.5	ns
t_{JR2}	receiver jitter for paired transitions	10 % to 90 %		9	-	+9	ns
t_{EOPR1}	EOP width at receiver	must reject as EOP; see Figure 21	[1]	40	-	-	ns
t_{EOPR2}	EOP width at receiver	must accept as EOP; see Figure 21	[1]	82	-	-	ns

[1] Characterized but not implemented as production test. Guaranteed by design.

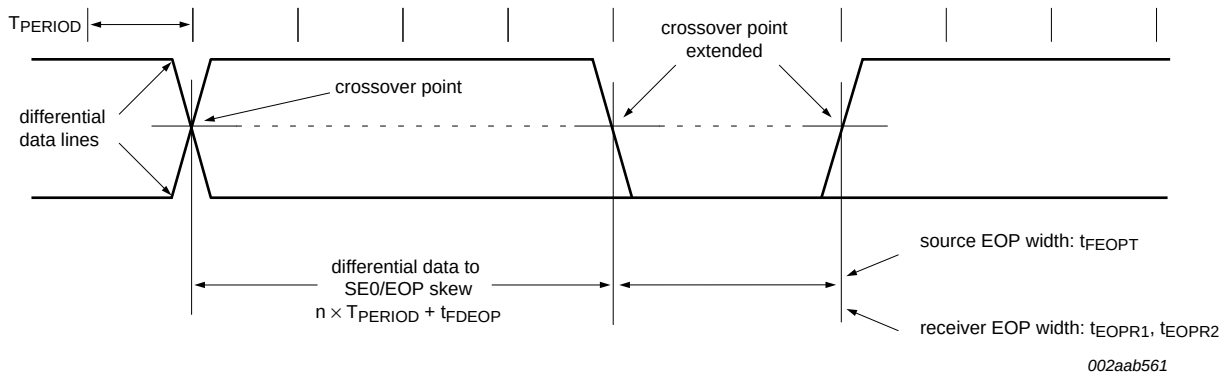

Fig 21. Differential data-to-EOP transition skew and EOP width

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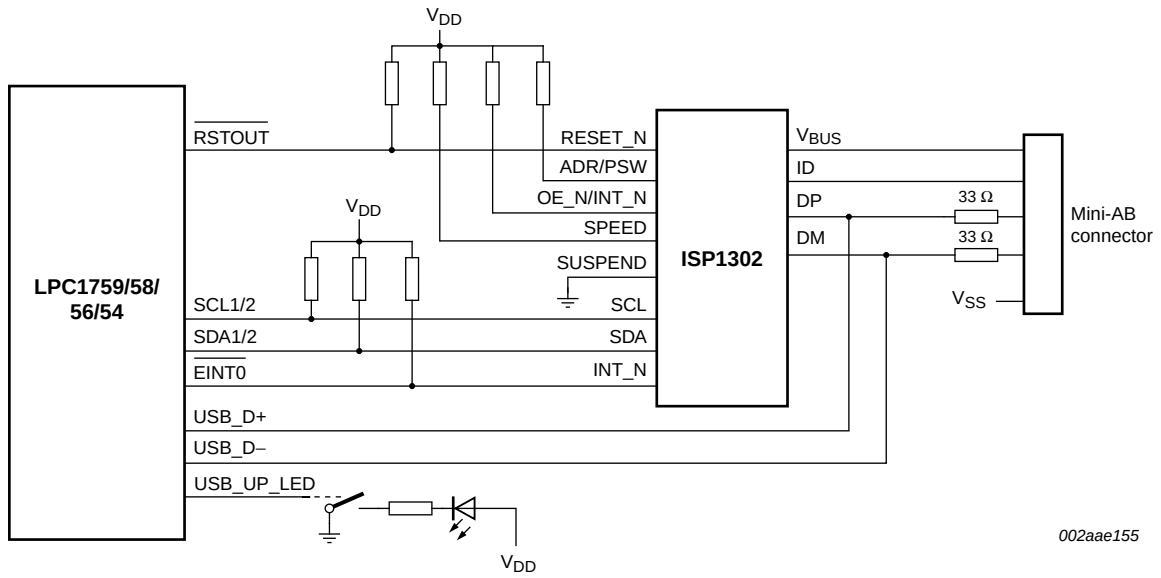

Fig 31. LPC1759/58/56/54 USB OTG port configuration

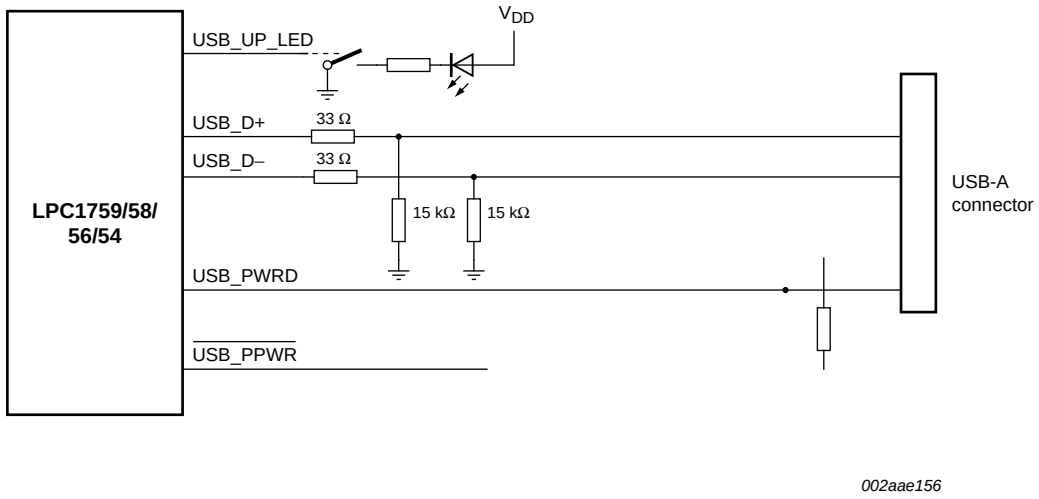

Fig 32. LPC1759/58/56/54 USB host port configuration

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23. Contents

1 General description 1
2 Features and benefits 1
3 Applications 3
4 Ordering information 4
4.1 Ordering options 4
5 Marking 5
6 Block diagram 6
7 Pinning information 7
7.1 Pinning 7
7.2 Pin description 7
8 Functional description 14
8.1 Architectural overview 14
8.2 ARM Cortex-M3 processor 14
8.3 On-chip flash program memory 14
8.4 On-chip SRAM 14
8.5 Memory Protection Unit (MPU) 15
8.6 Memory map 15
8.7 Nested Vectored Interrupt Controller (NVIC) . 17
8.7.1 Features 17
8.7.2 Interrupt sources 17
8.8 Pin connect block 17
8.9 General purpose DMA controller 17
8.9.1 Features 18
8.10 Fast general purpose parallel I/O 18
8.10.1 Features 19
8.11 Ethernet (LPC1758 only) 19
8.11.1 Features 19
8.12 USB interface 20
8.12.1 USB device controller 20
8.12.1.1 Features 20
8.12.2 USB host controller (LPC1759/58/56/54 only). 21
8.12.2.1 Features 21
8.12.3 USB OTG controller (LPC1759/58/56/54 only). . . 21
8.12.3.1 Features 21
8.13 CAN controller and acceptance filters 21
8.13.1 Features 22
8.14 12-bit ADC 22
8.14.1 Features 22
8.15 10-bit DAC (LPC1759/58/56/54 only) 22
8.15.1 Features 22
8.16 UARTs 23
8.16.1 Features 23
8.17 SPI serial I/O controller 23
8.17.1 Features 23
8.18 SSP serial I/O controller 23
8.18.1 Features 24
8.19 I^2C-bus serial I/O controllers 24
8.19.1 Features 24
8.20 I^2S-bus serial I/O controllers (LPC1759/58/56 only) 24
8.20.1 Features 25
8.21 General purpose 32-bit timers/external event counters 25
8.21.1 Features 25
8.22 Pulse width modulator 26
8.22.1 Features 26
8.23 Motor control PWM 27
8.24 Quadrature Encoder Interface (QEI) 27
8.24.1 Features 27
8.25 Repetitive Interrupt (RI) timer 28
8.25.1 Features 28
8.26 ARM Cortex-M3 system tick timer 28
8.27 Watchdog timer 28
8.27.1 Features 28
8.28 RTC and backup registers 29
8.28.1 Features 29
8.29 Clocking and power control 29
8.29.1 Crystal oscillators 29
8.29.1.1 Internal RC oscillator 30
8.29.1.2 Main oscillator 30
8.29.1.3 RTC oscillator 30
8.29.2 Main PLL (PLL0) 31
8.29.3 USB PLL (PLL1) 31
8.29.4 Wake-up timer 31
8.29.5 Power control 32
8.29.5.1 Sleep mode 32
8.29.5.2 Deep-sleep mode 32
8.29.5.3 Power-down mode 33
8.29.5.4 Deep power-down mode 33
8.29.5.5 Wakeup interrupt controller 33
8.29.6 Peripheral power control 33
8.29.7 Power domains 33
8.30 System control 35
8.30.1 Reset 35
8.30.2 Brownout detection 36
8.30.3 Code security (Code Read Protection - CRP) 36
8.30.4 APB interface 36
8.30.5 AHB multilayer matrix 37
8.30.6 External interrupt inputs 37
8.30.7 Memory mapping control 37
8.31 Emulation and debugging 37
9 Limiting values 38
10 Thermal characteristics 39

continued >>

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