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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M3
Core Size	32-Bit Single-Core
Speed	100MHz
Connectivity	CANbus, I²C, IrDA, Microwire, SPI, SSI, SSP, UART/USART, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, Motor Control PWM, POR, PWM, WDT
Number of I/O	52
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	32K x 8
Voltage - Supply (Vcc/Vdd)	2.4V ~ 3.6V
Data Converters	A/D 6x12b; D/A 1x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	80-LQFP
Supplier Device Package	80-LQFP (12x12)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/lpc1754fbd80-518

7. Pinning information

7.1 Pinning

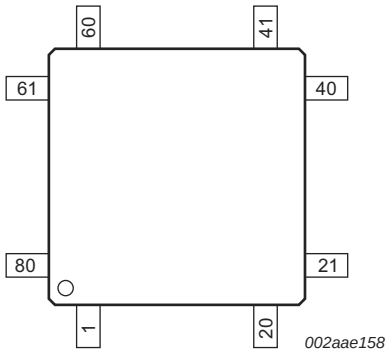


Fig 2. Pin configuration LQFP80 package

7.2 Pin description

Table 4. Pin description

Symbol	Pin	Type	Description
P0[0] to P0[31]		I/O	**Port 0:** Port 0 is a 32-bit I/O port with individual direction controls for each bit. The operation of Port 0 pins depends upon the pin function selected via the pin connect block. Some port pins are not available on the LQFP80 package.
P0[0]/RD1/TXD3/ SDA1	37[1]	I/O	**P0[0] —** General purpose digital input/output pin.
		I	**RD1 —** CAN1 receiver input.
		O	**TXD3 —** Transmitter output for UART3.
		I/O	**SDA1 —** I^2C1 data input/output (this is not an I^2C-bus compliant open-drain pin).
P0[1]/TD1/RXD3/ SCL1	38[1]	I/O	**P0[1] —** General purpose digital input/output pin.
		O	**TD1 —** CAN1 transmitter output.
		I	**RXD3 —** Receiver input for UART3.
		I/O	**SCL1 —** I^2C1 clock input/output (this is not an I^2C-bus compliant open-drain pin).
P0[2]/TXD0/AD0[7]	79[2]	I/O	**P0[2] —** General purpose digital input/output pin.
		O	**TXD0 —** Transmitter output for UART0.
		I	**AD0[7] —** A/D converter 0, input 7.
P0[3]/RXD0/AD0[6]	80[2]	I/O	**P0[3] —** General purpose digital input/output pin.
		I	**RXD0 —** Receiver input for UART0.
		I	**AD0[6] —** A/D converter 0, input 6.
P0[6]/ I2SRX_SDA/ SSEL1/MAT2[0]	64[1]	I/O	**P0[6] —** General purpose digital input/output pin.
		I/O	**I2SRX_SDA —** Receive data. It is driven by the transmitter and read by the receiver. Corresponds to the signal SD in the *I^2S-bus specification*. (LPC1759/58/56 only).
		I/O	**SSEL1 —** Slave Select for SSP1.
		O	**MAT2[0] —** Match output for Timer 2, channel 0.

Table 4. Pin description *…continued*

Symbol	Pin	Type	Description
P1[28]/MCOA2/ PCAP1[0]/ MAT0[0]	35[1]	I/O	**P1[28] —** General purpose digital input/output pin.
		O	**MCOA2 —** Motor control PWM channel 2, output A.
		I	**PCAP1[0] —** Capture input for PWM1, channel 0.
		O	**MAT0[0] —** Match output for Timer 0, channel 0.
P1[29]/MCOB2/ PCAP1[1]/ MAT0[1]	36[1]	I/O	**P1[29] —** General purpose digital input/output pin.
		O	**MCOB2 —** Motor control PWM channel 2, output B.
		I	**PCAP1[1] —** Capture input for PWM1, channel 1.
		O	**MAT0[1] —** Match output for Timer 0, channel 1.
P1[30]/V_{BUS}/ AD0[4]	18[2]	I/O	**P1[30] —** General purpose digital input/output pin.
		I	**V_{BUS} —** Monitors the presence of USB bus power. **Note:** This signal must be HIGH for USB reset to occur.
		I	**AD0[4] —** A/D converter 0, input 4.
P1[31]/SCK1/ AD0[5]	17[2]	I/O	**P1[31] —** General purpose digital input/output pin.
		I/O	**SCK1 —** Serial Clock for SSP1.
		I	**AD0[5] —** A/D converter 0, input 5.
P2[0] to P2[31]		I/O	**Port 2:** Port 2 is a 32-bit I/O port with individual direction controls for each bit. The operation of port 2 pins depends upon the pin function selected via the pin connect block. Some port pins are not available on the LQFP80 package.
P2[0]/PWM1[1]/ TXD1	60[1]	I/O	**P2[0] —** General purpose digital input/output pin.
		O	**PWM1[1] —** Pulse Width Modulator 1, channel 1 output.
		O	**TXD1 —** Transmitter output for UART1.
P2[1]/PWM1[2]/ RXD1	59[1]	I/O	**P2[1] —** General purpose digital input/output pin.
		O	**PWM1[2] —** Pulse Width Modulator 1, channel 2 output.
		I	**RXD1 —** Receiver input for UART1.
P2[2]/PWM1[3]/ CTS1/ TRACEDATA[3]	58[1]	I/O	**P2[2] —** General purpose digital input/output pin.
		O	**PWM1[3] —** Pulse Width Modulator 1, channel 3 output.
		I	**CTS1 —** Clear to Send input for UART1.
		O	**TRACEDATA[3] —** Trace data, bit 3.
P2[3]/PWM1[4]/ DCD1/ TRACEDATA[2]	55[1]	I/O	**P2[3] —** General purpose digital input/output pin.
		O	**PWM1[4] —** Pulse Width Modulator 1, channel 4 output.
		I	**DCD1 —** Data Carrier Detect input for UART1.
		O	**TRACEDATA[2] —** Trace data, bit 2.
P2[4]/PWM1[5]/ DSR1/ TRACEDATA[1]	54[1]	I/O	**P2[4] —** General purpose digital input/output pin.
		O	**PWM1[5] —** Pulse Width Modulator 1, channel 5 output.
		I	**DSR1 —** Data Set Ready input for UART1.
		O	**TRACEDATA[1] —** Trace data, bit 1.
P2[5]/PWM1[6]/ DTR1/ TRACEDATA[0]	53[1]	I/O	**P2[5] —** General purpose digital input/output pin.
		O	**PWM1[6] —** Pulse Width Modulator 1, channel 6 output.
		O	**DTR1 —** Data Terminal Ready output for UART1. Can also be configured to be an RS-485/EIA-485 output enable signal.
		O	**TRACEDATA[0] —** Trace data, bit 0.

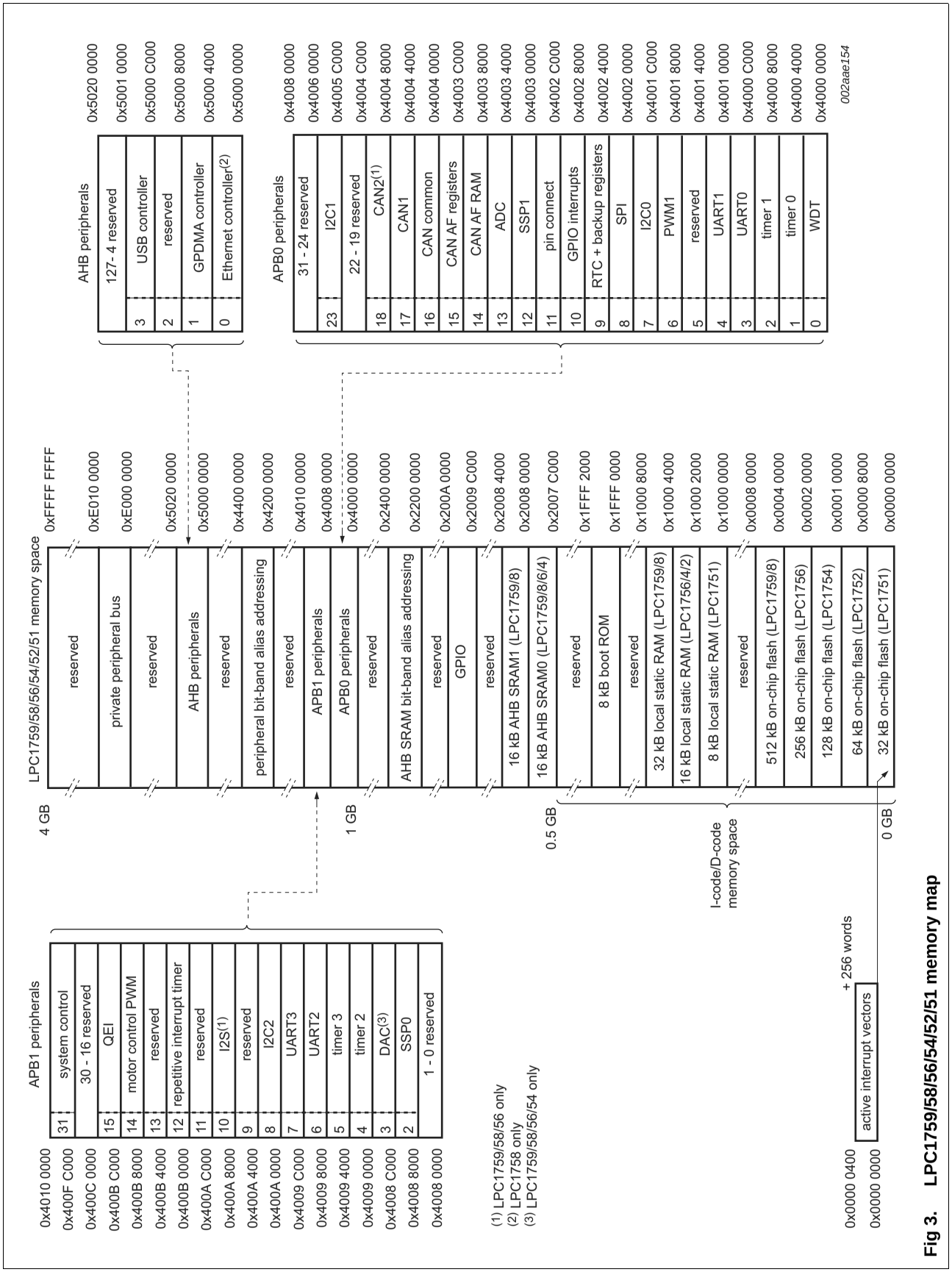


Fig 3. LPC1759/58/56/54/52/51 memory map

8.9.1 Features

- Eight DMA channels. Each channel can support an unidirectional transfer.
- 16 DMA request lines.
- Single DMA and burst DMA request signals. Each peripheral connected to the DMA Controller can assert either a burst DMA request or a single DMA request. The DMA burst size is set by programming the DMA Controller.
- Memory-to-memory, memory-to-peripheral, peripheral-to-memory, and peripheral-to-peripheral transfers are supported.
- Scatter or gather DMA is supported through the use of linked lists. This means that the source and destination areas do not have to occupy contiguous areas of memory.
- Hardware DMA channel priority.
- AHB slave DMA programming interface. The DMA Controller is programmed by writing to the DMA control registers over the AHB slave interface.
- One AHB bus master for transferring data. The interface transfers data when a DMA request goes active.
- 32-bit AHB master bus width.
- Incrementing or non-incrementing addressing for source and destination.
- Programmable DMA burst size. The DMA burst size can be programmed to more efficiently transfer data.
- Internal four-word FIFO per channel.
- Supports 8, 16, and 32-bit wide transactions.
- Big-endian and little-endian support. The DMA Controller defaults to little-endian mode on reset.
- An interrupt to the processor can be generated on a DMA completion or when a DMA error has occurred.
- Raw interrupt status. The DMA error and DMA count raw interrupt status can be read prior to masking.

8.10 Fast general purpose parallel I/O

Device pins that are not connected to a specific peripheral function are controlled by the GPIO registers. Pins may be dynamically configured as inputs or outputs. Separate registers allow setting or clearing any number of outputs simultaneously. The value of the output register may be read back as well as the current state of the port pins.

LPC1759/58/56/54/52/51 use accelerated GPIO functions:

- GPIO registers are accessed through the AHB multilayer bus so that the fastest possible I/O timing can be achieved.
- Mask registers allow treating sets of port bits as a group, leaving other bits unchanged.
- All GPIO registers are byte and half-word addressable.
- Entire port value can be written in one instruction.
- Support for Cortex-M3 bit banding.
- Support for use with the GPDMA controller.

8.13.1 Features

- One or two CAN controllers and buses.
- Data rates to 1 Mbit/s on each bus.
- 32-bit register and RAM access.
- Compatible with *CAN specification 2.0B, ISO 11898-1*.
- Global Acceptance Filter recognizes standard (11-bit) and extended-frame (29-bit) receive identifiers for all CAN buses.
- Acceptance Filter can provide FullCAN-style automatic reception for selected Standard Identifiers.
- FullCAN messages can generate interrupts.

8.14 12-bit ADC

The LPC1759/58/56/54/52/51 contain one ADC. It is a single 12-bit successive approximation ADC with six channels and DMA support.

8.14.1 Features

- 12-bit successive approximation ADC.
- Input multiplexing among 6 pins.
- Power-down mode.
- Measurement range VREFN to VREFP.
- 12-bit conversion rate: 200 kHz.
- Individual channels can be selected for conversion.
- Burst conversion mode for single or multiple inputs.
- Optional conversion on transition of input pin or Timer Match signal.
- Individual result registers for each ADC channel to reduce interrupt overhead.
- DMA support.

8.15 10-bit DAC (LPC1759/58/56/54 only)

The DAC allows to generate a variable analog output. The maximum output value of the DAC is VREFP.

8.15.1 Features

- 10-bit DAC
- Resistor string architecture
- Buffered output
- Power-down mode
- Selectable output drive
- Dedicated conversion timer
- DMA support

8.25 Repetitive Interrupt (RI) timer

The repetitive interrupt timer provides a free-running 32-bit counter which is compared to a selectable value, generating an interrupt when a match occurs. Any bits of the timer/compare can be masked such that they do not contribute to the match detection. The repetitive interrupt timer can be used to create an interrupt that repeats at predetermined intervals.

8.25.1 Features

- 32-bit counter running from PCLK. Counter can be free-running or be reset by a generated interrupt.
- 32-bit compare value.
- 32-bit compare mask. An interrupt is generated when the counter value equals the compare value, after masking. This allows for combinations not possible with a simple compare.

8.26 ARM Cortex-M3 system tick timer

The ARM Cortex-M3 includes a system tick timer (SYSTICK) that is intended to generate a dedicated SYSTICK exception at a 10 ms interval. In the LPC1759/58/56/54/52/51, this timer can be clocked from the internal AHB clock or from a device pin.

8.27 Watchdog timer

The purpose of the watchdog is to reset the microcontroller within a reasonable amount of time if it enters an erroneous state. When enabled, the watchdog will generate a system reset if the user program fails to ‘feed’ (or reload) the watchdog within a predetermined amount of time.

8.27.1 Features

- Internally resets chip if not periodically reloaded.
- Debug mode.
- Enabled by software but requires a hardware reset or a watchdog reset/interrupt to be disabled.
- Incorrect/Incomplete feed sequence causes reset/interrupt if enabled.
- Flag to indicate watchdog reset.
- Programmable 32-bit timer with internal prescaler.
- Selectable time period from ($T_{cy(WDCLK)} \times 256 \times 4$) to ($T_{cy(WDCLK)} \times 2^{32} \times 4$) in multiples of $T_{cy(WDCLK)} \times 4$.
- The Watchdog Clock (WDCLK) source can be selected from the Internal RC (IRC) oscillator, the RTC oscillator, or the APB peripheral clock. This gives a wide range of potential timing choices of Watchdog operation under different power reduction conditions. It also provides the ability to run the WDT from an entirely internal source that is not dependent on an external crystal and its associated components and wiring for increased reliability.
- Includes lock/safe feature.

On wake-up from Deep-sleep mode, the code execution and peripherals activities will resume after 4 cycles expire if the IRC was used before entering Deep-sleep mode. If the main external oscillator was used, the code execution will resume when 4096 cycles expire. PLL and clock dividers need to be reconfigured accordingly.

8.29.5.3 Power-down mode

Power-down mode does everything that Deep-sleep mode does, but also turns off the power to the IRC oscillator and the flash memory. This saves more power but requires waiting for resumption of flash operation before execution of code or data access in the flash memory can be accomplished.

On the wake-up of Power-down mode, if the IRC was used before entering Power-down mode, it will take IRC 60 μs to start-up. After this 4 IRC cycles will expire before the code execution can then be resumed if the code was running from SRAM. In the meantime, the flash wake-up timer then counts 4 MHz IRC clock cycles to make the 100 μs flash start-up time. When it times out, access to the flash will be allowed. Users need to reconfigure the PLL and clock dividers accordingly.

8.29.5.4 Deep power-down mode

The Deep power-down mode can only be entered from the RTC block. In Deep power-down mode, power is shut off to the entire chip with the exception of the RTC module and the $\overline{\text{RESET}}$ pin.

The LPC1759/58/56/54/52/51 can wake up from Deep power-down mode via the $\overline{\text{RESET}}$ pin or an alarm match event of the RTC.

8.29.5.5 Wakeup interrupt controller

The Wakeup Interrupt Controller (WIC) allows the CPU to automatically wake up from any enabled priority interrupt that can occur while the clocks are stopped in Deep sleep, Power-down, and Deep power-down modes.

The Wakeup Interrupt Controller (WIC) works in connection with the Nested Vectored Interrupt Controller (NVIC). When the CPU enters Deep sleep, Power-down, or Deep power-down mode, the NVIC sends a mask of the current interrupt situation to the WIC.This mask includes all of the interrupts that are both enabled and of sufficient priority to be serviced immediately. With this information, the WIC simply notices when one of the interrupts has occurred and then it wakes up the CPU.

The Wakeup Interrupt Controller (WIC) eliminates the need to periodically wake up the CPU and poll the interrupts resulting in additional power savings.

8.29.6 Peripheral power control

A power control for peripherals feature allows individual peripherals to be turned off if they are not needed in the application, resulting in additional power savings.

8.29.7 Power domains

The LPC1759/58/56/54/52/51 provide two independent power domains that allow the bulk of the device to have power removed while maintaining operation of the RTC and the backup Registers.

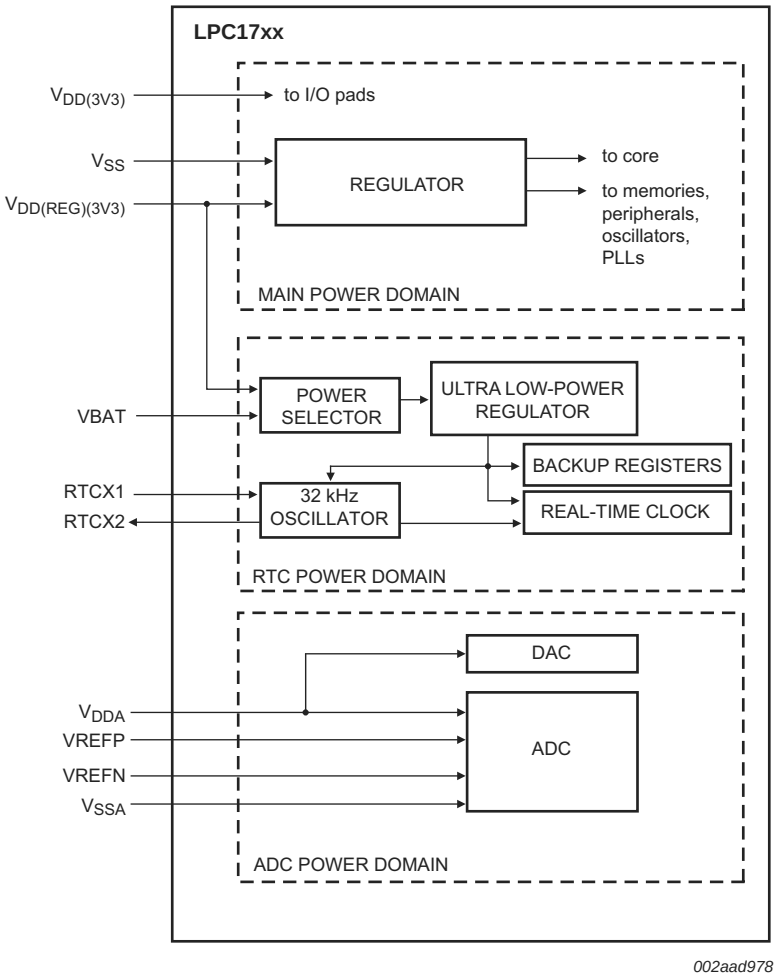


Fig 5. Power distribution

8.30 System control

8.30.1 Reset

Reset has four sources on the LPC17xx: the $\overline{\text{RESET}}$ pin, the Watchdog reset, power-on reset (POR), and the BrownOut Detection (BOD) circuit. The $\overline{\text{RESET}}$ pin is a Schmitt trigger input pin. Assertion of chip Reset by any source, once the operating voltage attains a usable level, causes the $\overline{\text{RSTOUT}}$ pin to go LOW and starts the wake-up timer (see description in Section 8.29.4). The wake-up timer ensures that reset remains asserted until the external Reset is de-asserted, the oscillator is running, a fixed number of clocks have passed, and the flash controller has completed its initialization. Once reset is de-asserted, or, in case of a BOD-triggered reset, once the voltage rises above the BOD threshold, the $\overline{\text{RSTOUT}}$ pin goes HIGH.

When the internal Reset is removed, the processor begins executing at address 0, which is initially the Reset vector mapped from the boot block. At that point, all of the processor and peripheral registers have been initialized to predetermined values.

9. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).[1]

Symbol	Parameter	Conditions		Min	Max	Unit
$V_{DD(3V3)}$	supply voltage (3.3 V)	external rail	[2]	−0.5	+4.6	V
$V_{DD(REG)(3V3)}$	regulator supply voltage (3.3 V)		[2]	−0.5	+4.6	V
V_{DDA}	analog 3.3 V pad supply voltage		[2]	−0.5	+4.6	V
$V_{i(VBAT)}$	input voltage on pin VBAT	for the RTC	[2]	−0.5	+4.6	V
$V_{i(VREFP)}$	input voltage on pin VREFP		[2]	−0.5	+4.6	V
V_{IA}	analog input voltage	on ADC related pins	[2][3]	−0.5	+5.1	V
V_I	input voltage	5 V tolerant digital I/O pins; $V_{DD} \geq 2.4$ V	[2][4]	−0.5	+5.5	V
		$V_{DD} = 0$ V		−0.5	+3.6	
I_{DD}	supply current	per supply pin		-	100	mA
I_{SS}	ground current	per ground pin		-	100	mA
I_{latch}	I/O latch-up current	$-(0.5V_{DD(3V3)}) < V_I < (1.5V_{DD(3V3)})$; $T_j < 125$ °C		-	100	mA
T_{stg}	storage temperature		[5]	−65	+150	°C
$T_{j(max)}$	maximum junction temperature				150	°C
$P_{tot(pack)}$	total power dissipation (per package)	based on package heat transfer, not device power consumption		-	1.5	W
V_{ESD}	electrostatic discharge voltage	human body model; all pins	[6]	−4000	+4000	V

[1] The following applies to the limiting values:

a) This product includes circuitry specifically designed for the protection of its internal devices from the damaging effects of excessive static charge. Nonetheless, it is suggested that conventional precautions be taken to avoid applying greater than the rated maximum.

b) Parameters are valid over operating temperature range unless otherwise specified. All voltages are with respect to V_{SS} unless otherwise noted.

c) The limiting values are stress ratings only. Operating the part at these values is not recommended, and proper operation is not guaranteed. The conditions for functional operation are specified in Table 7.

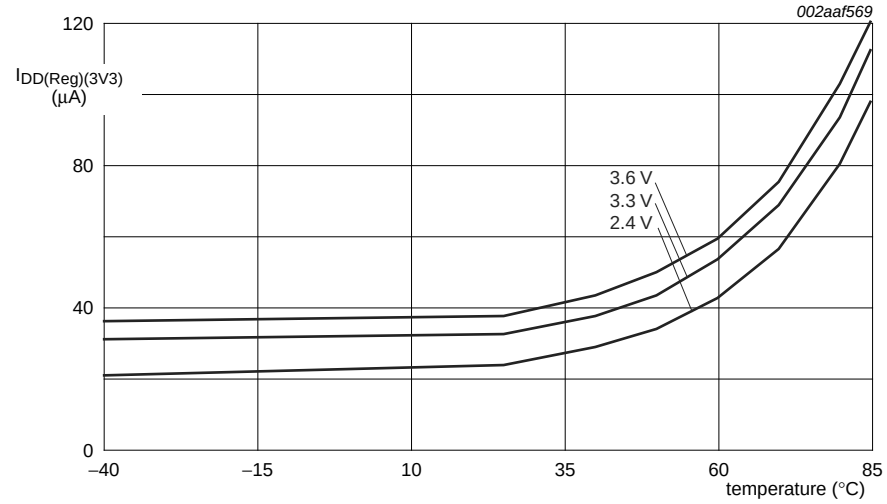
[2] Maximum/minimum voltage above the maximum operating voltage (see Table 7) and below ground that can be applied for a short time (< 10 ms) to a device without leading to irrecoverable failure. Failure includes the loss of reliability and shorter lifetime of the device.

[3] See Table 18 for maximum operating voltage.

[4] Including voltage on outputs in 3-state mode.

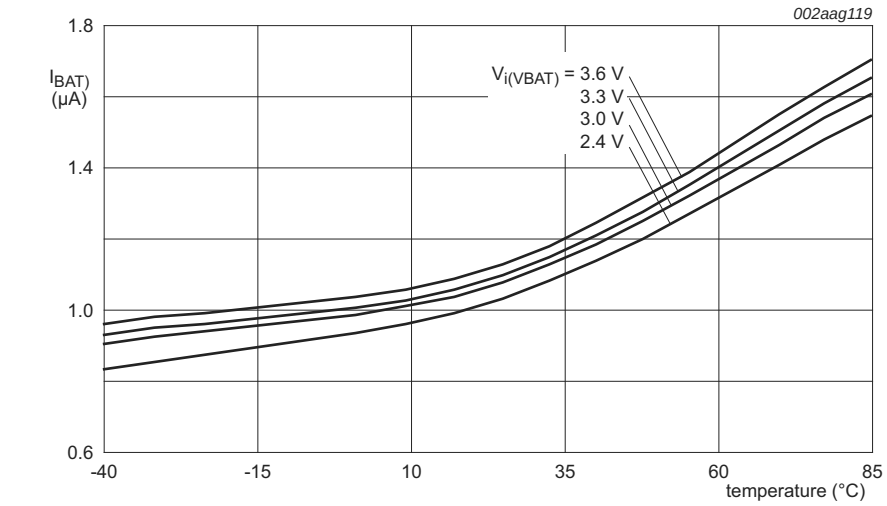
[5] The maximum non-operating storage temperature is different than the temperature for required shelf life which should be determined based on required shelf lifetime. Please refer to the JEDEC spec (J-STD-033B.1) for further details.

[6] Human body model: equivalent to discharging a 100 pF capacitor through a 1.5 kΩ series resistor.



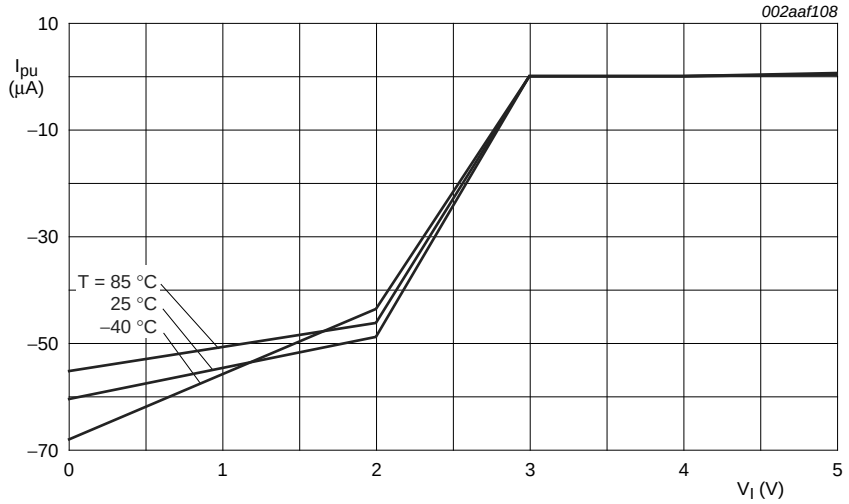
Conditions: $V_{DD(Reg)(3V3)}$ = 3.3 V; BOD disabled.

Fig 7. Power-down mode: Typical regulator supply current $I_{DD(Reg)(3V3)}$ versus temperature



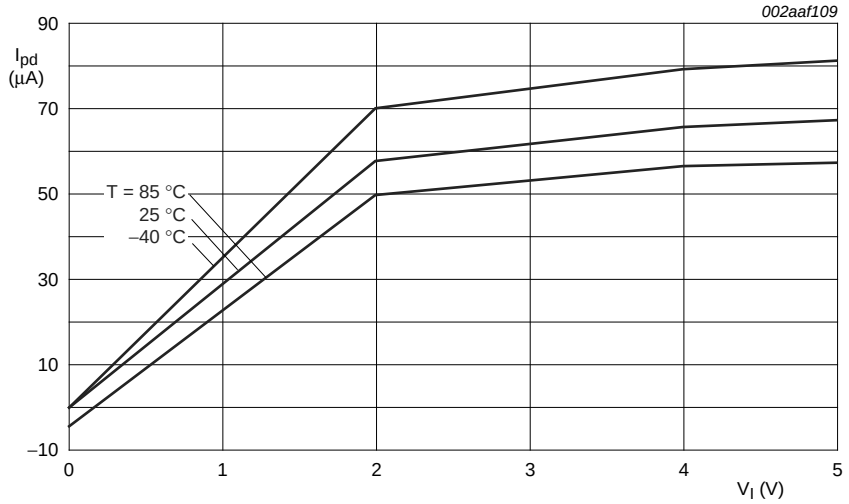
Conditions: $V_{DD(REG)(3V3)}$ floating; RTC running.

Fig 8. Deep power-down mode: Typical battery supply current I_{BAT} versus temperature



Conditions: $V_{DD(REG)(3V3)} = V_{DD(3V3)} = 3.3$ V; standard port pins.

Fig 12. Typical pull-up current I_{pu} versus input voltage V_I



Conditions: $V_{DD(REG)(3V3)} = V_{DD(3V3)} = 3.3$ V; standard port pins.

Fig 13. Typical pull-down current I_{pd} versus input voltage V_I

12.7 SSP interface

The maximum SSP speed is 33 Mbit/s in master mode or 8 Mbit/s in slave mode. In slave mode, the maximum SSP clock rate must be 1/12 of the SSP PCLK clock rate.

Table 15. Dynamic characteristics: SSP pins in SPI mode

C_L = 30 pF on all SSP pins; T_{amb} = −40 °C to 85 °C; $V_{DD(3V3)}$ = 3.3 V to 3.6 V; input slew = 1 ns; sampled at 10 % and 90 % of the signal level. Values guaranteed by design.

Symbol	Parameter	Conditions	Min	Max	Unit
SSP master					
t_{DS}	data set-up time	in SPI mode	16.1	-	ns
t_{DH}	data hold time	in SPI mode	0	-	ns
$t_{v(Q)}$	data output valid time	in SPI mode	-	2.5	ns
$t_{h(Q)}$	data output hold time	in SPI mode	0	-	ns
SSP slave					
t_{DS}	data set-up time	in SPI mode	16.1	-	ns
t_{DH}	data hold time	in SPI mode	0	-	ns
$t_{v(Q)}$	data output valid time	in SPI mode	-	$3*T_{cy(PCLK)} + 2.5$	ns
$t_{h(Q)}$	data output hold time	in SPI mode	0	-	ns

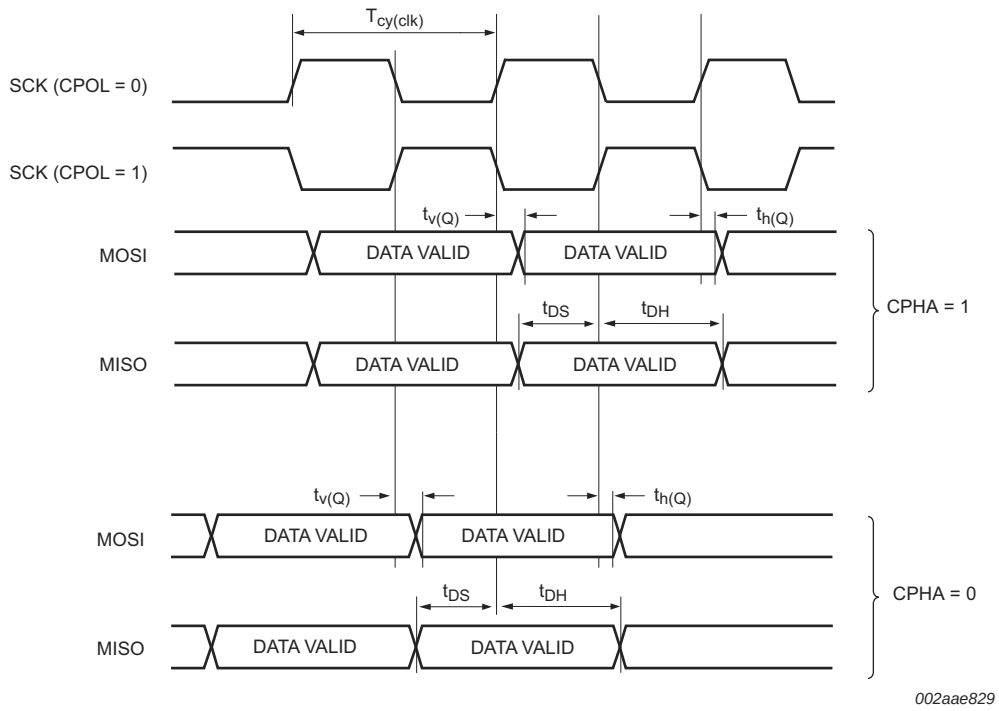


Fig 19. SSP master timing in SPI mode

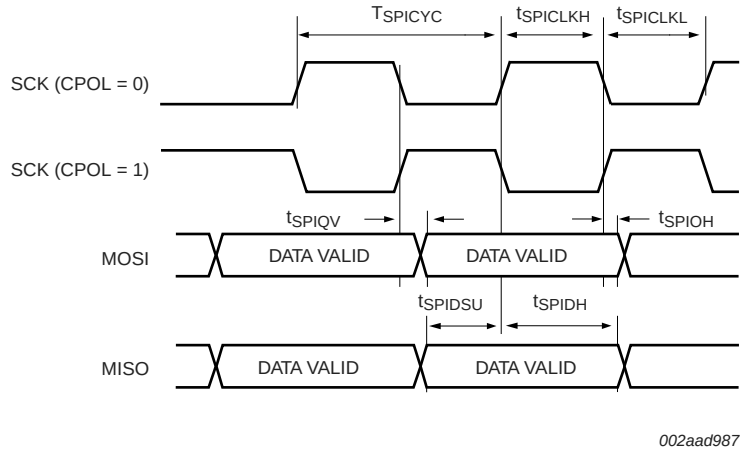


Fig 23. SPI master timing (CPHA = 0)

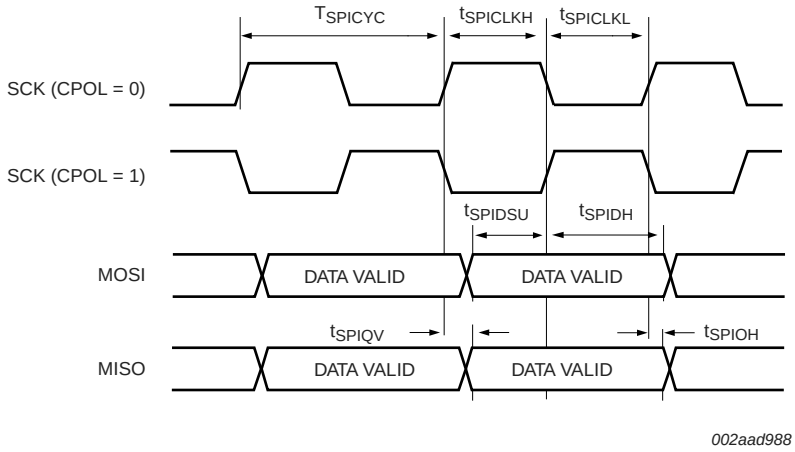


Fig 24. SPI slave timing (CPHA = 1)

Table 19. ADC characteristics (lower resolution)

T_{amb} = −40 °C to +85 °C unless otherwise specified; 12-bit ADC used as 10-bit resolution ADC.[1]

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
E_D	differential linearity error		[2][3]	-	±1	-	LSB
$E_{L(adj)}$	integral non-linearity		[4]	-	±1.5	-	LSB
E_O	offset error		[5]	-	±2	-	LSB
E_G	gain error		[6]	-	±2	-	LSB
$f_{clk(ADC)}$	ADC clock frequency	$3.0\ V \leq V_{DDA} \leq 3.6\ V$		-	-	33	MHz
		$2.7\ V \leq V_{DDA} < 3.0\ V$		-	-	25	MHz
$f_{c(ADC)}$	ADC conversion frequency	$3\ V \leq V_{DDA} \leq 3.6\ V$	[7]	-	-	500	kHz
		$2.7\ V \leq V_{DDA} < 3.0\ V$	[7]	-	-	400	kHz

[1] V_{DDA} and VREFP should be tied to $V_{DD(3V3)}$ if the ADC and DAC are not used.

[2] The ADC is monotonic, there are no missing codes.

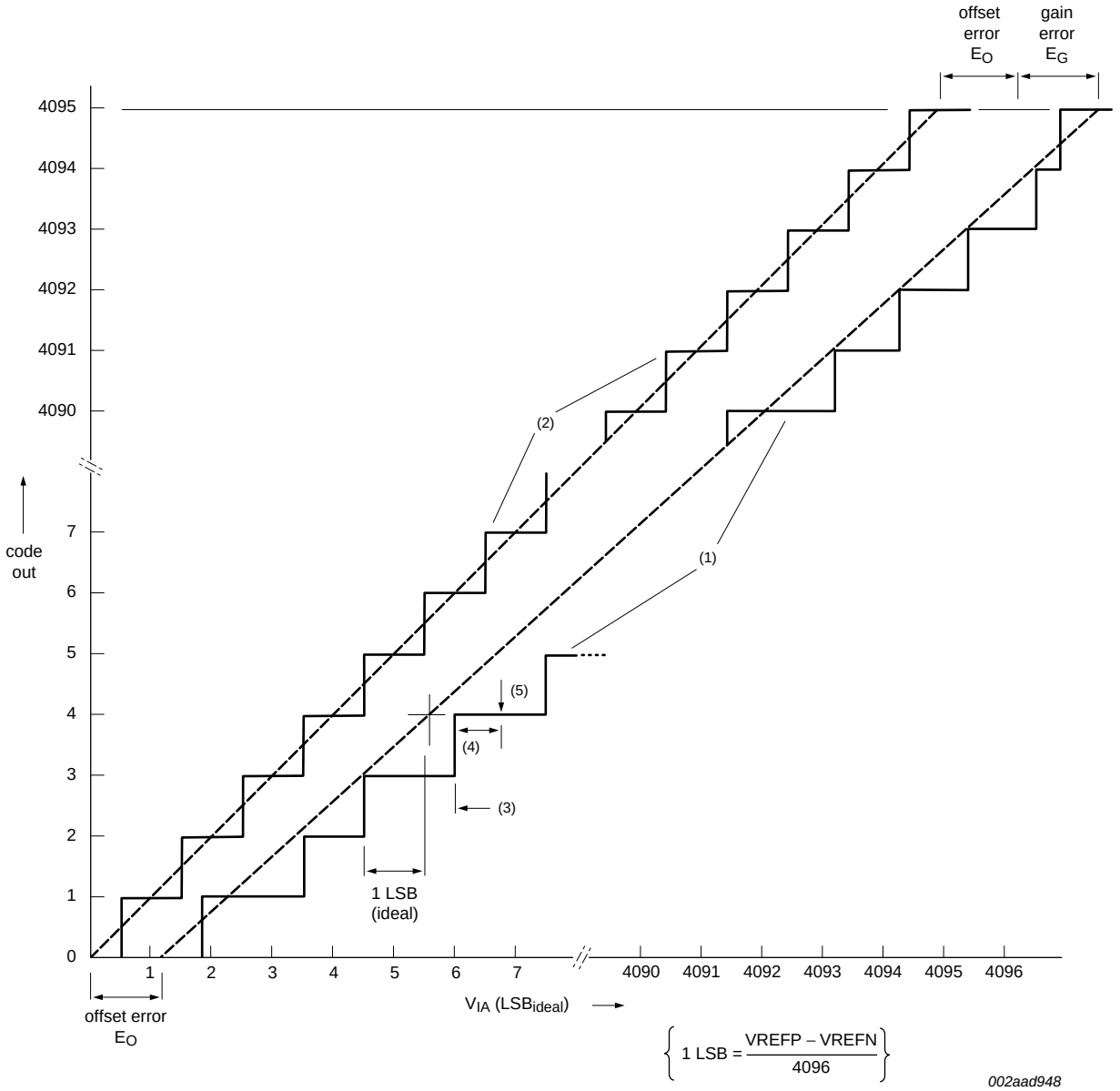
[3] The differential linearity error (E_D) is the difference between the actual step width and the ideal step width. See Figure 26.

[4] The integral non-linearity ($E_{L(adj)}$) is the peak difference between the center of the steps of the actual and the ideal transfer curve after appropriate adjustment of gain and offset errors. See Figure 26.

[5] The offset error (E_O) is the absolute difference between the straight line which fits the actual curve and the straight line which fits the ideal curve. See Figure 26.

[6] The gain error (E_G) is the relative difference in percent between the straight line fitting the actual transfer curve after removing offset error, and the straight line which fits the ideal transfer curve. See Figure 26.

[7] The conversion frequency corresponds to the number of samples per second.



(1) Example of an actual transfer curve.

(2) The ideal transfer curve.

(3) Differential linearity error (E_D).

(4) Integral non-linearity ($E_{L(adj)}$).

(5) Center of a step of the actual transfer curve.

Fig 26. 12-bit ADC characteristics

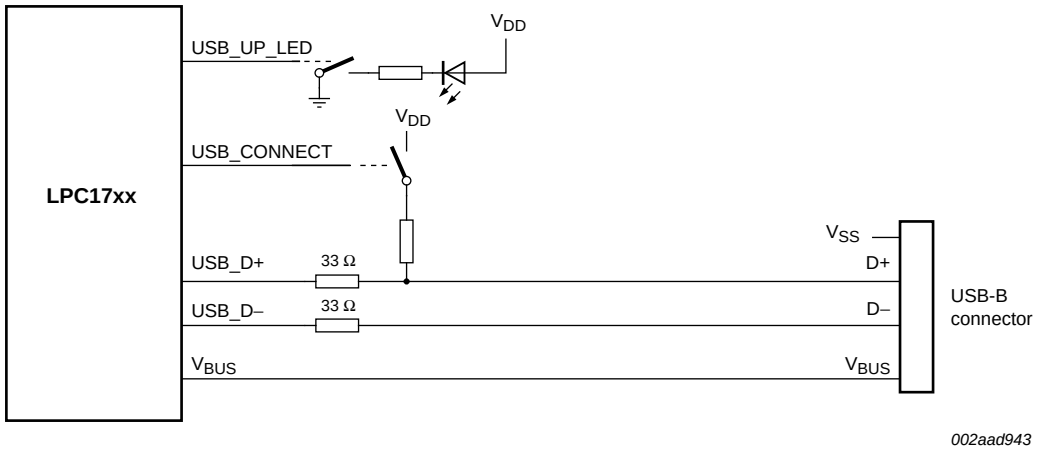


Fig 33. LPC1759/58/56/54/52/51 USB device port configuration

15.2 Crystal oscillator XTAL input and component selection

The input voltage to the on-chip oscillators is limited to 1.8 V. If the oscillator is driven by a clock in slave mode, it is recommended that the input be coupled through a capacitor with C_i = 100 pF. To limit the input voltage to the specified range, choose an additional capacitor to ground C_g which attenuates the input voltage by a factor $C_i/(C_i + C_g)$. In slave mode, a minimum of 200 mV(RMS) is needed.

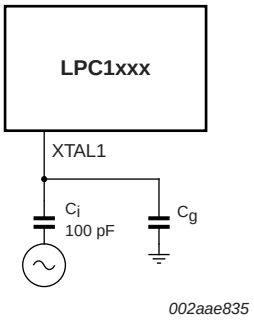


Fig 34. Slave mode operation of the on-chip oscillator

In slave mode the input clock signal should be coupled by means of a capacitor of 100 pF (Figure 34), with an amplitude between 200 mV(RMS) and 1000 mV(RMS). This corresponds to a square wave signal with a signal swing of between 280 mV and 1.4 V. The XTALOUT pin in this configuration can be left unconnected.

External components and models used in oscillation mode are shown in Figure 35 and in Table 22 and Table 23. Since the feedback resistance is integrated on chip, only a crystal and the capacitances C_{X1} and C_{X2} need to be connected externally in case of fundamental mode oscillation (the fundamental frequency is represented by L, C_L and R_S). Capacitance C_P in Figure 35 represents the parallel package capacitance and should not be larger than 7 pF. Parameters F_{OSC}, C_L, R_S and C_P are supplied by the crystal manufacturer.

15.6 ElectroMagnetic Compatibility (EMC)

Radiated emission measurements according to the IEC61967-2 standard using the TEM-cell method are shown for part LPC1768.

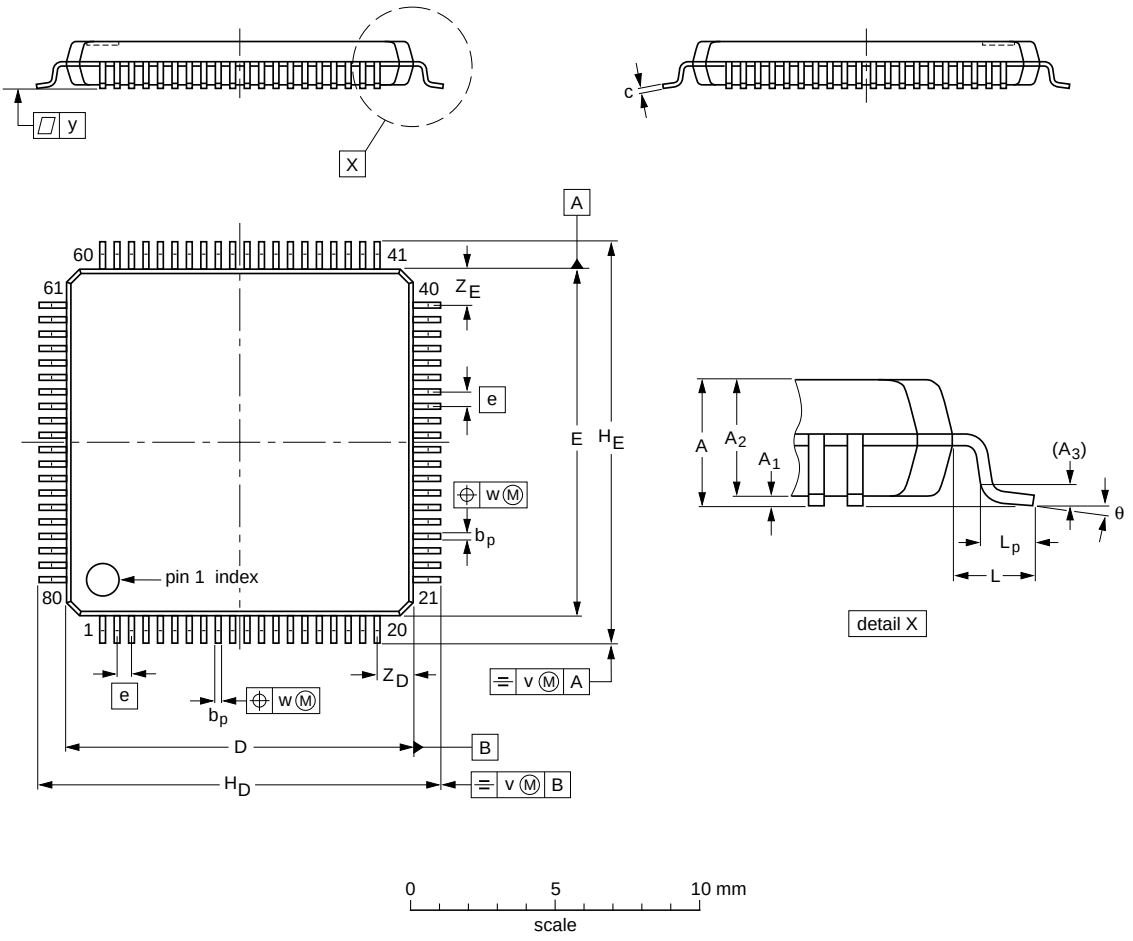
Table 24. ElectroMagnetic Compatibility (EMC) for part LPC1768 (TEM-cell method)
V_{DD} = 3.3 V; T_{amb} = 25 °C.

Parameter	Frequency band	System clock =					Unit
		12 MHz	24 MHz	48 MHz	72 MHz	100 MHz	
Input clock: IRC (4 MHz)							
maximum peak level	150 kHz to 30 MHz	−7	−6	−4	−7	−7	dBμV
	30 MHz to 150 MHz	+1	+5	+11	+16	+9	dBμV
	150 MHz to 1 GHz	−2	+4	+11	+12	+19	dBμV
IEC level[1]	-	O	O	N	M	L	-
Input clock: crystal oscillator (12 MHz)							
maximum peak level	150 kHz to 30 MHz	−5	−4	−4	−7	−8	dBμV
	30 MHz to 150 MHz	−1	+5	+10	+15	+7	dBμV
	150 MHz to 1 GHz	−1	+6	+11	+10	+16	dBμV
IEC level[1]	-	O	O	N	M	M	-

[1] IEC levels refer to Appendix D in the IEC61967-2 Specification.

16. Package outline

LQFP80: plastic low profile quad flat package; 80 leads; body 12 x 12 x 1.4 mm **SOT315-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_D	H_E	L	L_p	v	w	y	$Z_D^{(1)}$	$Z_E^{(1)}$	θ
mm	1.6	0.16 0.04	1.5 1.3	0.25	0.27 0.13	0.18 0.12	12.1 11.9	12.1 11.9	0.5	14.15 13.85	14.15 13.85	1	0.75 0.30	0.2	0.15	0.1	1.45 1.05	1.45 1.05	7^o 0^o

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT315-1	136E15	MS-026				~~00-01-19~~ 03-02-25

Fig 38. Package outline (LQFP80)

Table 26. Revision history *…continued*

Document ID	Release date	Data sheet status	Change notice	Supersedes
LPC1759_58_56_54_52_51 v.8.1	20130912	Product data sheet	-	LPC1759_58_56_54_52_51 v.8
Modifications:	• Added Table 6 “Thermal resistance”. • Table 5 “Limiting values”: – Updated min/max values for $V_{DD(3V3)}$ and $V_{DD(REG)(3V3)}$. – Updated conditions for V_I. – Updated table notes. • Table 7 “Static characteristics”: Added Table note 14 “TCK/SWDCLK pin needs to be externally pulled LOW.” • Updated Section 15.1 “Suggested USB interface solutions”. • Added Section 5 “Marking”. • Changed title of Figure 29 from “USB interface on a self-powered device” to “USB interface with soft-connect”.			
LPC1759_58_56_54_52_51 v.8	20120809	Product data sheet	-	LPC1759_58_56_54_52_51 v.7
Modifications:	• Remove table note “The peak current is limited to 25 times the corresponding maximum current.” from Table 4 “Limiting values”. • Change $V_{DD(3V3)}$ to $V_{DD(REG)(3V3)}$ in Section 11.3 “Internal oscillators”. • Glitch filter constant changed to 10 ns in Table note 5 in Table 3. • Description of $\overline{\text{RESET}}$ function updated in Table 3. • Pull-up value added for GPIO pins in Table 3. • Pin configuration diagram for LQFP80 package corrected (Figure 2). • Pin description of USB_UP_LED pin updated in Table 3. • R_{i1} and R_{i2} labels in Figure 26 updated. • Table note 9 updated in Table 3. • Table note 1 updated in Table 12. • Electromagnetic compatibility data added in Section 14.6. • Section 16 added.			
LPC1759_58_56_54_52_51 v.7	20110329	Product data sheet	-	LPC1759_58_56_54_52_51 v.6
Modifications:	• Pin description of pins P0[29] and P0[30] updated in Table note 4 of Table 3. Pins are not 5 V tolerant. • Typical value for Parameter N_{endu} added in Table 8. • Condition 3.0 V ≤ $V_{DD(3V3)}$ ≤ 3.6 V added in Table 15. • Typical values for parameters $I_{DD(REG)(3V3)}$ and I_{BAT} with condition Deep power-down mode corrected in Table 6 and Table note 9, Table note 10, and Table note 11 updated. • For Deep power-down mode, Figure 8 updated and Figure 9 added.			
LPC1759_58_56_54_52_51 v.6	20100825	Product data sheet	-	LPC1759_58_56_54_52_51 v.5
Modifications:	• Section 7.30.2; BOD level corrected. • Added Section 10.2.			
LPC1759_58_56_54_52_51 v.5	20100716	Product data sheet	-	LPC1759_58_56_54_52_51 v.4
LPC1759_58_56_54_52_51 v.4	20100126	Product data sheet	-	LPC1758_56_54_52_51 v.3
LPC1758_56_54_52_51 v.3	20091119	Product data sheet	-	LPC1758_56_54_52_51 v.2
LPC1758_56_54_52_51 v.2	20090211	Objective data sheet	-	LPC1758_56_54_52_51 v.1
LPC1758_56_54_52_51 v.1	20090115	Objective data sheet	-	-

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