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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Discontinued at Digi-Key
Core Processor	ARM® Cortex®-M3
Core Size	32-Bit Single-Core
Speed	100MHz
Connectivity	CANbus, I²C, IrDA, Microwire, SPI, SSI, SSP, UART/USART, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, Motor Control PWM, POR, PWM, WDT
Number of I/O	52
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	32K x 8
Voltage - Supply (Vcc/Vdd)	2.4V ~ 3.6V
Data Converters	A/D 6x12b; D/A 1x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	80-LQFP
Supplier Device Package	80-LQFP (12x12)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/lpc1754fbd80-551

4. Ordering information

Table 1. Ordering information

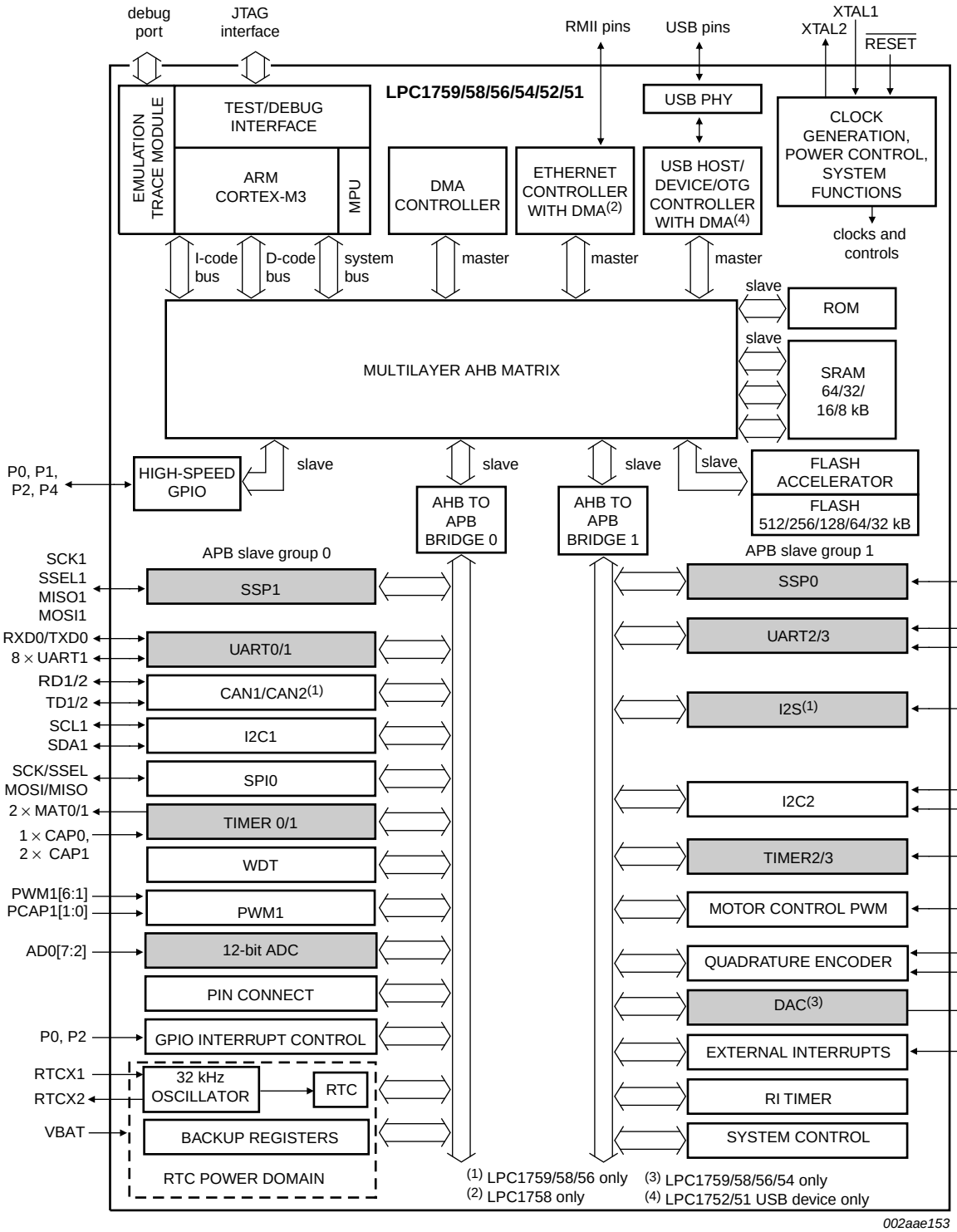
Type number	Package		
	Name	Description	Version
LPC1759FBD80	LQFP80	plastic low-profile quad package; 80 leads; body 12 × 12 × 1.4 mm	SOT315-1
LPC1758FBD80	LQFP80	plastic low-profile quad package; 80 leads; body 12 × 12 × 1.4 mm	SOT315-1
LPC1756FBD80	LQFP80	plastic low-profile quad package; 80 leads; body 12 × 12 × 1.4 mm	SOT315-1
LPC1754FBD80	LQFP80	plastic low-profile quad package; 80 leads; body 12 × 12 × 1.4 mm	SOT315-1
LPC1752FBD80	LQFP80	plastic low-profile quad package; 80 leads; body 12 × 12 × 1.4 mm	SOT315-1
LPC1751FBD80	LQFP80	plastic low-profile quad package; 80 leads; body 12 × 12 × 1.4 mm	SOT315-1

4.1 Ordering options

Table 2. Ordering options

Type number	Device order part number	Flash (kB)	SRAM in kB				Ethernet	USB	CAN	I^2S-bus	DAC	GPIO	Maximum CPU operating frequency (MHz)
			CPU	AHB SRAM0	AHB SRAM1	Total							
LPC1759FBD80	LPC1759FBD80,551	512	32	16	16	64	no	Device/Host/OTG	2	yes	yes	52	120
LPC1758FBD80	LPC1758FBD80Y	512	32	16	16	64	yes	Device/Host/OTG	2	yes	yes	52	100
LPC1756FBD80	LPC1756FBD80/CP327	256	16	16	-	32	no	Device/Host/OTG	2	yes	yes	52	100
LPC1754FBD80	LPC1754FBD80,551	128	16	16	-	32	no	Device/Host/OTG	1	no	yes	52	100
LPC1752FBD80	LPC1752FBD80,551	64	16	-	-	16	no	Device only	1	no	no	52	100
LPC1751FBD80	LPC1751FBD80,551	32	8	-	-	8	no	Device only	1	no	no	52	100

6. Block diagram



Grey-shaded blocks represent peripherals with connection to the GPDMA.

Fig 1. Block diagram

Table 4. Pin description *…continued*

Symbol	Pin	Type	Description
P0[7]/I2STX_CLK/ SCK1/MAT2[1]	63[1]	I/O	**P0[7] —** General purpose digital input/output pin.
		I/O	**I2STX_CLK —** Transmit Clock. It is driven by the master and received by the slave. Corresponds to the signal SCK in the *I²S-bus specification*. (LPC1759/58/56 only).
		I/O	**SCK1 —** Serial Clock for SSP1.
		O	**MAT2[1] —** Match output for Timer 2, channel 1.
P0[8]/I2STX_WS/ MISO1/MAT2[2]	62[1]	I/O	**P0[8] —** General purpose digital input/output pin.
		I/O	**I2STX_WS —** Transmit Word Select. It is driven by the master and received by the slave. Corresponds to the signal WS in the *I²S-bus specification*. (LPC1759/58/56 only).
		I/O	**MISO1 —** Master In Slave Out for SSP1.
		O	**MAT2[2] —** Match output for Timer 2, channel 2.
P0[9]/I2STX_SDA/ MOSI1/MAT2[3]	61[1]	I/O	**P0[9] —** General purpose digital input/output pin.
		I/O	**I2STX_SDA —** Transmit data. It is driven by the transmitter and read by the receiver. Corresponds to the signal SD in the *I²S-bus specification*. (LPC1759/58/56 only).
		I/O	**MOSI1 —** Master Out Slave In for SSP1.
		O	**MAT2[3] —** Match output for Timer 2, channel 3.
P0[10]/TXD2/ SDA2/MAT3[0]	39[1]	I/O	**P0[10] —** General purpose digital input/output pin.
		O	**TXD2 —** Transmitter output for UART2.
		I/O	**SDA2 —** I²C2 data input/output (this is not an open-drain pin).
		O	**MAT3[0] —** Match output for Timer 3, channel 0.
P0[11]/RXD2/ SCL2/MAT3[1]	40[1]	I/O	**P0[11] —** General purpose digital input/output pin.
		I	**RXD2 —** Receiver input for UART2.
		I/O	**SCL2 —** I²C2 clock input/output (this is not an open-drain pin).
		O	**MAT3[1] —** Match output for Timer 3, channel 1.
P0[15]/TXD1/ SCK0/SCK	47[1]	I/O	**P0[15] —** General purpose digital input/output pin.
		O	**TXD1 —** Transmitter output for UART1.
		I/O	**SCK0 —** Serial clock for SSP0.
		I/O	**SCK —** Serial clock for SPI.
P0[16]/RXD1/ SSEL0/SSEL	48[1]	I/O	**P0[16] —** General purpose digital input/output pin.
		I	**RXD1 —** Receiver input for UART1.
		I/O	**SSEL0 —** Slave Select for SSP0.
		I/O	**SSEL —** Slave Select for SPI.
P0[17]/CTS1/ MISO0/MISO	46[1]	I/O	**P0[17] —** General purpose digital input/output pin.
		I	**CTS1 —** Clear to Send input for UART1.
		I/O	**MISO0 —** Master In Slave Out for SSP0.
		I/O	**MISO —** Master In Slave Out for SPI.
P0[18]/DCD1/ MOSI0/MOSI	45[1]	I/O	**P0[18] —** General purpose digital input/output pin.
		I	**DCD1 —** Data Carrier Detect input for UART1.
		I/O	**MOSI0 —** Master Out Slave In for SSP0.
		I/O	**MOSI —** Master Out Slave In for SPI.

Table 4. Pin description *…continued*

Symbol	Pin	Type	Description
P1[28]/MCOA2/ PCAP1[0]/ MAT0[0]	35[1]	I/O	**P1[28] —** General purpose digital input/output pin.
		O	**MCOA2 —** Motor control PWM channel 2, output A.
		I	**PCAP1[0] —** Capture input for PWM1, channel 0.
		O	**MAT0[0] —** Match output for Timer 0, channel 0.
P1[29]/MCOB2/ PCAP1[1]/ MAT0[1]	36[1]	I/O	**P1[29] —** General purpose digital input/output pin.
		O	**MCOB2 —** Motor control PWM channel 2, output B.
		I	**PCAP1[1] —** Capture input for PWM1, channel 1.
		O	**MAT0[1] —** Match output for Timer 0, channel 1.
P1[30]/V_{BUS}/ AD0[4]	18[2]	I/O	**P1[30] —** General purpose digital input/output pin.
		I	**V_{BUS} —** Monitors the presence of USB bus power. **Note:** This signal must be HIGH for USB reset to occur.
		I	**AD0[4] —** A/D converter 0, input 4.
P1[31]/SCK1/ AD0[5]	17[2]	I/O	**P1[31] —** General purpose digital input/output pin.
		I/O	**SCK1 —** Serial Clock for SSP1.
		I	**AD0[5] —** A/D converter 0, input 5.
P2[0] to P2[31]		I/O	**Port 2:** Port 2 is a 32-bit I/O port with individual direction controls for each bit. The operation of port 2 pins depends upon the pin function selected via the pin connect block. Some port pins are not available on the LQFP80 package.
P2[0]/PWM1[1]/ TXD1	60[1]	I/O	**P2[0] —** General purpose digital input/output pin.
		O	**PWM1[1] —** Pulse Width Modulator 1, channel 1 output.
		O	**TXD1 —** Transmitter output for UART1.
P2[1]/PWM1[2]/ RXD1	59[1]	I/O	**P2[1] —** General purpose digital input/output pin.
		O	**PWM1[2] —** Pulse Width Modulator 1, channel 2 output.
		I	**RXD1 —** Receiver input for UART1.
P2[2]/PWM1[3]/ CTS1/ TRACEDATA[3]	58[1]	I/O	**P2[2] —** General purpose digital input/output pin.
		O	**PWM1[3] —** Pulse Width Modulator 1, channel 3 output.
		I	**CTS1 —** Clear to Send input for UART1.
		O	**TRACEDATA[3] —** Trace data, bit 3.
P2[3]/PWM1[4]/ DCD1/ TRACEDATA[2]	55[1]	I/O	**P2[3] —** General purpose digital input/output pin.
		O	**PWM1[4] —** Pulse Width Modulator 1, channel 4 output.
		I	**DCD1 —** Data Carrier Detect input for UART1.
		O	**TRACEDATA[2] —** Trace data, bit 2.
P2[4]/PWM1[5]/ DSR1/ TRACEDATA[1]	54[1]	I/O	**P2[4] —** General purpose digital input/output pin.
		O	**PWM1[5] —** Pulse Width Modulator 1, channel 5 output.
		I	**DSR1 —** Data Set Ready input for UART1.
		O	**TRACEDATA[1] —** Trace data, bit 1.
P2[5]/PWM1[6]/ DTR1/ TRACEDATA[0]	53[1]	I/O	**P2[5] —** General purpose digital input/output pin.
		O	**PWM1[6] —** Pulse Width Modulator 1, channel 6 output.
		O	**DTR1 —** Data Terminal Ready output for UART1. Can also be configured to be an RS-485/EIA-485 output enable signal.
		O	**TRACEDATA[0] —** Trace data, bit 0.

Table 4. Pin description *…continued*

Symbol	Pin	Type	Description
XTAL1	19[9][10]	I	Input to the oscillator circuit and internal clock generator circuits.
XTAL2	20[9][10]	O	Output from the oscillator amplifier.
RTCX1	13[9][11]	I	Input to the RTC oscillator circuit.
RTCX2	15[9]	O	Output from the RTC oscillator circuit.
V_{SS}	24, 33, 43, 57, 66, 78	I	**ground:** 0 V reference.
V_{SSA}	9	I	**analog ground:** 0 V reference. This should nominally be the same voltage as V_{SS}, but should be isolated to minimize noise and error.
$V_{DD(3V3)}$	21, 42, 56, 77	I	**3.3 V supply voltage:** This is the power supply voltage for the I/O ports.
$V_{DD(REG)(3V3)}$	34, 67	I	**3.3 V voltage regulator supply voltage:** This is the supply voltage for the on-chip voltage regulator only.
V_{DDA}	8	I	**analog 3.3 V pad supply voltage:** This should be nominally the same voltage as $V_{DD(3V3)}$ but should be isolated to minimize noise and error. This voltage is used to power the ADC and DAC. This pin should be tied to 3.3 V if the ADC and DAC are not used.
VREFP	10	I	**ADC positive reference voltage:** This should be nominally the same voltage as V_{DDA} but should be isolated to minimize noise and error. Level on this pin is used as a reference for ADC and DAC. This pin should be tied to 3.3 V if the ADC and DAC are not used.
VREFN	12	I	**ADC negative reference voltage:** This should be nominally the same voltage as V_{SS} but should be isolated to minimize noise and error. Level on this pin is used as a reference for ADC and DAC.
VBAT	16[11]	I	**RTC pin power supply:** 3.3 V on this pin supplies the power to the RTC peripheral.

[1] 5 V tolerant pad providing digital I/O functions with TTL levels and hysteresis. This pin is pulled up to a voltage level of 2.3 V to 2.6 V.

[2] 5 V tolerant pad providing digital I/O functions (with TTL levels and hysteresis) and analog input. When configured as a ADC input, digital section of the pad is disabled and the pin is not 5 V tolerant. This pin is pulled up to a voltage level of 2.3 V to 2.6 V.

[3] 5 V tolerant pad providing digital I/O with TTL levels and hysteresis and analog output function. When configured as the DAC output, digital section of the pad is disabled. This pin is pulled up to a voltage level of 2.3 V to 2.6 V.

[4] Pad provides digital I/O and USB functions. It is designed in accordance with the *USB specification, revision 2.0* (Full-speed and Low-speed mode only). This pad is not 5 V tolerant.

[5] 5 V tolerant pad with 10 ns glitch filter providing digital I/O functions with TTL levels and hysteresis. This pin is pulled up to a voltage level of 2.3 V to 2.6 V.

[6] 5 V tolerant pad with TTL levels and hysteresis. Internal pull-up and pull-down resistors disabled.

[7] 5 V tolerant pad with TTL levels and hysteresis and internal pull-up resistor.

[8] 5 V tolerant pad with 20 ns glitch filter providing digital I/O function with TTL levels and hysteresis.

[9] Pad provides special analog functionality. 32 kHz crystal oscillator must be used with the RTC.

[10] When the system oscillator is not used, connect XTAL1 and XTAL2 as follows: XTAL1 can be left floating or can be grounded (grounding is preferred to reduce susceptibility to noise). XTAL2 should be left floating.

[11] When the RTC is not used, connect VBAT to $V_{DD(REG)(3V3)}$ and leave RTCX1 floating.

- Receive filtering.
- Multicast and broadcast frame support for both transmit and receive.
- Optional automatic Frame Check Sequence (FCS) insertion with Cyclic Redundancy Check (CRC) for transmit.
- Selectable automatic transmit frame padding.
- Over-length frame support for both transmit and receive allows any length frames.
- Promiscuous receive mode.
- Automatic collision back-off and frame retransmission.
- Includes power management by clock switching.
- Wake-on-LAN power management support allows system wake-up: using the receive filters or a magic frame detection filter.

- Physical interface:
  - Attachment of external PHY chip through standard RMII interface.
  - PHY register access is available via the MIIM interface.

8.12 USB interface

The Universal Serial Bus (USB) is a 4-wire bus that supports communication between a host and one or more (up to 127) peripherals. The host controller allocates the USB bandwidth to attached devices through a token-based protocol. The bus supports hot plugging and dynamic configuration of the devices. All transactions are initiated by the host controller.

The LPC1759/58/56/54 USB interface includes a device, Host, and OTG controller with on-chip PHY for device and Host functions. The OTG switching protocol is supported through the use of an external controller. Details on typical USB interfacing solutions can be found in Section 15.1. The LPC1752/51 include a USB device controller only.

8.12.1 USB device controller

The device controller enables 12 Mbit/s data exchange with a USB Host controller. It consists of a register interface, serial interface engine, endpoint buffer memory, and a DMA controller. The serial interface engine decodes the USB data stream and writes data to the appropriate endpoint buffer. The status of a completed USB transfer or error condition is indicated via status registers. An interrupt is also generated if enabled. When enabled, the DMA controller transfers data between the endpoint buffer and the on-chip SRAM.

8.12.1.1 Features

- Fully compliant with *USB 2.0 specification (full speed)*.
- Supports 32 physical (16 logical) endpoints with a 4 kB endpoint buffer RAM.
- Supports Control, Bulk, Interrupt and Isochronous endpoints.
- Scalable realization of endpoints at run time.
- Endpoint Maximum packet size selection (up to USB maximum specification) by software at run time.
- Supports SoftConnect and GoodLink features.

8.16 UARTs

The LPC1759/58/56/54/52/51 each contain four UARTs. In addition to standard transmit and receive data lines, UART1 also provides a full modem control handshake interface and support for RS-485/9-bit mode allowing both software address detection and automatic address detection using 9-bit mode.

The UARTs include a fractional baud rate generator. Standard baud rates such as 115200 Bd can be achieved with any crystal frequency above 2 MHz.

8.16.1 Features

- Maximum UART data bit rate of 6.25 Mbit/s.
- 16 B Receive and Transmit FIFOs.
- Register locations conform to 16C550 industry standard.
- Receiver FIFO trigger points at 1 B, 4 B, 8 B, and 14 B.
- Built-in fractional baud rate generator covering wide range of baud rates without a need for external crystals of particular values.
- Fractional divider for baud rate control, auto baud capabilities and FIFO control mechanism that enables software flow control implementation.
- UART1 equipped with standard modem interface signals. This module also provides full support for hardware flow control (auto-CTS/RTS).
- Support for RS-485/9-bit/EIA-485 mode (UART1).
- UART3 includes an IrDA mode to support infrared communication.
- All UARTs have DMA support.

8.17 SPI serial I/O controller

The LPC1759/58/56/54/52/51 contain one SPI controller. SPI is a full duplex serial interface designed to handle multiple masters and slaves connected to a given bus. Only a single master and a single slave can communicate on the interface during a given data transfer. During a data transfer the master always sends 8 bits to 16 bits of data to the slave, and the slave always sends 8 bits to 16 bits of data to the master.

8.17.1 Features

- Maximum SPI data bit rate of 12.5 Mbit/s
- Compliant with SPI specification
- Synchronous, serial, full duplex communication
- Combined SPI master and slave
- Maximum data bit rate of one eighth of the input clock rate
- 8 bits to 16 bits per transfer

8.18 SSP serial I/O controller

The LPC1759/58/56/54/52/51 contain two SSP controllers. The SSP controller is capable of operation on a SPI, 4-wire SSI, or Microwire bus. It can interact with multiple masters and slaves on the bus. Only a single master and a single slave can communicate on the

- Pulse period and width can be any number of timer counts. This allows complete flexibility in the trade-off between resolution and repetition rate. All PWM outputs will occur at the same repetition rate.
- Double edge controlled PWM outputs can be programmed to be either positive going or negative going pulses.
- Match register updates are synchronized with pulse outputs to prevent generation of erroneous pulses. Software must ‘release’ new match values before they can become effective.
- May be used as a standard 32-bit timer/counter with a programmable 32-bit prescaler if the PWM mode is not enabled.

8.23 Motor control PWM

The motor control PWM is a specialized PWM supporting 3-phase motors and other combinations. Feedback inputs are provided to automatically sense rotor position and use that information to ramp speed up or down. At the same time, the motor control PWM is highly configurable for other generalized timing, counting, capture, and compare applications.

8.24 Quadrature Encoder Interface (QEI)

A quadrature encoder, also known as a 2-channel incremental encoder, converts angular displacement into two pulse signals. By monitoring both the number of pulses and the relative phase of the two signals, the user can track the position, direction of rotation, and velocity. In addition, a third channel, or index signal, can be used to reset the position counter. The quadrature encoder interface decodes the digital pulses from a quadrature encoder wheel to integrate position over time and determine direction of rotation. In addition, the QEI can capture the velocity of the encoder wheel.

8.24.1 Features

- Tracks encoder position.
- Increments/decrements depending on direction.
- Programmable for 2× or 4× position counting.
- Velocity capture using built-in timer.
- Velocity compare function with “less than” interrupt.
- Uses 32-bit registers for position and velocity.
- Three position compare registers with interrupts.
- Index counter for revolution counting.
- Index compare register with interrupts.
- Can combine index and position interrupts to produce an interrupt for whole and partial revolution displacement.
- Digital filter with programmable delays for encoder input signals.
- Can accept decoded signal inputs (clk and direction).
- Connected to APB.

8.29.2 Main PLL (PLL0)

The PLL0 accepts an input clock frequency in the range of 32 kHz to 25 MHz. The input frequency is multiplied up to a high frequency, then divided down to provide the actual clock used by the CPU and/or the USB block.

The PLL0 input, in the range of 32 kHz to 25 MHz, may initially be divided down by a value ‘N’, which may be in the range of 1 to 256. This input division provides a wide range of output frequencies from the same input frequency.

Following the PLL0 input divider is the PLL0 multiplier. This can multiply the input divider output through the use of a Current Controlled Oscillator (CCO) by a value ‘M’, in the range of 1 through 32768. The resulting frequency must be in the range of 275 MHz to 550 MHz. The multiplier works by dividing the CCO output by the value of M, then using a phase-frequency detector to compare the divided CCO output to the multiplier input. The error value is used to adjust the CCO frequency.

The PLL0 is turned off and bypassed following a chip Reset and by entering Power-down mode. PLL0 is enabled by software only. The program must configure and activate the PLL0, wait for the PLL0 to lock, and then connect to the PLL0 as a clock source.

8.29.3 USB PLL (PLL1)

The LPC1759/58/56/54/52/51 contain a second, dedicated USB PLL1 to provide clocking for the USB interface.

The PLL1 receives its clock input from the main oscillator only and provides a fixed 48 MHz clock to the USB block only. The PLL1 is disabled and powered off on reset. If the PLL1 is left disabled, the USB clock will be supplied by the 48 MHz clock from the main PLL0.

The PLL1 accepts an input clock frequency in the range of 10 MHz to 25 MHz only. The input frequency is multiplied up the range of 48 MHz for the USB clock using a Current Controlled Oscillators (CCO). It is insured that the PLL1 output has a 50 % duty cycle.

8.29.4 Wake-up timer

The LPC1759/58/56/54/52/51 begin operation at power-up and when awakened from Power-down mode by using the 4 MHz IRC oscillator as the clock source. This allows chip operation to resume quickly. If the main oscillator or the PLL is needed by the application, software will need to enable these features and wait for them to stabilize before they are used as a clock source.

When the main oscillator is initially activated, the wake-up timer allows software to ensure that the main oscillator is fully functional before the processor uses it as a clock source and starts to execute instructions. This is important at power on, all types of Reset, and whenever any of the aforementioned functions are turned off for any reason. Since the oscillator and other functions are turned off during Power-down mode, any wake-up of the processor from Power-down mode makes use of the wake-up Timer.

The Wake-up Timer monitors the crystal oscillator to check whether it is safe to begin code execution. When power is applied to the chip, or when some event caused the chip to exit Power-down mode, some time is required for the oscillator to produce a signal of sufficient amplitude to drive the clock logic. The amount of time depends on many factors, including the rate of $V_{DD(3V3)}$ ramp (in the case of power on), the type of crystal and its

On the LPC1759/58/56/54/52/51, I/O pads are powered by the 3.3 V ($V_{DD(3V3)}$) pins, while the $V_{DD(REG)(3V3)}$ pin powers the on-chip voltage regulator which in turn provides power to the CPU and most of the peripherals.

Depending on the LPC1759/58/56/54/52/51 application, a design can use two power options to manage power consumption.

The first option assumes that power consumption is not a concern and the design ties the $V_{DD(3V3)}$ and $V_{DD(REG)(3V3)}$ pins together. This approach requires only one 3.3 V power supply for both pads, the CPU, and peripherals. While this solution is simple, it does not support powering down the I/O pad ring “on the fly” while keeping the CPU and peripherals alive.

The second option uses two power supplies; a 3.3 V supply for the I/O pads ($V_{DD(3V3)}$) and a dedicated 3.3 V supply for the CPU ($V_{DD(REG)(3V3)}$). Having the on-chip voltage regulator powered independently from the I/O pad ring enables shutting down of the I/O pad power supply “on the fly”, while the CPU and peripherals stay active.

The VBAT pin supplies power only to the RTC domain. The RTC requires a minimum of power to operate, which can be supplied by an external battery. The device core power ($V_{DD(REG)(3V3)}$) is used to operate the RTC whenever $V_{DD(REG)(3V3)}$ is present. Therefore, there is no power drain from the RTC battery when $V_{DD(REG)(3V3)}$ is available.

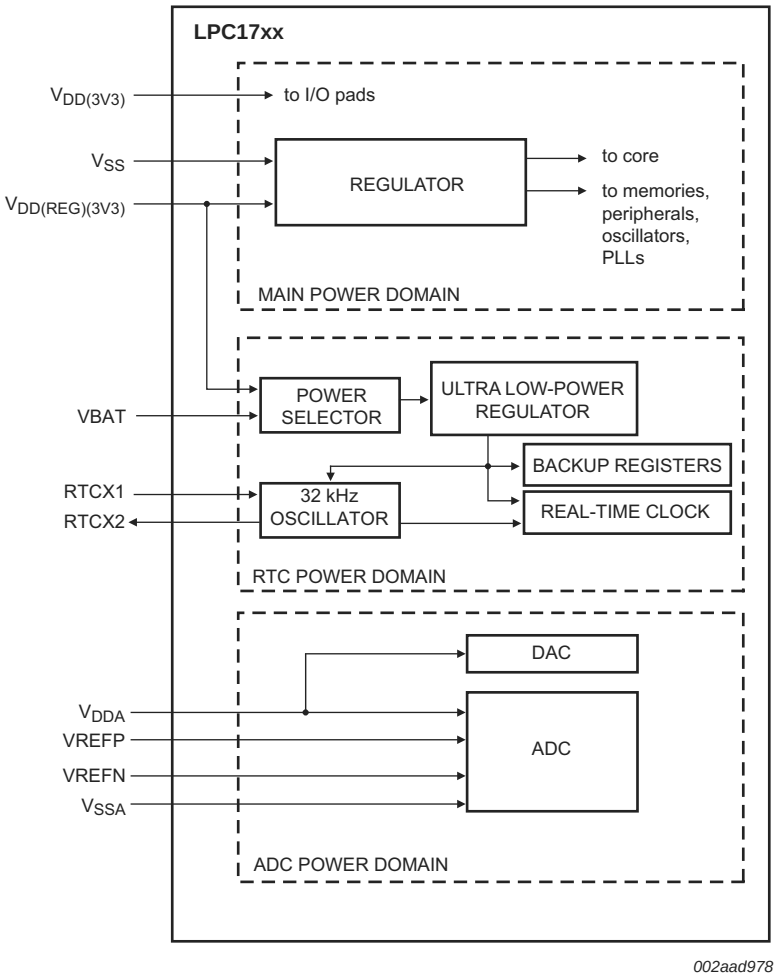


Fig 5. Power distribution

8.30 System control

8.30.1 Reset

Reset has four sources on the LPC17xx: the $\overline{\text{RESET}}$ pin, the Watchdog reset, power-on reset (POR), and the BrownOut Detection (BOD) circuit. The $\overline{\text{RESET}}$ pin is a Schmitt trigger input pin. Assertion of chip Reset by any source, once the operating voltage attains a usable level, causes the $\overline{\text{RSTOUT}}$ pin to go LOW and starts the wake-up timer (see description in Section 8.29.4). The wake-up timer ensures that reset remains asserted until the external Reset is de-asserted, the oscillator is running, a fixed number of clocks have passed, and the flash controller has completed its initialization. Once reset is de-asserted, or, in case of a BOD-triggered reset, once the voltage rises above the BOD threshold, the $\overline{\text{RSTOUT}}$ pin goes HIGH.

When the internal Reset is removed, the processor begins executing at address 0, which is initially the Reset vector mapped from the boot block. At that point, all of the processor and peripheral registers have been initialized to predetermined values.

8.30.5 AHB multilayer matrix

The LPC1759/58/56/54/52/51 use an AHB multilayer matrix. This matrix connects the instruction (I-code) and data (D-code) CPU buses of the ARM Cortex-M3 to the flash memory, the main (32 kB) static RAM, and the Boot ROM. The GPDMA can also access all of these memories. The peripheral DMA controllers, Ethernet (LPC1758 only) and USB, can access all SRAM blocks. Additionally, the matrix connects the CPU system bus and all of the DMA controllers to the various peripheral functions.

8.30.6 External interrupt inputs

The LPC1759/58/56/54/52/51 include up to 30 edge sensitive interrupt inputs combined with one level sensitive external interrupt input as selectable pin function. The external interrupt input can optionally be used to wake up the processor from Power-down mode.

8.30.7 Memory mapping control

The Cortex-M3 incorporates a mechanism that allows remapping the interrupt vector table to alternate locations in the memory map. This is controlled via the Vector Table Offset Register contained in the NVIC.

The vector table may be located anywhere within the bottom 1 GB of Cortex-M3 address space. The vector table must be located on a 128 word (512 byte) boundary because the NVIC on the LPC1759/58/56/54/52/51 is configured for 128 total interrupts.

8.31 Emulation and debugging

Debug and trace functions are integrated into the ARM Cortex-M3. Serial wire debug and trace functions are supported in addition to a standard JTAG debug and parallel trace functions. The ARM Cortex-M3 is configured to support up to eight breakpoints and four watch points.

11. Static characteristics

Table 7. Static characteristics

T_{amb} = −40 °C to +85 °C, unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ[1]	Max	Unit
Supply pins							
$V_{DD(3V3)}$	supply voltage (3.3 V)	external rail	[2]	2.4	3.3	3.6	V
$V_{DD(REG)(3V3)}$	regulator supply voltage (3.3 V)			2.4	3.3	3.6	V
V_{DDA}	analog 3.3 V pad supply voltage		[3][4]	2.5	3.3	3.6	V
$V_{i(VBAT)}$	input voltage on pin VBAT		[5]	2.1	3.3	3.6	V
$V_{i(VREFP)}$	input voltage on pin VREFP		[3]	2.5	3.3	V_{DDA}	V
$I_{DD(REG)(3V3)}$	regulator supply current (3.3 V)	active mode; code `while(1){}` executed from flash; all peripherals disabled; PCLK = $CCLK/8$					
		CCLK = 12 MHz; PLL disabled	[6][7]	-	7	-	mA
		CCLK = 100 MHz; PLL enabled	[6][7]	-	42	-	mA
		CCLK = 100 MHz; PLL enabled (LPC1759)	[6][8]		50		
		CCLK = 120 MHz; PLL enabled (LPC1759)	[6][8]	-	67	-	mA
		sleep mode	[6][9]	-	2	-	mA
		deep sleep mode	[6][10]	-	240	-	μA
		power-down mode	[6][10]	-	31	-	μA
		deep power-down mode; RTC running	[11]	-	630	-	nA
I_{BAT}	battery supply current	Deep power-down mode; RTC running					
		$V_{DD(REG)(3V3)}$ present	[12]	-	530	-	nA
		$V_{DD(REG)(3V3)}$ not present	[13]	-	1.1	-	μA
$I_{DD(IO)}$	I/O supply current	deep sleep mode	[14][15]	-	40	-	nA
		power-down mode	[14][15]	-	40	-	nA
		deep power-down mode	[14]	-	10	-	nA

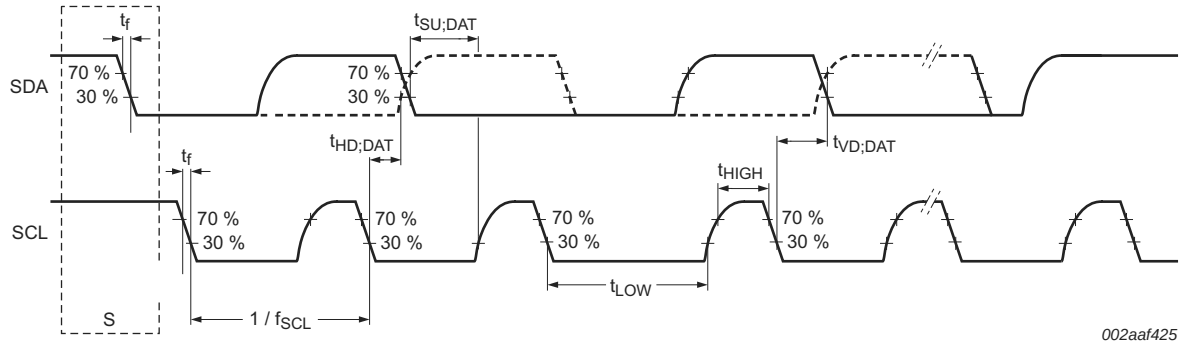


Fig 16. I²C-bus pins clock timing

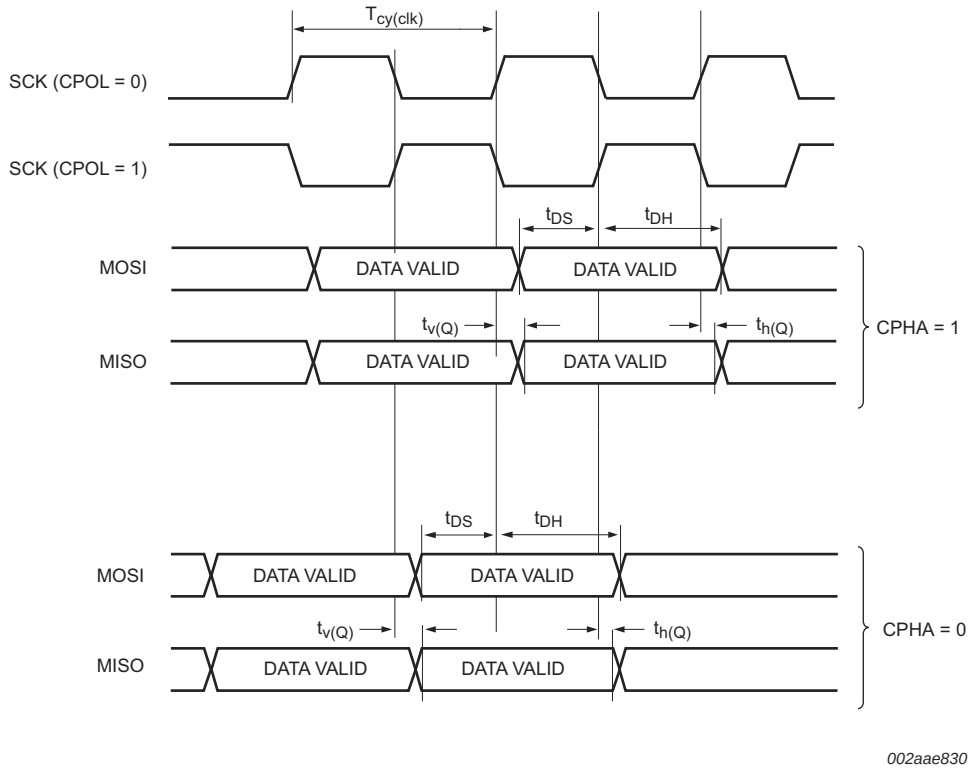


Fig 20. SSP slave timing in SPI mode

Table 19. ADC characteristics (lower resolution)

T_{amb} = −40 °C to +85 °C unless otherwise specified; 12-bit ADC used as 10-bit resolution ADC.[1]

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
E_D	differential linearity error		[2][3]	-	±1	-	LSB
$E_{L(adj)}$	integral non-linearity		[4]	-	±1.5	-	LSB
E_O	offset error		[5]	-	±2	-	LSB
E_G	gain error		[6]	-	±2	-	LSB
$f_{clk(ADC)}$	ADC clock frequency	$3.0\ V \leq V_{DDA} \leq 3.6\ V$		-	-	33	MHz
		$2.7\ V \leq V_{DDA} < 3.0\ V$		-	-	25	MHz
$f_{c(ADC)}$	ADC conversion frequency	$3\ V \leq V_{DDA} \leq 3.6\ V$	[7]	-	-	500	kHz
		$2.7\ V \leq V_{DDA} < 3.0\ V$	[7]	-	-	400	kHz

[1] V_{DDA} and VREFP should be tied to $V_{DD(3V3)}$ if the ADC and DAC are not used.

[2] The ADC is monotonic, there are no missing codes.

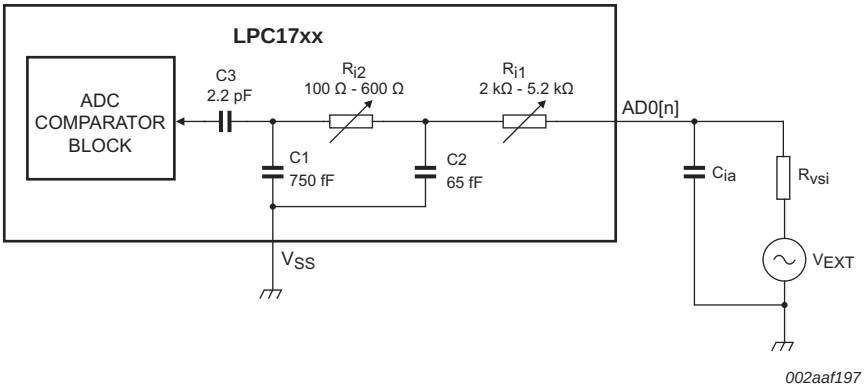
[3] The differential linearity error (E_D) is the difference between the actual step width and the ideal step width. See Figure 26.

[4] The integral non-linearity ($E_{L(adj)}$) is the peak difference between the center of the steps of the actual and the ideal transfer curve after appropriate adjustment of gain and offset errors. See Figure 26.

[5] The offset error (E_O) is the absolute difference between the straight line which fits the actual curve and the straight line which fits the ideal curve. See Figure 26.

[6] The gain error (E_G) is the relative difference in percent between the straight line fitting the actual transfer curve after removing offset error, and the straight line which fits the ideal transfer curve. See Figure 26.

[7] The conversion frequency corresponds to the number of samples per second.



The values of resistor components R_{i1} and R_{i2} vary with temperature and input voltage and are process-dependent (see Table 20).

Parasitic resistance and capacitance from the pad are not included in this figure.

Fig 27. ADC interface to pins AD0[n]

Table 20. ADC interface components

Component	Range	Description
R_{i1}	2 kΩ to 5.2 kΩ	Switch-on resistance for channel selection switch. Varies with temperature, input voltage, and process.
R_{i2}	100 Ω to 600 Ω	Switch-on resistance for the comparator input switch. Varies with temperature, input voltage, and process.
C1	750 fF	Parasitic capacitance from the ADC block level.
C2	65 fF	Parasitic capacitance from the ADC block level.
C3	2.2 pF	Sampling capacitor.

14. DAC electrical characteristics (LPC1759/58/56/54 only)

Table 21. DAC electrical characteristics

V_{DDA} = 2.7 V to 3.6 V; T_{amb} = −40 °C to +85 °C unless otherwise specified

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
E_D	differential linearity error			-	±1	-	LSB
$E_{L(adj)}$	integral non-linearity			-	±1.5	-	LSB
E_O	offset error			-	0.6	-	%
E_G	gain error			-	0.6	-	%
C_L	load capacitance			-	200	-	pF
R_L	load resistance			1	-	-	kΩ

15.6 ElectroMagnetic Compatibility (EMC)

Radiated emission measurements according to the IEC61967-2 standard using the TEM-cell method are shown for part LPC1768.

Table 24. ElectroMagnetic Compatibility (EMC) for part LPC1768 (TEM-cell method)
V_{DD} = 3.3 V; T_{amb} = 25 °C.

Parameter	Frequency band	System clock =					Unit
		12 MHz	24 MHz	48 MHz	72 MHz	100 MHz	
Input clock: IRC (4 MHz)							
maximum peak level	150 kHz to 30 MHz	−7	−6	−4	−7	−7	dBμV
	30 MHz to 150 MHz	+1	+5	+11	+16	+9	dBμV
	150 MHz to 1 GHz	−2	+4	+11	+12	+19	dBμV
IEC level[1]	-	O	O	N	M	L	-
Input clock: crystal oscillator (12 MHz)							
maximum peak level	150 kHz to 30 MHz	−5	−4	−4	−7	−8	dBμV
	30 MHz to 150 MHz	−1	+5	+10	+15	+7	dBμV
	150 MHz to 1 GHz	−1	+6	+11	+10	+16	dBμV
IEC level[1]	-	O	O	N	M	M	-

[1] IEC levels refer to Appendix D in the IEC61967-2 Specification.

18. Abbreviations

Table 25. Abbreviations

Acronym	Description
ADC	Analog-to-Digital Converter
AHB	Advanced High-performance Bus
AMBA	Advanced Microcontroller Bus Architecture
APB	Advanced Peripheral Bus
BOD	BrownOut Detection
CAN	Controller Area Network
DAC	Digital-to-Analog Converter
DMA	Direct Memory Access
EOP	End Of Packet
GPIO	General Purpose Input/Output
IRC	Internal RC
IrDA	Infrared Data Association
JTAG	Joint Test Action Group
MAC	Media Access Control
MIIM	Media Independent Interface Management
OTG	On-The-Go
PHY	Physical Layer
PLL	Phase-Locked Loop
PWM	Pulse Width Modulator
RMII	Reduced Media Independent Interface
SE0	Single Ended Zero
SPI	Serial Peripheral Interface
SSI	Serial Synchronous Interface
SSP	Synchronous Serial Port
TTL	Transistor-Transistor Logic
UART	Universal Asynchronous Receiver/Transmitter
USB	Universal Serial Bus

19. References

[1] LPC176x/5x User manual UM10360:
http://www.nxp.com/documents/user_manual/UM10360.pdf

[2] LPC175x Errata sheet:
http://www.nxp.com/documents/errata_sheet/ES_LPC175X.pdf

[3] Technical note ADC design guidelines:
http://www.nxp.com/documents/technical_note/TN00009.pdf

20. Revision history

Table 26. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
LPC1759_58_56_54_52_51 v.8.6	20150818	Product data sheet	-	LPC1759_58_56_54_52_51 v.8.5
Modifications:	• Updated max value of $t_{v(Q)}$ (data output valid time) in SPI mode to $3*T_{cy(PCLK)}$ + 2.5 ns. See Table 15 “Dynamic characteristics: SSP pins in SPI mode”. • Updated Section 2 “Features and benefits”: Added Boundary scan Description Language (BSDL) is not available for this device. • Updated Figure 3 “LPC1759/58/56/54/52/51 memory map”: APB0 slot 7 (0x4001C000) was "reserved" and changed it to I2C0. • Added a column for GPIO pins and device order part number to the ordering options table. See Table 2 “Ordering options”.			
LPC1759_58_56_54_52_51 v.8.5	20140624	Product data sheet	-	LPC1759_58_56_54_52_51 v.8.4
Modifications:	• SSP timing diagram updated. SSP timing parameters $t_{v(Q)}$, $t_{h(Q)}$, t_{DS}, and t_{DH} added. See Section 12.7 “SSP interface”. • SSP maximum bit rate in master mode corrected to 33 Mbit/s. • Parameter $T_{j(max)}$ added in Table 5 “Limiting values”. • Description of capture channels corrected in Section 8.21.1.			
LPC1759_58_56_54_52_51 v.8.4	20140404	Product data sheet	-	LPC1759_58_56_54_52_51 v.8.3
Modifications:	• Table 4 “Pin description”: Changed RX_MCLK and TX_MCLK type from INPUT to OUTPUT.			
LPC1759_58_56_54_52_51 v.8.3	20140108	Product data sheet	-	LPC1759_58_56_54_52_51 v.8.2
Modifications:	• Table 6 “Thermal resistance (±15 %)”: Added ±15 % to table title.			
LPC1759_58_56_54_52_51 v.8.2	20131018	Product data sheet	-	LPC1759_58_56_54_52_51 v.8.1
Modifications:	• Table 5 “Limiting values”: Removed condition “5 V tolerant open-drain pins...” from V_I. • Table 7 “Static characteristics”: – Added Table note 3 “VDDA and VREFP should be tied to VDD(3V3) if the ADC and DAC are not used.” – Added Table note 4 “VDDA for DAC specs are from 2.7 V to 3.6 V.” – V_{DDA}/VREFP spec changed from 2.7 V to 2.5 V. • Table 18 “ADC characteristics (full resolution)”: – Added Table note 1 “VDDA and VREFP should be tied to VDD(3V3) if the ADC and DAC are not used.” – V_{DDA} changed from 2.7 V to 2.5 V. • Table 19 “ADC characteristics (lower resolution)”: Added Table note 1 “VDDA and VREFP should be tied to VDD(3V3) if the ADC and DAC are not used.”			