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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Discontinued at Digi-Key
Core Processor	ARM® Cortex®-M3
Core Size	32-Bit Single-Core
Speed	100MHz
Connectivity	CANbus, I²C, IrDA, Microwire, SPI, SSI, SSP, UART/USART, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, I²S, Motor Control PWM, POR, PWM, WDT
Number of I/O	52
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	32K x 8
Voltage - Supply (Vcc/Vdd)	2.4V ~ 3.6V
Data Converters	A/D 6x12b; D/A 1x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	80-LQFP
Supplier Device Package	80-LQFP (12x12)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/lpc1756fbd80-551

- ◆ WatchDog Timer (WDT). The WDT can be clocked from the internal RC oscillator, the RTC oscillator, or the APB clock.
- ◆ ARM Cortex-M3 system tick timer, including an external clock input option.
- ◆ Repetitive Interrupt Timer (RIT) provides programmable and repeating timed interrupts.
- ◆ Each peripheral has its own clock divider for further power savings.

- Standard JTAG debug interface for compatibility with existing tools. Serial Wire Debug and Serial Wire Trace Port options. Boundary scan Description Language (BSDL) is not available for this device.
- Emulation trace module enables non-intrusive, high-speed real-time tracing of instruction execution.
- Integrated PMU (Power Management Unit) automatically adjusts internal regulators to minimize power consumption during Sleep, Deep sleep, Power-down, and Deep power-down modes.
- Four reduced power modes: Sleep, Deep-sleep, Power-down, and Deep power-down.
- Single 3.3 V power supply (2.4 V to 3.6 V).
- One external interrupt input configurable as edge/level sensitive. All pins on Port 0 and Port 2 can be used as edge sensitive interrupt sources.
- Non-maskable Interrupt (NMI) input.
- The Wakeup Interrupt Controller (WIC) allows the CPU to automatically wake up from any priority interrupt that can occur while the clocks are stopped in Deep sleep, Power-down, and Deep power-down modes.
- Processor wake-up from Power-down mode via any interrupt able to operate during Power-down mode (includes external interrupts, RTC interrupt, USB activity, Ethernet wake-up interrupt (LPC1758 only), CAN bus activity, Port 0/2 pin interrupt, and NMI).
- Brownout detect with separate threshold for interrupt and forced reset.
- Power-On Reset (POR).
- Crystal oscillator with an operating range of 1 MHz to 25 MHz.
- 4 MHz internal RC oscillator trimmed to 1 % accuracy that can optionally be used as a system clock.
- PLL allows CPU operation up to the maximum CPU rate without the need for a high-frequency crystal. May be run from the main oscillator, the internal RC oscillator, or the RTC oscillator.
- USB PLL for added flexibility.
- Code Read Protection (CRP) with different security levels.
- Unique device serial number for identification purposes.
- Available as 80-pin LQFP package (12 mm × 12 mm × 1.4 mm).

3. Applications

- eMetering
- Lighting
- Industrial networking
- Alarm systems
- White goods
- Motor control

4. Ordering information

Table 1. Ordering information

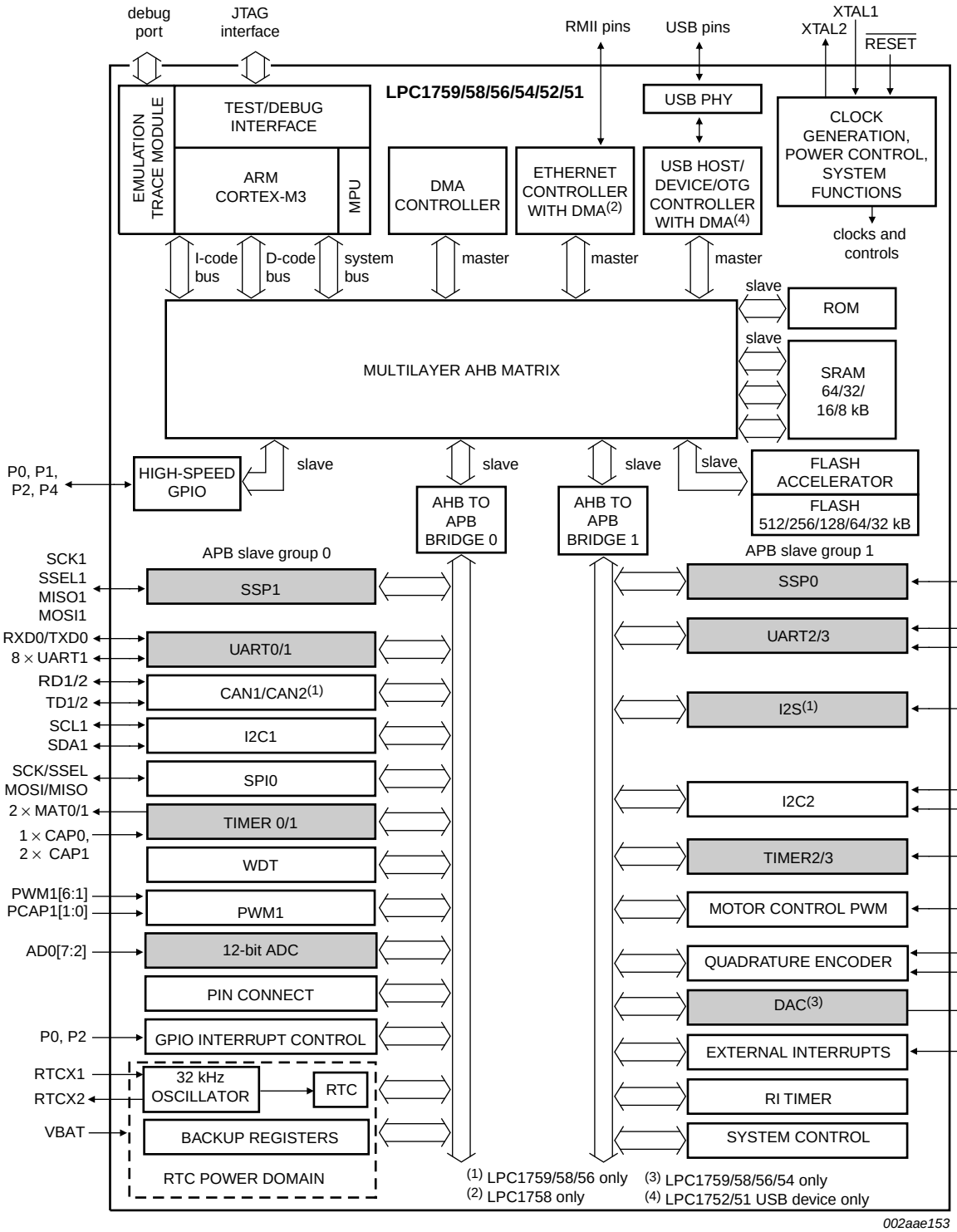
Type number	Package		
	Name	Description	Version
LPC1759FBD80	LQFP80	plastic low-profile quad package; 80 leads; body 12 × 12 × 1.4 mm	SOT315-1
LPC1758FBD80	LQFP80	plastic low-profile quad package; 80 leads; body 12 × 12 × 1.4 mm	SOT315-1
LPC1756FBD80	LQFP80	plastic low-profile quad package; 80 leads; body 12 × 12 × 1.4 mm	SOT315-1
LPC1754FBD80	LQFP80	plastic low-profile quad package; 80 leads; body 12 × 12 × 1.4 mm	SOT315-1
LPC1752FBD80	LQFP80	plastic low-profile quad package; 80 leads; body 12 × 12 × 1.4 mm	SOT315-1
LPC1751FBD80	LQFP80	plastic low-profile quad package; 80 leads; body 12 × 12 × 1.4 mm	SOT315-1

4.1 Ordering options

Table 2. Ordering options

Type number	Device order part number	Flash (kB)	SRAM in kB				Ethernet	USB	CAN	I^2S-bus	DAC	GPIO	Maximum CPU operating frequency (MHz)
			CPU	AHB SRAM0	AHB SRAM1	Total							
LPC1759FBD80	LPC1759FBD80,551	512	32	16	16	64	no	Device/Host/OTG	2	yes	yes	52	120
LPC1758FBD80	LPC1758FBD80Y	512	32	16	16	64	yes	Device/Host/OTG	2	yes	yes	52	100
LPC1756FBD80	LPC1756FBD80/CP327	256	16	16	-	32	no	Device/Host/OTG	2	yes	yes	52	100
LPC1754FBD80	LPC1754FBD80,551	128	16	16	-	32	no	Device/Host/OTG	1	no	yes	52	100
LPC1752FBD80	LPC1752FBD80,551	64	16	-	-	16	no	Device only	1	no	no	52	100
LPC1751FBD80	LPC1751FBD80,551	32	8	-	-	8	no	Device only	1	no	no	52	100

6. Block diagram



Grey-shaded blocks represent peripherals with connection to the GPDMA.

Fig 1. Block diagram

Table 4. Pin description *…continued*

Symbol	Pin	Type	Description
P0[7]/I2STX_CLK/ SCK1/MAT2[1]	63[1]	I/O	**P0[7] —** General purpose digital input/output pin.
		I/O	**I2STX_CLK —** Transmit Clock. It is driven by the master and received by the slave. Corresponds to the signal SCK in the *I²S-bus specification*. (LPC1759/58/56 only).
		I/O	**SCK1 —** Serial Clock for SSP1.
		O	**MAT2[1] —** Match output for Timer 2, channel 1.
P0[8]/I2STX_WS/ MISO1/MAT2[2]	62[1]	I/O	**P0[8] —** General purpose digital input/output pin.
		I/O	**I2STX_WS —** Transmit Word Select. It is driven by the master and received by the slave. Corresponds to the signal WS in the *I²S-bus specification*. (LPC1759/58/56 only).
		I/O	**MISO1 —** Master In Slave Out for SSP1.
		O	**MAT2[2] —** Match output for Timer 2, channel 2.
P0[9]/I2STX_SDA/ MOSI1/MAT2[3]	61[1]	I/O	**P0[9] —** General purpose digital input/output pin.
		I/O	**I2STX_SDA —** Transmit data. It is driven by the transmitter and read by the receiver. Corresponds to the signal SD in the *I²S-bus specification*. (LPC1759/58/56 only).
		I/O	**MOSI1 —** Master Out Slave In for SSP1.
		O	**MAT2[3] —** Match output for Timer 2, channel 3.
P0[10]/TXD2/ SDA2/MAT3[0]	39[1]	I/O	**P0[10] —** General purpose digital input/output pin.
		O	**TXD2 —** Transmitter output for UART2.
		I/O	**SDA2 —** I²C2 data input/output (this is not an open-drain pin).
		O	**MAT3[0] —** Match output for Timer 3, channel 0.
P0[11]/RXD2/ SCL2/MAT3[1]	40[1]	I/O	**P0[11] —** General purpose digital input/output pin.
		I	**RXD2 —** Receiver input for UART2.
		I/O	**SCL2 —** I²C2 clock input/output (this is not an open-drain pin).
		O	**MAT3[1] —** Match output for Timer 3, channel 1.
P0[15]/TXD1/ SCK0/SCK	47[1]	I/O	**P0[15] —** General purpose digital input/output pin.
		O	**TXD1 —** Transmitter output for UART1.
		I/O	**SCK0 —** Serial clock for SSP0.
		I/O	**SCK —** Serial clock for SPI.
P0[16]/RXD1/ SSEL0/SSEL	48[1]	I/O	**P0[16] —** General purpose digital input/output pin.
		I	**RXD1 —** Receiver input for UART1.
		I/O	**SSEL0 —** Slave Select for SSP0.
		I/O	**SSEL —** Slave Select for SPI.
P0[17]/CTS1/ MISO0/MISO	46[1]	I/O	**P0[17] —** General purpose digital input/output pin.
		I	**CTS1 —** Clear to Send input for UART1.
		I/O	**MISO0 —** Master In Slave Out for SSP0.
		I/O	**MISO —** Master In Slave Out for SPI.
P0[18]/DCD1/ MOSI0/MOSI	45[1]	I/O	**P0[18] —** General purpose digital input/output pin.
		I	**DCD1 —** Data Carrier Detect input for UART1.
		I/O	**MOSI0 —** Master Out Slave In for SSP0.
		I/O	**MOSI —** Master Out Slave In for SPI.

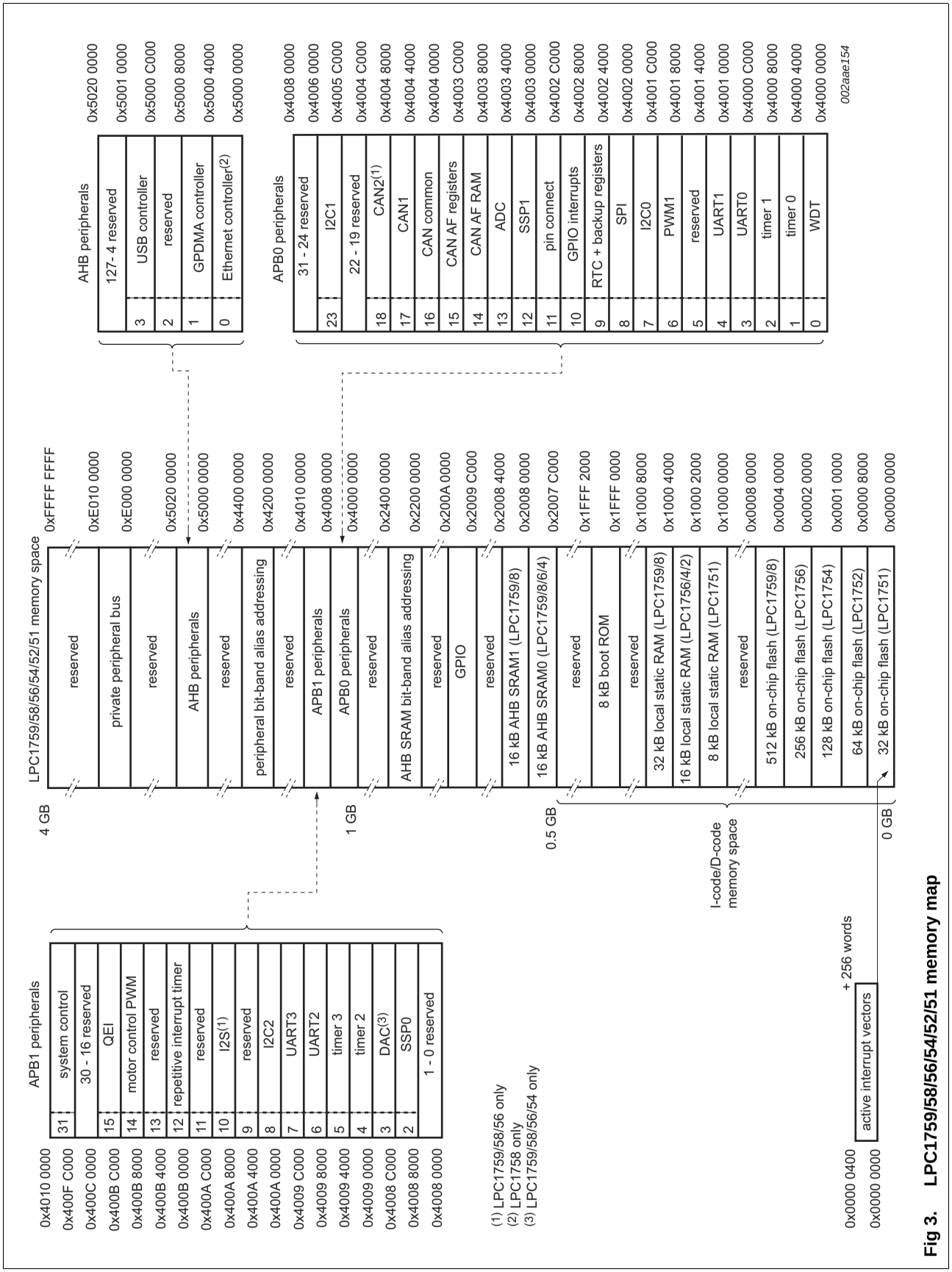


Fig 3. LPC1759/58/56/54/52/51 memory map

8.7 Nested Vectored Interrupt Controller (NVIC)

The NVIC is an integral part of the Cortex-M3. The tight coupling to the CPU allows for low interrupt latency and efficient processing of late arriving interrupts.

8.7.1 Features

- Controls system exceptions and peripheral interrupts
- In the LPC1759/58/56/54/52/51, the NVIC supports 33 vectored interrupts
- 32 programmable interrupt priority levels, with hardware priority level masking
- Relocatable vector table
- Non-Maskable Interrupt (NMI)
- Software interrupt generation

8.7.2 Interrupt sources

Each peripheral device has one interrupt line connected to the NVIC but may have several interrupt flags. Individual interrupt flags may also represent more than one interrupt source.

Any pin on Port 0 and Port 2 (total of 30 pins) regardless of the selected function, can be programmed to generate an interrupt on a rising edge, a falling edge, or both.

8.8 Pin connect block

The pin connect block allows selected pins of the microcontroller to have more than one function. Configuration registers control the multiplexers to allow connection between the pin and the on-chip peripherals.

Peripherals should be connected to the appropriate pins prior to being activated and prior to any related interrupt(s) being enabled. Activity of any enabled peripheral function that is not mapped to a related pin should be considered undefined.

Most pins can also be configured as open-drain outputs or to have a pull-up, pull-down, or no resistor enabled.

8.9 General purpose DMA controller

The GPDMA is an AMBA AHB compliant peripheral allowing selected LPC1759/58/56/54/52/51 peripherals to have DMA support.

The GPDMA enables peripheral-to-memory, memory-to-peripheral, peripheral-to-peripheral, and memory-to-memory transactions. The source and destination areas can each be either a memory region or a peripheral, and can be accessed through the AHB master. The GPDMA controller allows data transfers between the USB and Ethernet (LPC1758 only) controllers and the various on-chip SRAM areas. The supported APB peripherals are SSP0/1, all UARTs, the I^2S-bus interface, the ADC, and the DAC. Two match signals for each timer can be used to trigger DMA transfers.

Remark: Note that the DAC is not available on the LPC1752/51, and the I^2S-bus interface is not available on the LPC1754/52/51.

8.9.1 Features

- Eight DMA channels. Each channel can support an unidirectional transfer.
- 16 DMA request lines.
- Single DMA and burst DMA request signals. Each peripheral connected to the DMA Controller can assert either a burst DMA request or a single DMA request. The DMA burst size is set by programming the DMA Controller.
- Memory-to-memory, memory-to-peripheral, peripheral-to-memory, and peripheral-to-peripheral transfers are supported.
- Scatter or gather DMA is supported through the use of linked lists. This means that the source and destination areas do not have to occupy contiguous areas of memory.
- Hardware DMA channel priority.
- AHB slave DMA programming interface. The DMA Controller is programmed by writing to the DMA control registers over the AHB slave interface.
- One AHB bus master for transferring data. The interface transfers data when a DMA request goes active.
- 32-bit AHB master bus width.
- Incrementing or non-incrementing addressing for source and destination.
- Programmable DMA burst size. The DMA burst size can be programmed to more efficiently transfer data.
- Internal four-word FIFO per channel.
- Supports 8, 16, and 32-bit wide transactions.
- Big-endian and little-endian support. The DMA Controller defaults to little-endian mode on reset.
- An interrupt to the processor can be generated on a DMA completion or when a DMA error has occurred.
- Raw interrupt status. The DMA error and DMA count raw interrupt status can be read prior to masking.

8.10 Fast general purpose parallel I/O

Device pins that are not connected to a specific peripheral function are controlled by the GPIO registers. Pins may be dynamically configured as inputs or outputs. Separate registers allow setting or clearing any number of outputs simultaneously. The value of the output register may be read back as well as the current state of the port pins.

LPC1759/58/56/54/52/51 use accelerated GPIO functions:

- GPIO registers are accessed through the AHB multilayer bus so that the fastest possible I/O timing can be achieved.
- Mask registers allow treating sets of port bits as a group, leaving other bits unchanged.
- All GPIO registers are byte and half-word addressable.
- Entire port value can be written in one instruction.
- Support for Cortex-M3 bit banding.
- Support for use with the GPDMA controller.

- Receive filtering.
- Multicast and broadcast frame support for both transmit and receive.
- Optional automatic Frame Check Sequence (FCS) insertion with Cyclic Redundancy Check (CRC) for transmit.
- Selectable automatic transmit frame padding.
- Over-length frame support for both transmit and receive allows any length frames.
- Promiscuous receive mode.
- Automatic collision back-off and frame retransmission.
- Includes power management by clock switching.
- Wake-on-LAN power management support allows system wake-up: using the receive filters or a magic frame detection filter.

- Physical interface:
  - Attachment of external PHY chip through standard RMII interface.
  - PHY register access is available via the MIIM interface.

8.12 USB interface

The Universal Serial Bus (USB) is a 4-wire bus that supports communication between a host and one or more (up to 127) peripherals. The host controller allocates the USB bandwidth to attached devices through a token-based protocol. The bus supports hot plugging and dynamic configuration of the devices. All transactions are initiated by the host controller.

The LPC1759/58/56/54 USB interface includes a device, Host, and OTG controller with on-chip PHY for device and Host functions. The OTG switching protocol is supported through the use of an external controller. Details on typical USB interfacing solutions can be found in Section 15.1. The LPC1752/51 include a USB device controller only.

8.12.1 USB device controller

The device controller enables 12 Mbit/s data exchange with a USB Host controller. It consists of a register interface, serial interface engine, endpoint buffer memory, and a DMA controller. The serial interface engine decodes the USB data stream and writes data to the appropriate endpoint buffer. The status of a completed USB transfer or error condition is indicated via status registers. An interrupt is also generated if enabled. When enabled, the DMA controller transfers data between the endpoint buffer and the on-chip SRAM.

8.12.1.1 Features

- Fully compliant with *USB 2.0 specification (full speed)*.
- Supports 32 physical (16 logical) endpoints with a 4 kB endpoint buffer RAM.
- Supports Control, Bulk, Interrupt and Isochronous endpoints.
- Scalable realization of endpoints at run time.
- Endpoint Maximum packet size selection (up to USB maximum specification) by software at run time.
- Supports SoftConnect and GoodLink features.

8.13.1 Features

- One or two CAN controllers and buses.
- Data rates to 1 Mbit/s on each bus.
- 32-bit register and RAM access.
- Compatible with *CAN specification 2.0B, ISO 11898-1*.
- Global Acceptance Filter recognizes standard (11-bit) and extended-frame (29-bit) receive identifiers for all CAN buses.
- Acceptance Filter can provide FullCAN-style automatic reception for selected Standard Identifiers.
- FullCAN messages can generate interrupts.

8.14 12-bit ADC

The LPC1759/58/56/54/52/51 contain one ADC. It is a single 12-bit successive approximation ADC with six channels and DMA support.

8.14.1 Features

- 12-bit successive approximation ADC.
- Input multiplexing among 6 pins.
- Power-down mode.
- Measurement range VREFN to VREFP.
- 12-bit conversion rate: 200 kHz.
- Individual channels can be selected for conversion.
- Burst conversion mode for single or multiple inputs.
- Optional conversion on transition of input pin or Timer Match signal.
- Individual result registers for each ADC channel to reduce interrupt overhead.
- DMA support.

8.15 10-bit DAC (LPC1759/58/56/54 only)

The DAC allows to generate a variable analog output. The maximum output value of the DAC is VREFP.

8.15.1 Features

- 10-bit DAC
- Resistor string architecture
- Buffered output
- Power-down mode
- Selectable output drive
- Dedicated conversion timer
- DMA support

8.16 UARTs

The LPC1759/58/56/54/52/51 each contain four UARTs. In addition to standard transmit and receive data lines, UART1 also provides a full modem control handshake interface and support for RS-485/9-bit mode allowing both software address detection and automatic address detection using 9-bit mode.

The UARTs include a fractional baud rate generator. Standard baud rates such as 115200 Bd can be achieved with any crystal frequency above 2 MHz.

8.16.1 Features

- Maximum UART data bit rate of 6.25 Mbit/s.
- 16 B Receive and Transmit FIFOs.
- Register locations conform to 16C550 industry standard.
- Receiver FIFO trigger points at 1 B, 4 B, 8 B, and 14 B.
- Built-in fractional baud rate generator covering wide range of baud rates without a need for external crystals of particular values.
- Fractional divider for baud rate control, auto baud capabilities and FIFO control mechanism that enables software flow control implementation.
- UART1 equipped with standard modem interface signals. This module also provides full support for hardware flow control (auto-CTS/RTS).
- Support for RS-485/9-bit/EIA-485 mode (UART1).
- UART3 includes an IrDA mode to support infrared communication.
- All UARTs have DMA support.

8.17 SPI serial I/O controller

The LPC1759/58/56/54/52/51 contain one SPI controller. SPI is a full duplex serial interface designed to handle multiple masters and slaves connected to a given bus. Only a single master and a single slave can communicate on the interface during a given data transfer. During a data transfer the master always sends 8 bits to 16 bits of data to the slave, and the slave always sends 8 bits to 16 bits of data to the master.

8.17.1 Features

- Maximum SPI data bit rate of 12.5 Mbit/s
- Compliant with SPI specification
- Synchronous, serial, full duplex communication
- Combined SPI master and slave
- Maximum data bit rate of one eighth of the input clock rate
- 8 bits to 16 bits per transfer

8.18 SSP serial I/O controller

The LPC1759/58/56/54/52/51 contain two SSP controllers. The SSP controller is capable of operation on a SPI, 4-wire SSI, or Microwire bus. It can interact with multiple masters and slaves on the bus. Only a single master and a single slave can communicate on the

8.30.5 AHB multilayer matrix

The LPC1759/58/56/54/52/51 use an AHB multilayer matrix. This matrix connects the instruction (I-code) and data (D-code) CPU buses of the ARM Cortex-M3 to the flash memory, the main (32 kB) static RAM, and the Boot ROM. The GPDMA can also access all of these memories. The peripheral DMA controllers, Ethernet (LPC1758 only) and USB, can access all SRAM blocks. Additionally, the matrix connects the CPU system bus and all of the DMA controllers to the various peripheral functions.

8.30.6 External interrupt inputs

The LPC1759/58/56/54/52/51 include up to 30 edge sensitive interrupt inputs combined with one level sensitive external interrupt input as selectable pin function. The external interrupt input can optionally be used to wake up the processor from Power-down mode.

8.30.7 Memory mapping control

The Cortex-M3 incorporates a mechanism that allows remapping the interrupt vector table to alternate locations in the memory map. This is controlled via the Vector Table Offset Register contained in the NVIC.

The vector table may be located anywhere within the bottom 1 GB of Cortex-M3 address space. The vector table must be located on a 128 word (512 byte) boundary because the NVIC on the LPC1759/58/56/54/52/51 is configured for 128 total interrupts.

8.31 Emulation and debugging

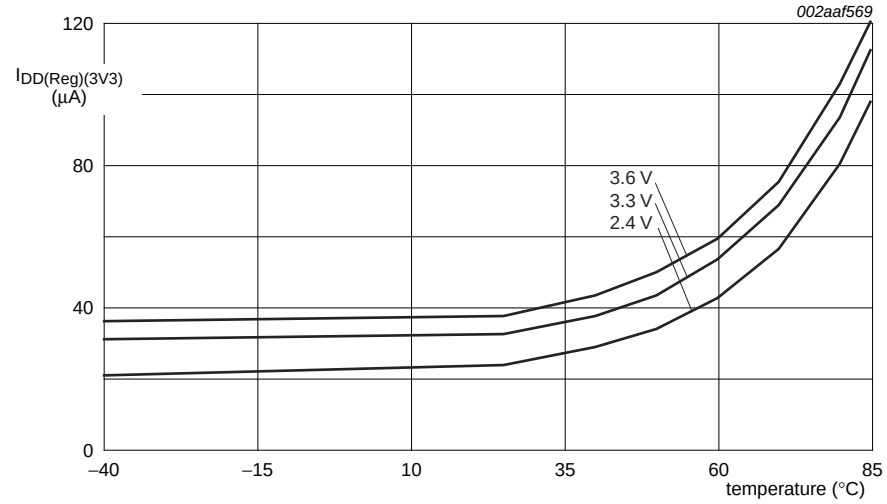
Debug and trace functions are integrated into the ARM Cortex-M3. Serial wire debug and trace functions are supported in addition to a standard JTAG debug and parallel trace functions. The ARM Cortex-M3 is configured to support up to eight breakpoints and four watch points.

11. Static characteristics

Table 7. Static characteristics

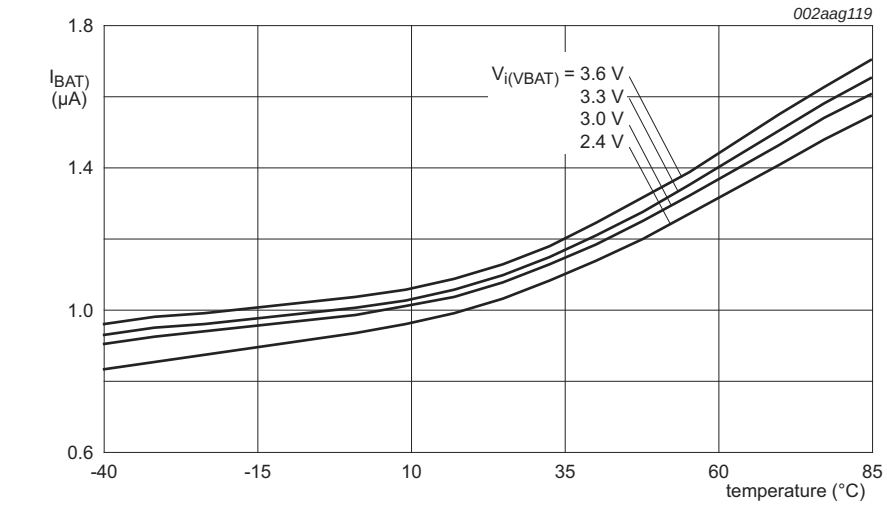
T_{amb} = −40 °C to +85 °C, unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ[1]	Max	Unit
Supply pins							
$V_{DD(3V3)}$	supply voltage (3.3 V)	external rail	[2]	2.4	3.3	3.6	V
$V_{DD(REG)(3V3)}$	regulator supply voltage (3.3 V)			2.4	3.3	3.6	V
V_{DDA}	analog 3.3 V pad supply voltage		[3][4]	2.5	3.3	3.6	V
$V_{i(VBAT)}$	input voltage on pin VBAT		[5]	2.1	3.3	3.6	V
$V_{i(VREFP)}$	input voltage on pin VREFP		[3]	2.5	3.3	V_{DDA}	V
$I_{DD(REG)(3V3)}$	regulator supply current (3.3 V)	active mode; code `while(1){}` executed from flash; all peripherals disabled; PCLK = $CCLK/8$					
		CCLK = 12 MHz; PLL disabled	[6][7]	-	7	-	mA
		CCLK = 100 MHz; PLL enabled	[6][7]	-	42	-	mA
		CCLK = 100 MHz; PLL enabled (LPC1759)	[6][8]		50		
		CCLK = 120 MHz; PLL enabled (LPC1759)	[6][8]	-	67	-	mA
		sleep mode	[6][9]	-	2	-	mA
		deep sleep mode	[6][10]	-	240	-	μA
		power-down mode	[6][10]	-	31	-	μA
		deep power-down mode; RTC running	[11]	-	630	-	nA
I_{BAT}	battery supply current	Deep power-down mode; RTC running					
		$V_{DD(REG)(3V3)}$ present	[12]	-	530	-	nA
		$V_{DD(REG)(3V3)}$ not present	[13]	-	1.1	-	μA
$I_{DD(IO)}$	I/O supply current	deep sleep mode	[14][15]	-	40	-	nA
		power-down mode	[14][15]	-	40	-	nA
		deep power-down mode	[14]	-	10	-	nA



Conditions: $V_{DD(Reg)(3V3)}$ = 3.3 V; BOD disabled.

Fig 7. Power-down mode: Typical regulator supply current $I_{DD(Reg)(3V3)}$ versus temperature



Conditions: $V_{DD(REG)(3V3)}$ floating; RTC running.

Fig 8. Deep power-down mode: Typical battery supply current I_{BAT} versus temperature

12. Dynamic characteristics

12.1 Flash memory

Table 9. Flash characteristics

T_{amb} = −40 °C to +85 °C, unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
N_{endu}	endurance		[1]	10000	100000	-	cycles
t_{ret}	retention time	powered		10	-	-	years
		unpowered		20	-	-	years
t_{er}	erase time	sector or multiple consecutive sectors		95	100	105	ms
t_{prog}	programming time		[2]	0.95	1	1.05	ms

[1] Number of program/erase cycles.

[2] Programming times are given for writing 256 bytes from RAM to the flash. Data must be written to the flash in blocks of 256 bytes.

12.2 External clock

Table 10. Dynamic characteristic: external clock

T_{amb} = −40 °C to +85 °C; $V_{DD(3V3)}$ over specified ranges.[1]

Symbol	Parameter	Conditions		Min	Typ[2]	Max	Unit
f_{osc}	oscillator frequency			1	-	25	MHz
$T_{cy(clk)}$	clock cycle time			40	-	1000	ns
t_{CHCX}	clock HIGH time			$T_{cy(clk)} \times 0.4$	-	-	ns
t_{CLCX}	clock LOW time			$T_{cy(clk)} \times 0.4$	-	-	ns
t_{CLCH}	clock rise time			-	-	5	ns
t_{CHCL}	clock fall time			-	-	5	ns

[1] Parameters are valid over operating temperature range unless otherwise specified.

[2] Typical ratings are not guaranteed. The values listed are at room temperature (25 °C), nominal supply voltages.

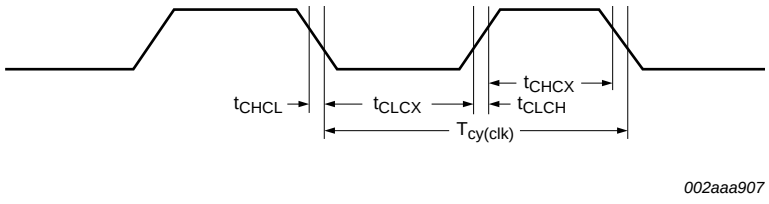


Fig 14. External clock timing (with an amplitude of at least $V_{i(RMS)}$ = 200 mV)

12.8 USB interface

Table 16. Dynamic characteristics: USB pins (full-speed)

C_L = 50 pF; R_{pu} = 1.5 kΩ on D+ to $V_{DD(3V3)}$; 3.0 V ≤ $V_{DD(3V3)}$ ≤ 3.6 V.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
t_r	rise time	10 % to 90 %		8.5	-	13.8	ns
t_f	fall time	10 % to 90 %		7.7	-	13.7	ns
t_{FRFM}	differential rise and fall time matching	t_r / t_f		-	-	109	%
V_{CRS}	output signal crossover voltage			1.3	-	2.0	V
t_{FEOPT}	source SE0 interval of EOP	see Figure 21		160	-	175	ns
t_{FDEOP}	source jitter for differential transition to SE0 transition	see Figure 21		−2	-	+5	ns
t_{JR1}	receiver jitter to next transition			−18.5	-	+18.5	ns
t_{JR2}	receiver jitter for paired transitions	10 % to 90 %		−9	-	+9	ns
t_{EOPR1}	EOP width at receiver	must reject as EOP; see Figure 21	[1]	40	-	-	ns
t_{EOPR2}	EOP width at receiver	must accept as EOP; see Figure 21	[1]	82	-	-	ns

[1] Characterized but not implemented as production test. Guaranteed by design.

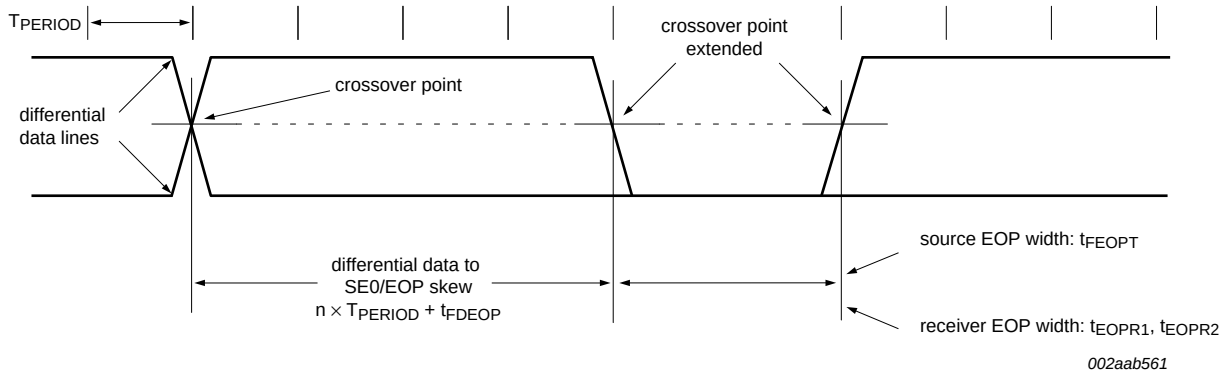


Fig 21. Differential data-to-EOP transition skew and EOP width

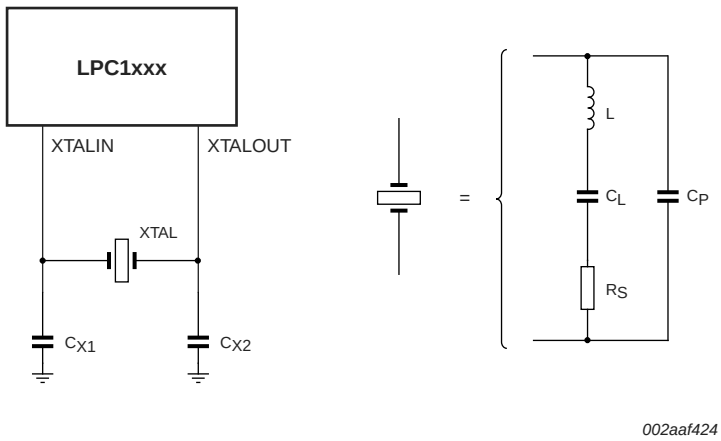


Fig 35. Oscillator modes and models: oscillation mode of operation and external crystal model used for C_{X1}/C_{X2} evaluation

Table 22. Recommended values for C_{X1}/C_{X2} in oscillation mode (crystal and external components parameters): low frequency mode

Fundamental oscillation frequency F_{OSC}	Crystal load capacitance C_L	Maximum crystal series resistance R_S	External load capacitors C_{X1}/C_{X2}
1 MHz to 5 MHz	10 pF	< 300 Ω	18 pF, 18 pF
	20 pF	< 300 Ω	39 pF, 39 pF
	30 pF	< 300 Ω	57 pF, 57 pF
5 MHz to 10 MHz	10 pF	< 300 Ω	18 pF, 18 pF
	20 pF	< 200 Ω	39 pF, 39 pF
	30 pF	< 100 Ω	57 pF, 57 pF
10 MHz to 15 MHz	10 pF	< 160 Ω	18 pF, 18 pF
	20 pF	< 60 Ω	39 pF, 39 pF
15 MHz to 20 MHz	10 pF	< 80 Ω	18 pF, 18 pF

Table 23. Recommended values for C_{X1}/C_{X2} in oscillation mode (crystal and external components parameters): high frequency mode

Fundamental oscillation frequency F_{OSC}	Crystal load capacitance C_L	Maximum crystal series resistance R_S	External load capacitors C_{X1}, C_{X2}
15 MHz to 20 MHz	10 pF	< 180 Ω	18 pF, 18 pF
	20 pF	< 100 Ω	39 pF, 39 pF
20 MHz to 25 MHz	10 pF	< 160 Ω	18 pF, 18 pF
	20 pF	< 80 Ω	39 pF, 39 pF

15.3 XTAL Printed-Circuit Board (PCB) layout guidelines

The crystal should be connected on the PCB as close as possible to the oscillator input and output pins of the chip. Take care that the load capacitors C_{x1}, C_{x2}, and C_{x3} in case of third overtone crystal usage have a common ground plane. The external components must also be connected to the ground plain. Loops must be made as small as possible in

15.5 Reset pin configuration

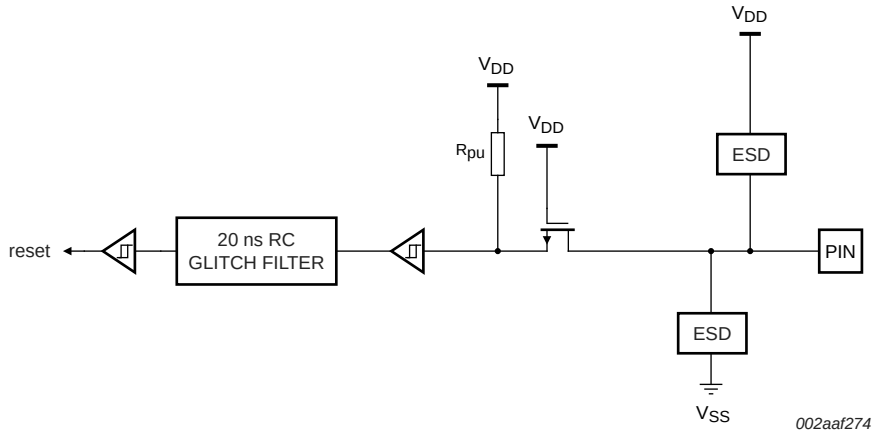
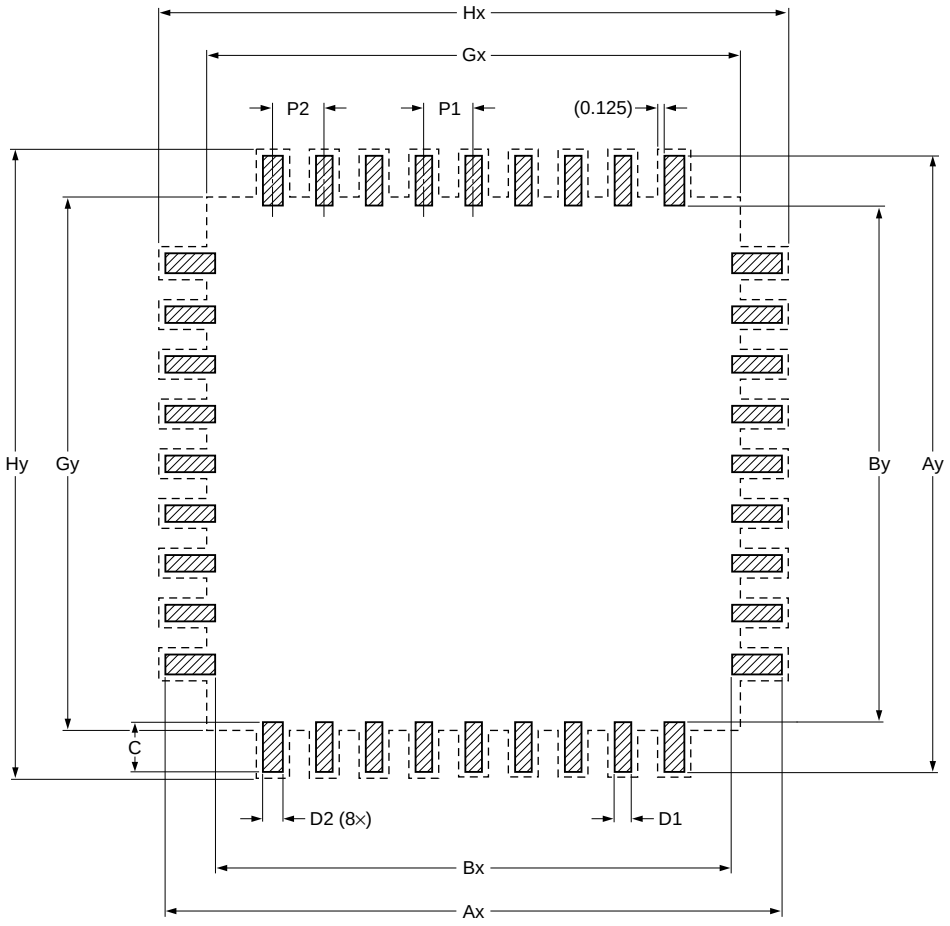


Fig 37. Reset pin configuration

17. Soldering

Footprint information for reflow soldering of LQFP80 package **SOT315-1**



Generic footprint pattern

Refer to the package outline drawing for actual layout

solder land

occupied area

DIMENSIONS in mm

P1	P2	Ax	Ay	Bx	By	C	D1	D2	Gx	Gy	Hx	Hy
0.500	0.560	15.300	15.300	12.300	12.300	1.500	0.280	0.400	12.500	12.500	15.550	15.550

sot315-1_fr

Fig 39. Reflow soldering for the LQFP80 package

Table 26. Revision history *…continued*

Document ID	Release date	Data sheet status	Change notice	Supersedes
LPC1759_58_56_54_52_51 v.8.1	20130912	Product data sheet	-	LPC1759_58_56_54_52_51 v.8
Modifications:	• Added Table 6 “Thermal resistance”. • Table 5 “Limiting values”: – Updated min/max values for $V_{DD(3V3)}$ and $V_{DD(REG)(3V3)}$. – Updated conditions for V_I. – Updated table notes. • Table 7 “Static characteristics”: Added Table note 14 “TCK/SWDCLK pin needs to be externally pulled LOW.” • Updated Section 15.1 “Suggested USB interface solutions”. • Added Section 5 “Marking”. • Changed title of Figure 29 from “USB interface on a self-powered device” to “USB interface with soft-connect”.			
LPC1759_58_56_54_52_51 v.8	20120809	Product data sheet	-	LPC1759_58_56_54_52_51 v.7
Modifications:	• Remove table note “The peak current is limited to 25 times the corresponding maximum current.” from Table 4 “Limiting values”. • Change $V_{DD(3V3)}$ to $V_{DD(REG)(3V3)}$ in Section 11.3 “Internal oscillators”. • Glitch filter constant changed to 10 ns in Table note 5 in Table 3. • Description of $\overline{\text{RESET}}$ function updated in Table 3. • Pull-up value added for GPIO pins in Table 3. • Pin configuration diagram for LQFP80 package corrected (Figure 2). • Pin description of USB_UP_LED pin updated in Table 3. • R_{i1} and R_{i2} labels in Figure 26 updated. • Table note 9 updated in Table 3. • Table note 1 updated in Table 12. • Electromagnetic compatibility data added in Section 14.6. • Section 16 added.			
LPC1759_58_56_54_52_51 v.7	20110329	Product data sheet	-	LPC1759_58_56_54_52_51 v.6
Modifications:	• Pin description of pins P0[29] and P0[30] updated in Table note 4 of Table 3. Pins are not 5 V tolerant. • Typical value for Parameter N_{endu} added in Table 8. • Condition 3.0 V ≤ $V_{DD(3V3)}$ ≤ 3.6 V added in Table 15. • Typical values for parameters $I_{DD(REG)(3V3)}$ and I_{BAT} with condition Deep power-down mode corrected in Table 6 and Table note 9, Table note 10, and Table note 11 updated. • For Deep power-down mode, Figure 8 updated and Figure 9 added.			
LPC1759_58_56_54_52_51 v.6	20100825	Product data sheet	-	LPC1759_58_56_54_52_51 v.5
Modifications:	• Section 7.30.2; BOD level corrected. • Added Section 10.2.			
LPC1759_58_56_54_52_51 v.5	20100716	Product data sheet	-	LPC1759_58_56_54_52_51 v.4
LPC1759_58_56_54_52_51 v.4	20100126	Product data sheet	-	LPC1758_56_54_52_51 v.3
LPC1758_56_54_52_51 v.3	20091119	Product data sheet	-	LPC1758_56_54_52_51 v.2
LPC1758_56_54_52_51 v.2	20090211	Objective data sheet	-	LPC1758_56_54_52_51 v.1
LPC1758_56_54_52_51 v.1	20090115	Objective data sheet	-	-

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