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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Discontinued at Digi-Key
Core Processor	ARM® Cortex®-M3
Core Size	32-Bit Single-Core
Speed	100MHz
Connectivity	CANbus, Ethernet, I²C, IrDA, Microwire, SPI, SSI, UART/USART, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, I²S, Motor Control PWM, POR, PWM, WDT
Number of I/O	52
Program Memory Size	512KB (512K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	64K x 8
Voltage - Supply (Vcc/Vdd)	2.4V ~ 3.6V
Data Converters	A/D 6x12b; D/A 1x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	80-LQFP
Supplier Device Package	80-LQFP (12x12)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/lpc1758fbd80-551

5. Marking

The LPC175x devices typically have the following top-side marking:

LPC175xxxx

xxxxxxx

xxYYWWR[x]

The last/second to last letter in the third line (field ‘R’) will identify the device revision. This data sheet covers the following revisions of the LPC175x:

Table 3. Device revision table

Revision identifier (R)	Revision description
‘-’	Initial device revision
‘A’	Second device revision

Field ‘YY’ states the year the device was manufactured. Field ‘WW’ states the week the device was manufactured during that year.

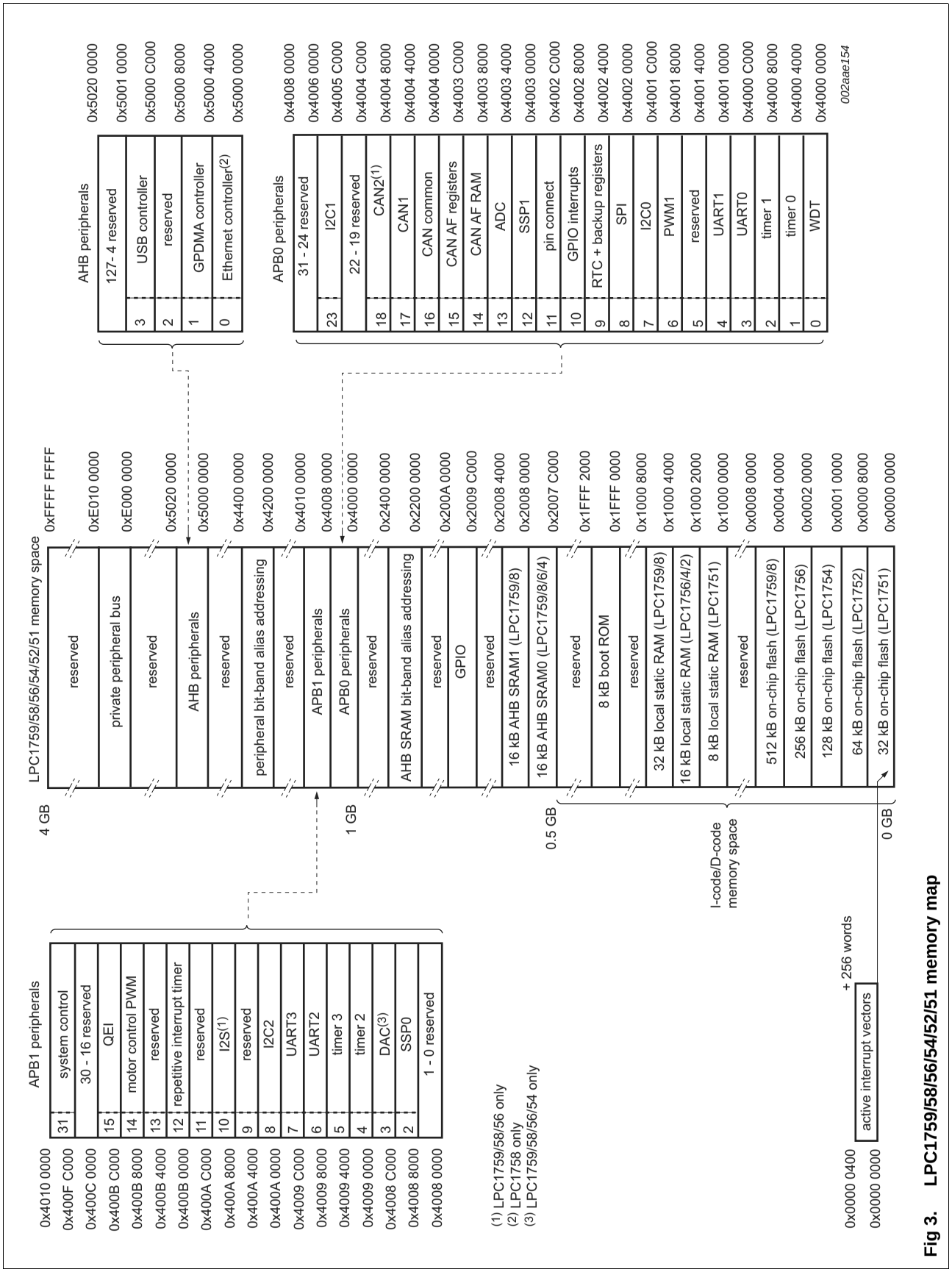


Fig 3. LPC1759/58/56/54/52/51 memory map

8.7 Nested Vectored Interrupt Controller (NVIC)

The NVIC is an integral part of the Cortex-M3. The tight coupling to the CPU allows for low interrupt latency and efficient processing of late arriving interrupts.

8.7.1 Features

- Controls system exceptions and peripheral interrupts
- In the LPC1759/58/56/54/52/51, the NVIC supports 33 vectored interrupts
- 32 programmable interrupt priority levels, with hardware priority level masking
- Relocatable vector table
- Non-Maskable Interrupt (NMI)
- Software interrupt generation

8.7.2 Interrupt sources

Each peripheral device has one interrupt line connected to the NVIC but may have several interrupt flags. Individual interrupt flags may also represent more than one interrupt source.

Any pin on Port 0 and Port 2 (total of 30 pins) regardless of the selected function, can be programmed to generate an interrupt on a rising edge, a falling edge, or both.

8.8 Pin connect block

The pin connect block allows selected pins of the microcontroller to have more than one function. Configuration registers control the multiplexers to allow connection between the pin and the on-chip peripherals.

Peripherals should be connected to the appropriate pins prior to being activated and prior to any related interrupt(s) being enabled. Activity of any enabled peripheral function that is not mapped to a related pin should be considered undefined.

Most pins can also be configured as open-drain outputs or to have a pull-up, pull-down, or no resistor enabled.

8.9 General purpose DMA controller

The GPDMA is an AMBA AHB compliant peripheral allowing selected LPC1759/58/56/54/52/51 peripherals to have DMA support.

The GPDMA enables peripheral-to-memory, memory-to-peripheral, peripheral-to-peripheral, and memory-to-memory transactions. The source and destination areas can each be either a memory region or a peripheral, and can be accessed through the AHB master. The GPDMA controller allows data transfers between the USB and Ethernet (LPC1758 only) controllers and the various on-chip SRAM areas. The supported APB peripherals are SSP0/1, all UARTs, the I^2S-bus interface, the ADC, and the DAC. Two match signals for each timer can be used to trigger DMA transfers.

Remark: Note that the DAC is not available on the LPC1752/51, and the I^2S-bus interface is not available on the LPC1754/52/51.

Additionally, any pin on Port 0 and Port 2 (total of 42 pins) providing a digital function can be programmed to generate an interrupt on a rising edge, a falling edge, or both. The edge detection is asynchronous, so it may operate when clocks are not present such as during Power-down mode. Each enabled interrupt can be used to wake up the chip from Power-down mode.

8.10.1 Features

- Bit level set and clear registers allow a single instruction to set or clear any number of bits in one port.
- Direction control of individual bits.
- All I/O default to inputs after reset.
- Pull-up/pull-down resistor configuration and open-drain configuration can be programmed through the pin connect block for each GPIO pin.

8.11 Ethernet (LPC1758 only)

The Ethernet block contains a full featured 10 Mbit/s or 100 Mbit/s Ethernet MAC designed to provide optimized performance through the use of DMA hardware acceleration. Features include a generous suite of control registers, half or full duplex operation, flow control, control frames, hardware acceleration for transmit retry, receive packet filtering and wake-up on LAN activity. Automatic frame transmission and reception with scatter-gather DMA off-loads many operations from the CPU.

The Ethernet block and the CPU share the ARM Cortex-M3 D-code and system bus through the AHB-multilayer matrix to access the various on-chip SRAM blocks for Ethernet data, control, and status information.

The Ethernet block interfaces between an off-chip Ethernet PHY using the Reduced MII (RMII) protocol and the on-chip Media Independent Interface Management (MIIM) serial bus.

The Ethernet block supports bus clock rates of up to 100 MHz.

8.11.1 Features

- Ethernet standards support:
  - Supports 10 Mbit/s or 100 Mbit/s PHY devices including 10 Base-T, 100 Base-TX, 100 Base-FX, and 100 Base-T4.
  - Fully compliant with *IEEE standard 802.3*.
  - Fully compliant with 802.3x full duplex flow control and half duplex back pressure.
  - Flexible transmit and receive frame options.
  - Virtual Local Area Network (VLAN) frame support.
- Memory management:
  - Independent transmit and receive buffers memory mapped to shared SRAM.
  - DMA managers with scatter/gather DMA and arrays of frame descriptors.
  - Memory traffic optimized by buffering and pre-fetching.
- Enhanced Ethernet features:

8.16 UARTs

The LPC1759/58/56/54/52/51 each contain four UARTs. In addition to standard transmit and receive data lines, UART1 also provides a full modem control handshake interface and support for RS-485/9-bit mode allowing both software address detection and automatic address detection using 9-bit mode.

The UARTs include a fractional baud rate generator. Standard baud rates such as 115200 Bd can be achieved with any crystal frequency above 2 MHz.

8.16.1 Features

- Maximum UART data bit rate of 6.25 Mbit/s.
- 16 B Receive and Transmit FIFOs.
- Register locations conform to 16C550 industry standard.
- Receiver FIFO trigger points at 1 B, 4 B, 8 B, and 14 B.
- Built-in fractional baud rate generator covering wide range of baud rates without a need for external crystals of particular values.
- Fractional divider for baud rate control, auto baud capabilities and FIFO control mechanism that enables software flow control implementation.
- UART1 equipped with standard modem interface signals. This module also provides full support for hardware flow control (auto-CTS/RTS).
- Support for RS-485/9-bit/EIA-485 mode (UART1).
- UART3 includes an IrDA mode to support infrared communication.
- All UARTs have DMA support.

8.17 SPI serial I/O controller

The LPC1759/58/56/54/52/51 contain one SPI controller. SPI is a full duplex serial interface designed to handle multiple masters and slaves connected to a given bus. Only a single master and a single slave can communicate on the interface during a given data transfer. During a data transfer the master always sends 8 bits to 16 bits of data to the slave, and the slave always sends 8 bits to 16 bits of data to the master.

8.17.1 Features

- Maximum SPI data bit rate of 12.5 Mbit/s
- Compliant with SPI specification
- Synchronous, serial, full duplex communication
- Combined SPI master and slave
- Maximum data bit rate of one eighth of the input clock rate
- 8 bits to 16 bits per transfer

8.18 SSP serial I/O controller

The LPC1759/58/56/54/52/51 contain two SSP controllers. The SSP controller is capable of operation on a SPI, 4-wire SSI, or Microwire bus. It can interact with multiple masters and slaves on the bus. Only a single master and a single slave can communicate on the

bus during a given data transfer. The SSP supports full duplex transfers, with frames of 4 bits to 16 bits of data flowing from the master to the slave and from the slave to the master. In practice, often only one of these data flows carries meaningful data.

8.18.1 Features

- Maximum SSP speed of 33 Mbit/s (master) or 8 Mbit/s (slave)
- Compatible with Motorola SPI, 4-wire Texas Instruments SSI, and National Semiconductor Microwire buses
- Synchronous serial communication
- Master or slave operation
- 8-frame FIFOs for both transmit and receive
- 4-bit to 16-bit frame
- DMA transfers supported by GPDMA

8.19 I^2C-bus serial I/O controllers

The LPC1759/58/56/54/52/51 each contain two I^2C-bus controllers.

The I^2C-bus is bidirectional for inter-IC control using only two wires: a Serial Clock Line (SCL) and a Serial DAta line (SDA). Each device is recognized by a unique address and can operate as either a receiver-only device (e.g., an LCD driver) or a transmitter with the capability to both receive and send information (such as memory). Transmitters and/or receivers can operate in either master or slave mode, depending on whether the chip has to initiate a data transfer or is only addressed. The I^2C is a multi-master bus and can be controlled by more than one bus master connected to it.

8.19.1 Features

- I^2C1 and I^2C2 use standard I/O pins with bit rates of up to 400 kbit/s (Fast I^2C-bus).
- Easy to configure as master, slave, or master/slave.
- Programmable clocks allow versatile rate control.
- Bidirectional data transfer between masters and slaves.
- Multi-master bus (no central master).
- Arbitration between simultaneously transmitting masters without corruption of serial data on the bus.
- Serial clock synchronization allows devices with different bit rates to communicate via one serial bus.
- Serial clock synchronization can be used as a handshake mechanism to suspend and resume serial transfer.
- The I^2C-bus can be used for test and diagnostic purposes.
- Both I^2C-bus controllers support multiple address recognition and a bus monitor mode.

8.20 I^2S-bus serial I/O controllers (LPC1759/58/56 only)

The I^2S-bus provides a standard communication interface for digital audio applications.

- Pulse period and width can be any number of timer counts. This allows complete flexibility in the trade-off between resolution and repetition rate. All PWM outputs will occur at the same repetition rate.
- Double edge controlled PWM outputs can be programmed to be either positive going or negative going pulses.
- Match register updates are synchronized with pulse outputs to prevent generation of erroneous pulses. Software must ‘release’ new match values before they can become effective.
- May be used as a standard 32-bit timer/counter with a programmable 32-bit prescaler if the PWM mode is not enabled.

8.23 Motor control PWM

The motor control PWM is a specialized PWM supporting 3-phase motors and other combinations. Feedback inputs are provided to automatically sense rotor position and use that information to ramp speed up or down. At the same time, the motor control PWM is highly configurable for other generalized timing, counting, capture, and compare applications.

8.24 Quadrature Encoder Interface (QEI)

A quadrature encoder, also known as a 2-channel incremental encoder, converts angular displacement into two pulse signals. By monitoring both the number of pulses and the relative phase of the two signals, the user can track the position, direction of rotation, and velocity. In addition, a third channel, or index signal, can be used to reset the position counter. The quadrature encoder interface decodes the digital pulses from a quadrature encoder wheel to integrate position over time and determine direction of rotation. In addition, the QEI can capture the velocity of the encoder wheel.

8.24.1 Features

- Tracks encoder position.
- Increments/decrements depending on direction.
- Programmable for 2× or 4× position counting.
- Velocity capture using built-in timer.
- Velocity compare function with “less than” interrupt.
- Uses 32-bit registers for position and velocity.
- Three position compare registers with interrupts.
- Index counter for revolution counting.
- Index compare register with interrupts.
- Can combine index and position interrupts to produce an interrupt for whole and partial revolution displacement.
- Digital filter with programmable delays for encoder input signals.
- Can accept decoded signal inputs (clk and direction).
- Connected to APB.

8.25 Repetitive Interrupt (RI) timer

The repetitive interrupt timer provides a free-running 32-bit counter which is compared to a selectable value, generating an interrupt when a match occurs. Any bits of the timer/compare can be masked such that they do not contribute to the match detection. The repetitive interrupt timer can be used to create an interrupt that repeats at predetermined intervals.

8.25.1 Features

- 32-bit counter running from PCLK. Counter can be free-running or be reset by a generated interrupt.
- 32-bit compare value.
- 32-bit compare mask. An interrupt is generated when the counter value equals the compare value, after masking. This allows for combinations not possible with a simple compare.

8.26 ARM Cortex-M3 system tick timer

The ARM Cortex-M3 includes a system tick timer (SYSTICK) that is intended to generate a dedicated SYSTICK exception at a 10 ms interval. In the LPC1759/58/56/54/52/51, this timer can be clocked from the internal AHB clock or from a device pin.

8.27 Watchdog timer

The purpose of the watchdog is to reset the microcontroller within a reasonable amount of time if it enters an erroneous state. When enabled, the watchdog will generate a system reset if the user program fails to ‘feed’ (or reload) the watchdog within a predetermined amount of time.

8.27.1 Features

- Internally resets chip if not periodically reloaded.
- Debug mode.
- Enabled by software but requires a hardware reset or a watchdog reset/interrupt to be disabled.
- Incorrect/Incomplete feed sequence causes reset/interrupt if enabled.
- Flag to indicate watchdog reset.
- Programmable 32-bit timer with internal prescaler.
- Selectable time period from ($T_{cy(WDCLK)} \times 256 \times 4$) to ($T_{cy(WDCLK)} \times 2^{32} \times 4$) in multiples of $T_{cy(WDCLK)} \times 4$.
- The Watchdog Clock (WDCLK) source can be selected from the Internal RC (IRC) oscillator, the RTC oscillator, or the APB peripheral clock. This gives a wide range of potential timing choices of Watchdog operation under different power reduction conditions. It also provides the ability to run the WDT from an entirely internal source that is not dependent on an external crystal and its associated components and wiring for increased reliability.
- Includes lock/safe feature.

Table 7. Static characteristics *…continued*
T_{amb} = −40 °C to +85 °C, unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ[1]	Max	Unit
Oscillator pins							
$V_{i(XTAL1)}$	input voltage on pin XTAL1			−0.5	1.8	1.95	V
$V_{o(XTAL2)}$	output voltage on pin XTAL2			−0.5	1.8	1.95	V
$V_{i(RTCX1)}$	input voltage on pin RTCX1			−0.5	-	3.6	V
$V_{o(RTCX2)}$	output voltage on pin RTCX2			−0.5	-	3.6	V
USB pins							
I_{OZ}	OFF-state output current	0 V < V_I < 3.3 V	[2]	-	-	±10	μA
V_{BUS}	bus supply voltage		[2]	-	-	5.25	V
V_{DI}	differential input sensitivity voltage	|(D+) − (D−)|	[2]	0.2	-	-	V
V_{CM}	differential common mode voltage range	includes V_{DI} range	[2]	0.8	-	2.5	V
$V_{th(rs)se}$	single-ended receiver switching threshold voltage		[2]	0.8	-	2.0	V
V_{OL}	LOW-level output voltage for low-/full-speed	R_L of 1.5 kΩ to 3.6 V	[2]	-	-	0.18	V
V_{OH}	HIGH-level output voltage (driven) for low-/full-speed	R_L of 15 kΩ to GND	[2]	2.8	-	3.5	V
C_{trans}	transceiver capacitance	pin to GND	[2]	-	-	20	pF
Z_{DRV}	driver output impedance for driver which is not high-speed capable	with 33 Ω series resistor; steady state drive	[2][24]	36	-	44.1	Ω

[1] Typical ratings are not guaranteed. The values listed are at room temperature (25 °C), nominal supply voltages.

[2] For USB operation 3.0 V ≤ $V_{DD((3V3)}$ ≤ 3.6 V. Guaranteed by design.

[3] V_{DDA} and VREFP should be tied to $V_{DD(3V3)}$ if the ADC and DAC are not used.

[4] V_{DDA} for DAC specs are from 2.7 V to 3.6 V.

[5] The RTC typically fails when $V_{i(VBAT)}$ drops below 1.6 V.

[6] $V_{DD(REG)(3V3)}$ = 3.3 V; T_{amb} = 25 °C for all power consumption measurements.

[7] Applies to LPC1758, LPC1756, LPC1754, LPC1752, LPC1751.

[8] Applies to LPC1759 only.

[9] IRC running at 4 MHz; main oscillator and PLL disabled; PCLK = $^{CCLK}/_{8}$.

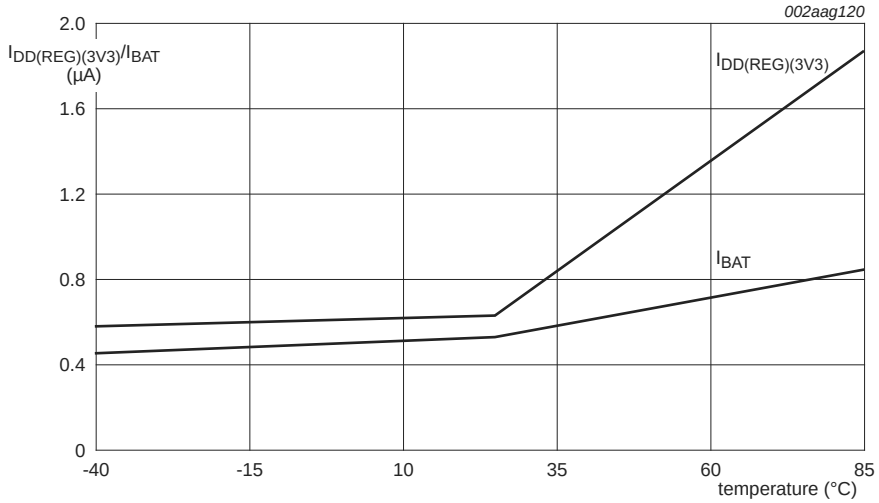
[10] BOD disabled.

[11] On pin $V_{DD(REG)(3V3)}$. I_{BAT} = 530 nA. $V_{DD(REG)(3V3)}$ = 3.0 V; V_{BAT} = 3.0 V; T_{amb} = 25 °C.

[12] On pin VBAT. $I_{DD(REG)(3V3)}$ = 630 nA. $V_{DD(REG)(3V3)}$ = 3.0 V; V_{BAT} = 3.0 V. T_{amb} = 25 °C.

[13] On pin VBAT. V_{BAT} = 3.0 V. T_{amb} = 25 °C.

[14] All internal pull-ups disabled. All pins configured as output and driven LOW. $V_{DD(3V3)}$ = 3.3 V; T_{amb} = 25 °C.



Conditions: V_{BAT} = 3.0 V; $V_{DD(REG)(3V3)}$ = 3.0 V; RTC running.

Fig 9. Deep power-down mode: Typical regulator supply current $I_{DD(REG)(3V3)}$ and battery supply current I_{BAT} versus temperature

12.5 I²C-bus

Table 13. Dynamic characteristic: I²C-bus pins[1]
T_{amb} = −40 °C to +85 °C.[2]

Symbol	Parameter		Conditions	Min	Max	Unit
f_{SCL}	SCL clock frequency		Standard-mode	0	100	kHz
			Fast-mode	0	400	kHz
t_f	fall time	[3][4][5][6]	of both SDA and SCL signals Standard-mode	-	300	ns
			Fast-mode	$20 + 0.1 \times C_b$	300	ns
t_{LOW}	LOW period of the SCL clock		Standard-mode	4.7	-	µs
			Fast-mode	1.3	-	µs
t_{HIGH}	HIGH period of the SCL clock		Standard-mode	4.0	-	µs
			Fast-mode	0.6	-	µs
$t_{HD;DAT}$	data hold time	[3][7][8]	Standard-mode	0	-	µs
			Fast-mode	0	-	µs
$t_{SU;DAT}$	data set-up time	[9]	Standard-mode	250	-	ns
			Fast-mode	100	-	ns

[1] See the I²C-bus specification *UM10204* for details.

[2] Parameters are valid over operating temperature range unless otherwise specified.

[3] A device must internally provide a hold time of at least 300 ns for the SDA signal (with respect to the V_{IH}(min) of the SCL signal) to bridge the undefined region of the falling edge of SCL.

[4] C_b = total capacitance of one bus line in pF.

[5] The maximum t_f for the SDA and SCL bus lines is specified at 300 ns. The maximum fall time for the SDA output stage t_f is specified at 250 ns. This allows series protection resistors to be connected in between the SDA and the SCL pins and the SDA/SCL bus lines without exceeding the maximum specified t_f.

[6] In Fast-mode Plus, fall time is specified the same for both output stage and bus timing. If series resistors are used, designers should allow for this when considering bus timing.

[7] tHD;DAT is the data hold time that is measured from the falling edge of SCL; applies to data in transmission and the acknowledge.

[8] The maximum $t_{HD;DAT}$ could be 3.45 µs and 0.9 µs for Standard-mode and Fast-mode but must be less than the maximum of $t_{VD;DAT}$ or $t_{VD;ACK}$ by a transition time (see the I²C-bus specification *UM10204*). This maximum must only be met if the device does not stretch the LOW period (t_{LOW}) of the SCL signal. If the clock stretches the SCL, the data must be valid by the set-up time before it releases the clock.

[9] tSU;DAT is the data set-up time that is measured with respect to the rising edge of SCL; applies to data in transmission and the acknowledge.

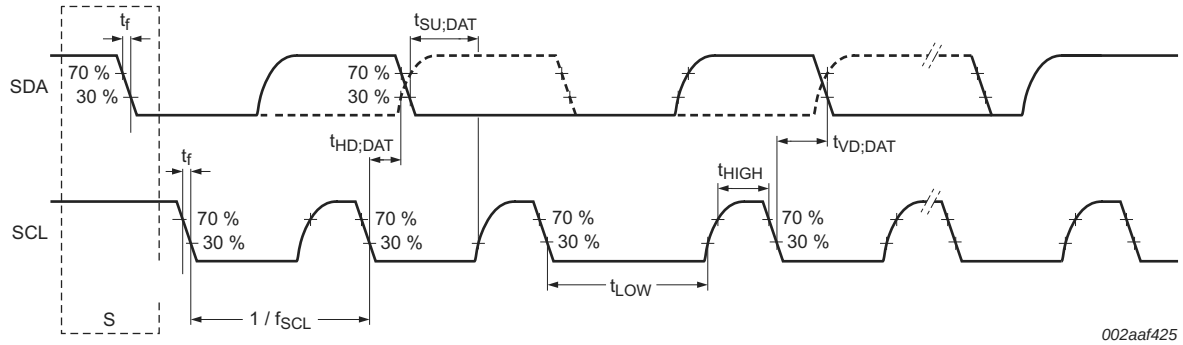


Fig 16. I²C-bus pins clock timing

12.7 SSP interface

The maximum SSP speed is 33 Mbit/s in master mode or 8 Mbit/s in slave mode. In slave mode, the maximum SSP clock rate must be 1/12 of the SSP PCLK clock rate.

Table 15. Dynamic characteristics: SSP pins in SPI mode

C_L = 30 pF on all SSP pins; T_{amb} = −40 °C to 85 °C; $V_{DD(3V3)}$ = 3.3 V to 3.6 V; input slew = 1 ns; sampled at 10 % and 90 % of the signal level. Values guaranteed by design.

Symbol	Parameter	Conditions	Min	Max	Unit
SSP master					
t_{DS}	data set-up time	in SPI mode	16.1	-	ns
t_{DH}	data hold time	in SPI mode	0	-	ns
$t_{v(Q)}$	data output valid time	in SPI mode	-	2.5	ns
$t_{h(Q)}$	data output hold time	in SPI mode	0	-	ns
SSP slave					
t_{DS}	data set-up time	in SPI mode	16.1	-	ns
t_{DH}	data hold time	in SPI mode	0	-	ns
$t_{v(Q)}$	data output valid time	in SPI mode	-	$3*T_{cy(PCLK)} + 2.5$	ns
$t_{h(Q)}$	data output hold time	in SPI mode	0	-	ns

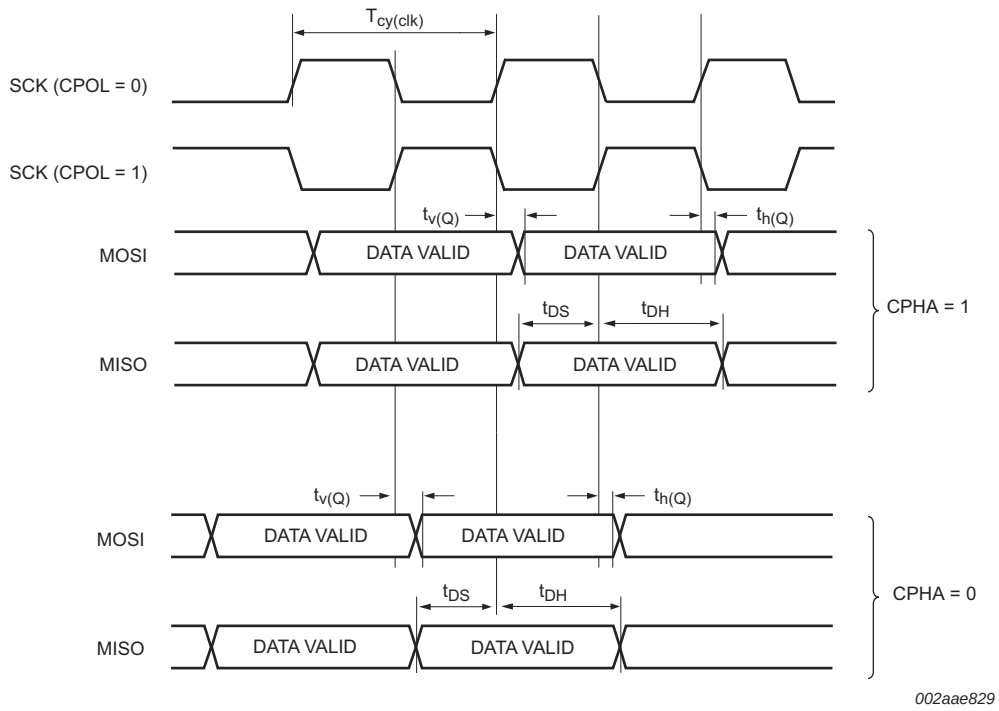


Fig 19. SSP master timing in SPI mode

12.9 SPI

Table 17. Dynamic characteristics of SPI pins
T_{amb} = −40 °C to +85 °C.

Symbol	Parameter		Min	Typ	Max	Unit
$T_{cy(PCLK)}$	PCLK cycle time		10	-	-	ns
T_{SPICYC}	SPI cycle time	[1]	79.6	-	-	ns
$t_{SPICLKH}$	SPICLK HIGH time		0.485 × T_{SPICYC}	-	-	ns
$t_{SPICLKL}$	SPICLK LOW time			-	0.515 × T_{SPICYC}	ns
SPI master						
t_{SPIDSU}	SPI data set-up time	[2]	0	-	-	ns
t_{SPIDH}	SPI data hold time	[2]	2 × $T_{cy(PCLK)}$ − 5	-	-	ns
t_{SPIQV}	SPI data output valid time	[2]	2 × $T_{cy(PCLK)}$ + 30	-	-	ns
t_{SPIOH}	SPI output data hold time	[2]	2 × $T_{cy(PCLK)}$ + 5	-	-	ns
SPI slave						
t_{SPIDSU}	SPI data set-up time	[2]	0	-	-	ns
t_{SPIDH}	SPI data hold time	[2]	2 × $T_{cy(PCLK)}$ + 5	-	-	ns
t_{SPIQV}	SPI data output valid time	[2]	2 × $T_{cy(PCLK)}$ + 35	-	-	ns
t_{SPIOH}	SPI output data hold time	[2]	2 × $T_{cy(PCLK)}$ + 15	-	-	ns

[1] $T_{SPICYC} = (T_{cy(PCLK)} \times n) \pm 0.5$ %, n is the SPI clock divider value ($n \geq 8$); PCLK is derived from the processor clock CCLK.

[2] Timing parameters are measured with respect to the 50 % edge of the clock PCLK and the 10 % (90 %) edge of the data signal (MOSI or MISO).

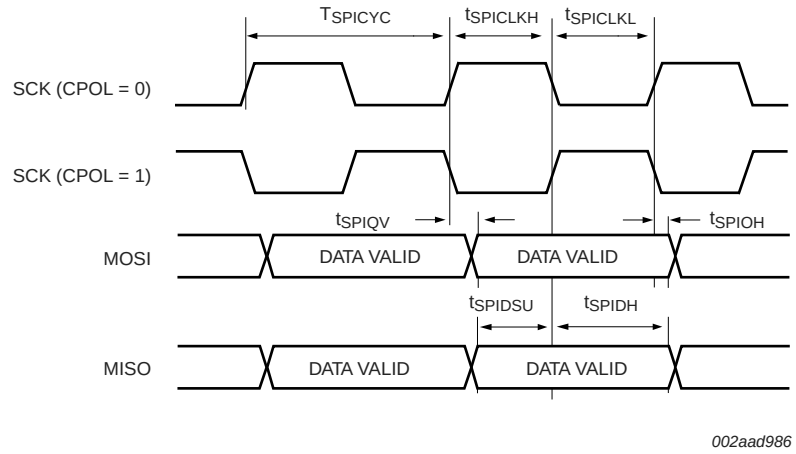


Fig 22. SPI master timing (CPHA = 1)

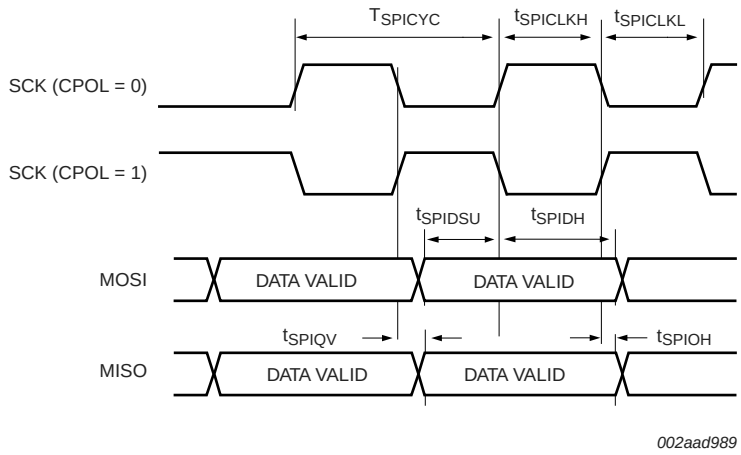


Fig 25. SPI slave timing (CPHA = 0)

13. ADC electrical characteristics

Table 18. ADC characteristics (full resolution)

V_{DDA} = 2.5 V to 3.6 V; T_{amb} = −40 °C to +85 °C unless otherwise specified; ADC frequency 13 MHz; 12-bit resolution.[1]

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{IA}	analog input voltage			0	-	V_{DDA}	V
C_{ia}	analog input capacitance			-	-	15	pF
E_D	differential linearity error		[2][3]	-	-	±1	LSB
$E_{L(adj)}$	integral non-linearity		[4]	-	-	±3	LSB
E_O	offset error		[5][6]	-	-	±2	LSB
E_G	gain error		[7]	-	-	0.5	%
E_T	absolute error		[8]	-	-	4	LSB
R_{vsi}	voltage source interface resistance		[9]	-	-	7.5	kΩ
$f_{clk(ADC)}$	ADC clock frequency			-	-	13	MHz
$f_{c(ADC)}$	ADC conversion frequency		[10]	-	-	200	kHz

[1] V_{DDA} and VREFP should be tied to $V_{DD(3V3)}$ if the ADC and DAC are not used.

[2] The ADC is monotonic, there are no missing codes.

[3] The differential linearity error (E_D) is the difference between the actual step width and the ideal step width. See Figure 26.

[4] The integral non-linearity ($E_{L(adj)}$) is the peak difference between the center of the steps of the actual and the ideal transfer curve after appropriate adjustment of gain and offset errors. See Figure 26.

[5] The offset error (E_O) is the absolute difference between the straight line which fits the actual curve and the straight line which fits the ideal curve. See Figure 26.

[6] ADCOFFS value (bits 7:4) = 2 in the ADTRM register. See LPC17xx user manual UM10360.

[7] The gain error (E_G) is the relative difference in percent between the straight line fitting the actual transfer curve after removing offset error, and the straight line which fits the ideal transfer curve. See Figure 26.

[8] The absolute error (E_T) is the maximum difference between the center of the steps of the actual transfer curve of the non-calibrated ADC and the ideal transfer curve. See Figure 26.

[9] See Figure 27.

[10] The conversion frequency corresponds to the number of samples per second.

15. Application information

15.1 Suggested USB interface solutions

If the LPC1759/58/56/54/52/51 V_{DD} is always greater than 0 V while V_{BUS} = 5 V, the V_{BUS} pin can be connected directly to the V_{BUS} pin on the USB connector.

This applies to bus powered devices where the USB cable supplies the system power. For systems where V_{DD} can be 0 V and V_{BUS} is directly applied to the V_{BUS} pin, precautions must be taken to reduce the voltage to below 3.6 V.

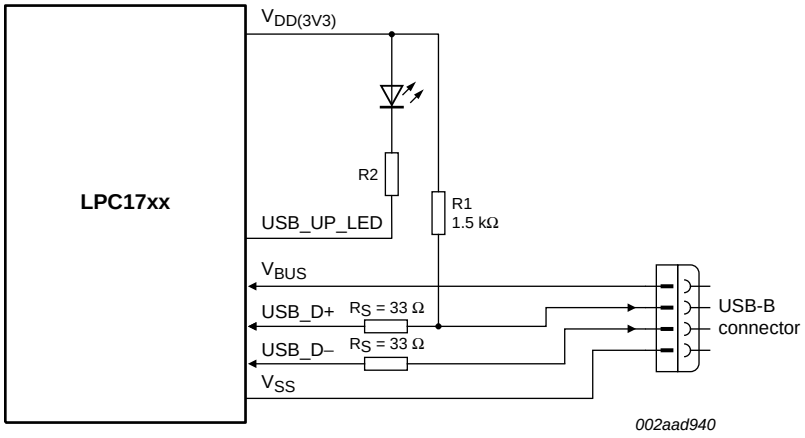


Fig 28. LPC1759/58/56/54/52/51 USB interface on a bus-powered device

The maximum allowable voltage on the V_{BUS} pin is 3.6 V. One method is to use a voltage divider to connect the V_{BUS} pin to the V_{BUS} on the USB connector.

The voltage divider ratio should be such that the V_{BUS} pin will be greater than $0.7V_{DD}$ to indicate a logic HIGH while below the 3.6 V allowable maximum voltage.

Use the following operating conditions:

$VBUS_{max}$ = 5.25 V

V_{DD} = 3.6 V

The voltage divider would need to provide a reduction of 3.6 V/5.25 V or ~0.686 V.

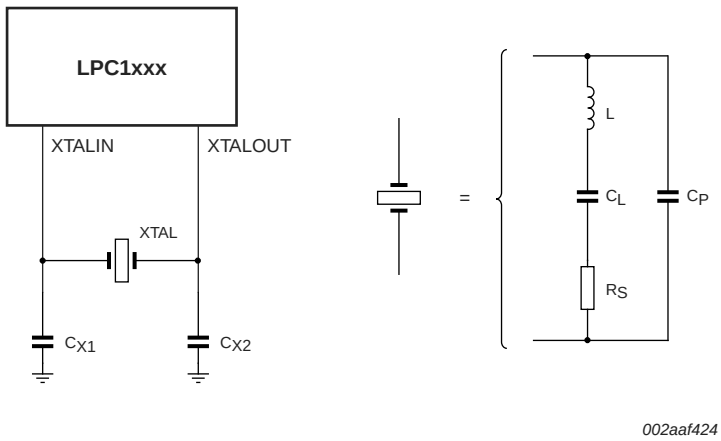


Fig 35. Oscillator modes and models: oscillation mode of operation and external crystal model used for C_{X1}/C_{X2} evaluation

Table 22. Recommended values for C_{X1}/C_{X2} in oscillation mode (crystal and external components parameters): low frequency mode

Fundamental oscillation frequency F_{OSC}	Crystal load capacitance C_L	Maximum crystal series resistance R_S	External load capacitors C_{X1}/C_{X2}
1 MHz to 5 MHz	10 pF	< 300 Ω	18 pF, 18 pF
	20 pF	< 300 Ω	39 pF, 39 pF
	30 pF	< 300 Ω	57 pF, 57 pF
5 MHz to 10 MHz	10 pF	< 300 Ω	18 pF, 18 pF
	20 pF	< 200 Ω	39 pF, 39 pF
	30 pF	< 100 Ω	57 pF, 57 pF
10 MHz to 15 MHz	10 pF	< 160 Ω	18 pF, 18 pF
	20 pF	< 60 Ω	39 pF, 39 pF
15 MHz to 20 MHz	10 pF	< 80 Ω	18 pF, 18 pF

Table 23. Recommended values for C_{X1}/C_{X2} in oscillation mode (crystal and external components parameters): high frequency mode

Fundamental oscillation frequency F_{OSC}	Crystal load capacitance C_L	Maximum crystal series resistance R_S	External load capacitors C_{X1}, C_{X2}
15 MHz to 20 MHz	10 pF	< 180 Ω	18 pF, 18 pF
	20 pF	< 100 Ω	39 pF, 39 pF
20 MHz to 25 MHz	10 pF	< 160 Ω	18 pF, 18 pF
	20 pF	< 80 Ω	39 pF, 39 pF

15.3 XTAL Printed-Circuit Board (PCB) layout guidelines

The crystal should be connected on the PCB as close as possible to the oscillator input and output pins of the chip. Take care that the load capacitors C_{x1}, C_{x2}, and C_{x3} in case of third overtone crystal usage have a common ground plane. The external components must also be connected to the ground plain. Loops must be made as small as possible in

18. Abbreviations

Table 25. Abbreviations

Acronym	Description
ADC	Analog-to-Digital Converter
AHB	Advanced High-performance Bus
AMBA	Advanced Microcontroller Bus Architecture
APB	Advanced Peripheral Bus
BOD	BrownOut Detection
CAN	Controller Area Network
DAC	Digital-to-Analog Converter
DMA	Direct Memory Access
EOP	End Of Packet
GPIO	General Purpose Input/Output
IRC	Internal RC
IrDA	Infrared Data Association
JTAG	Joint Test Action Group
MAC	Media Access Control
MIIM	Media Independent Interface Management
OTG	On-The-Go
PHY	Physical Layer
PLL	Phase-Locked Loop
PWM	Pulse Width Modulator
RMII	Reduced Media Independent Interface
SE0	Single Ended Zero
SPI	Serial Peripheral Interface
SSI	Serial Synchronous Interface
SSP	Synchronous Serial Port
TTL	Transistor-Transistor Logic
UART	Universal Asynchronous Receiver/Transmitter
USB	Universal Serial Bus

19. References

[1] LPC176x/5x User manual UM10360:
http://www.nxp.com/documents/user_manual/UM10360.pdf

[2] LPC175x Errata sheet:
http://www.nxp.com/documents/errata_sheet/ES_LPC175X.pdf

[3] Technical note ADC design guidelines:
http://www.nxp.com/documents/technical_note/TN00009.pdf

Table 26. Revision history *…continued*

Document ID	Release date	Data sheet status	Change notice	Supersedes
LPC1759_58_56_54_52_51 v.8.1	20130912	Product data sheet	-	LPC1759_58_56_54_52_51 v.8
Modifications:	• Added Table 6 “Thermal resistance”. • Table 5 “Limiting values”: – Updated min/max values for $V_{DD(3V3)}$ and $V_{DD(REG)(3V3)}$. – Updated conditions for V_I. – Updated table notes. • Table 7 “Static characteristics”: Added Table note 14 “TCK/SWDCLK pin needs to be externally pulled LOW.” • Updated Section 15.1 “Suggested USB interface solutions”. • Added Section 5 “Marking”. • Changed title of Figure 29 from “USB interface on a self-powered device” to “USB interface with soft-connect”.			
LPC1759_58_56_54_52_51 v.8	20120809	Product data sheet	-	LPC1759_58_56_54_52_51 v.7
Modifications:	• Remove table note “The peak current is limited to 25 times the corresponding maximum current.” from Table 4 “Limiting values”. • Change $V_{DD(3V3)}$ to $V_{DD(REG)(3V3)}$ in Section 11.3 “Internal oscillators”. • Glitch filter constant changed to 10 ns in Table note 5 in Table 3. • Description of $\overline{\text{RESET}}$ function updated in Table 3. • Pull-up value added for GPIO pins in Table 3. • Pin configuration diagram for LQFP80 package corrected (Figure 2). • Pin description of USB_UP_LED pin updated in Table 3. • R_{i1} and R_{i2} labels in Figure 26 updated. • Table note 9 updated in Table 3. • Table note 1 updated in Table 12. • Electromagnetic compatibility data added in Section 14.6. • Section 16 added.			
LPC1759_58_56_54_52_51 v.7	20110329	Product data sheet	-	LPC1759_58_56_54_52_51 v.6
Modifications:	• Pin description of pins P0[29] and P0[30] updated in Table note 4 of Table 3. Pins are not 5 V tolerant. • Typical value for Parameter N_{endu} added in Table 8. • Condition 3.0 V ≤ $V_{DD(3V3)}$ ≤ 3.6 V added in Table 15. • Typical values for parameters $I_{DD(REG)(3V3)}$ and I_{BAT} with condition Deep power-down mode corrected in Table 6 and Table note 9, Table note 10, and Table note 11 updated. • For Deep power-down mode, Figure 8 updated and Figure 9 added.			
LPC1759_58_56_54_52_51 v.6	20100825	Product data sheet	-	LPC1759_58_56_54_52_51 v.5
Modifications:	• Section 7.30.2; BOD level corrected. • Added Section 10.2.			
LPC1759_58_56_54_52_51 v.5	20100716	Product data sheet	-	LPC1759_58_56_54_52_51 v.4
LPC1759_58_56_54_52_51 v.4	20100126	Product data sheet	-	LPC1758_56_54_52_51 v.3
LPC1758_56_54_52_51 v.3	20091119	Product data sheet	-	LPC1758_56_54_52_51 v.2
LPC1758_56_54_52_51 v.2	20090211	Objective data sheet	-	LPC1758_56_54_52_51 v.1
LPC1758_56_54_52_51 v.1	20090115	Objective data sheet	-	-

21. Legal information

21.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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