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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M3
Core Size	32-Bit Single-Core
Speed	100MHz
Connectivity	CANbus, Ethernet, I²C, IrDA, Microwire, SPI, SSI, UART/USART, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, I²S, Motor Control PWM, POR, PWM, WDT
Number of I/O	52
Program Memory Size	512KB (512K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	64K x 8
Voltage - Supply (Vcc/Vdd)	2.4V ~ 3.6V
Data Converters	A/D 6x12b; D/A 1x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	80-LQFP
Supplier Device Package	80-LQFP (12x12)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/lpc1758fbd80y

- ◆ WatchDog Timer (WDT). The WDT can be clocked from the internal RC oscillator, the RTC oscillator, or the APB clock.
- ◆ ARM Cortex-M3 system tick timer, including an external clock input option.
- ◆ Repetitive Interrupt Timer (RIT) provides programmable and repeating timed interrupts.
- ◆ Each peripheral has its own clock divider for further power savings.

- Standard JTAG debug interface for compatibility with existing tools. Serial Wire Debug and Serial Wire Trace Port options. Boundary scan Description Language (BSDL) is not available for this device.
- Emulation trace module enables non-intrusive, high-speed real-time tracing of instruction execution.
- Integrated PMU (Power Management Unit) automatically adjusts internal regulators to minimize power consumption during Sleep, Deep sleep, Power-down, and Deep power-down modes.
- Four reduced power modes: Sleep, Deep-sleep, Power-down, and Deep power-down.
- Single 3.3 V power supply (2.4 V to 3.6 V).
- One external interrupt input configurable as edge/level sensitive. All pins on Port 0 and Port 2 can be used as edge sensitive interrupt sources.
- Non-maskable Interrupt (NMI) input.
- The Wakeup Interrupt Controller (WIC) allows the CPU to automatically wake up from any priority interrupt that can occur while the clocks are stopped in Deep sleep, Power-down, and Deep power-down modes.
- Processor wake-up from Power-down mode via any interrupt able to operate during Power-down mode (includes external interrupts, RTC interrupt, USB activity, Ethernet wake-up interrupt (LPC1758 only), CAN bus activity, Port 0/2 pin interrupt, and NMI).
- Brownout detect with separate threshold for interrupt and forced reset.
- Power-On Reset (POR).
- Crystal oscillator with an operating range of 1 MHz to 25 MHz.
- 4 MHz internal RC oscillator trimmed to 1 % accuracy that can optionally be used as a system clock.
- PLL allows CPU operation up to the maximum CPU rate without the need for a high-frequency crystal. May be run from the main oscillator, the internal RC oscillator, or the RTC oscillator.
- USB PLL for added flexibility.
- Code Read Protection (CRP) with different security levels.
- Unique device serial number for identification purposes.
- Available as 80-pin LQFP package (12 mm × 12 mm × 1.4 mm).

3. Applications

- eMetering
- Lighting
- Industrial networking
- Alarm systems
- White goods
- Motor control

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5. Marking

The LPC175x devices typically have the following top-side marking:

LPC175xxxx

xxxxxxx

xxYYWWR[x]

The last/second to last letter in the third line (field ‘R’) will identify the device revision. This data sheet covers the following revisions of the LPC175x:

Table 3. Device revision table

Revision identifier (R)	Revision description
‘-’	Initial device revision
‘A’	Second device revision

Field ‘YY’ states the year the device was manufactured. Field ‘WW’ states the week the device was manufactured during that year.

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Table 4. Pin description *…continued*

Symbol	Pin	Type	Description
P1[18]/ USB_UP_LED/ PWM1[1]/ CAP1[0]	25[1]	I/O	**P1[18] —** General purpose digital input/output pin.
		O	**USB_UP_LED —** USB GoodLink LED indicator. It is LOW when the device is configured (non-control endpoints enabled), or when the host is enabled and has detected a device on the bus. It is HIGH when the device is not configured, or when host is enabled and has not detected a device on the bus, or during global suspend. It transitions between LOW and HIGH (flashes) when the host is enabled and detects activity on the bus.
		O	**PWM1[1] —** Pulse Width Modulator 1, channel 1 output.
		I	**CAP1[0] —** Capture input for Timer 1, channel 0.
P1[19]/MCOA0/ USB_PPWR CAP1[1]	26[1]	I/O	**P1[19] —** General purpose digital input/output pin.
		O	**MCOA0 —** Motor control PWM channel 0, output A.
		O	**$\overline{\text{USB\_PPWR}}$ —** Port Power enable signal for USB port. (LPC1759/58/56/54 only).
		I	**CAP1[1] —** Capture input for Timer 1, channel 1.
P1[20]/MCI0/ PWM1[2]/SCK0	27[1]	I/O	**P1[20] —** General purpose digital input/output pin.
		I	**MCI0 —** Motor control PWM channel 0, input. Also Quadrature Encoder Interface PHA input.
		O	**PWM1[2] —** Pulse Width Modulator 1, channel 2 output.
		I/O	**SCK0 —** Serial clock for SSP0.
P1[22]/MCOB0/ USB_PWRD/ MAT1[0]	28[1]	I/O	**P1[22] —** General purpose digital input/output pin.
		O	**MCOB0 —** Motor control PWM channel 0, output B.
		I	**USB_PWRD —** Power Status for USB port (host power switch). (LPC1759/58/56/54 only).
		O	**MAT1[0] —** Match output for Timer 1, channel 0.
P1[23]/MCI1/ PWM1[4]/MISO0	29[1]	I/O	**P1[23] —** General purpose digital input/output pin.
		I	**MCI1 —** Motor control PWM channel 1, input. Also Quadrature Encoder Interface PHB input.
		O	**PWM1[4] —** Pulse Width Modulator 1, channel 4 output.
		I/O	**MISO0 —** Master In Slave Out for SSP0.
P1[24]/MCI2/ PWM1[5]/MOSI0	30[1]	I/O	**P1[24] —** General purpose digital input/output pin.
		I	**MCI2 —** Motor control PWM channel 2, input. Also Quadrature Encoder Interface INDEX input.
		O	**PWM1[5] —** Pulse Width Modulator 1, channel 5 output.
		I/O	**MOSI0 —** Master Out Slave in for SSP0.
P1[25]/MCOA1/ MAT1[1]	31[1]	I/O	**P1[25] —** General purpose digital input/output pin.
		O	**MCOA1 —** Motor control PWM channel 1, output A.
		O	**MAT1[1] —** Match output for Timer 1, channel 1.
P1[26]/MCOB1/ PWM1[6]/CAP0[0]	32[1]	I/O	**P1[26] —** General purpose digital input/output pin.
		O	**MCOB1 —** Motor control PWM channel 1, output B.
		O	**PWM1[6] —** Pulse Width Modulator 1, channel 6 output.
		I	**CAP0[0] —** Capture input for Timer 0, channel 0.

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Table 4. Pin description *…continued*

Symbol	Pin	Type	Description
P1[28]/MCOA2/ PCAP1[0]/ MAT0[0]	35[1]	I/O	**P1[28] —** General purpose digital input/output pin.
		O	**MCOA2 —** Motor control PWM channel 2, output A.
		I	**PCAP1[0] —** Capture input for PWM1, channel 0.
		O	**MAT0[0] —** Match output for Timer 0, channel 0.
P1[29]/MCOB2/ PCAP1[1]/ MAT0[1]	36[1]	I/O	**P1[29] —** General purpose digital input/output pin.
		O	**MCOB2 —** Motor control PWM channel 2, output B.
		I	**PCAP1[1] —** Capture input for PWM1, channel 1.
		O	**MAT0[1] —** Match output for Timer 0, channel 1.
P1[30]/V_{BUS}/ AD0[4]	18[2]	I/O	**P1[30] —** General purpose digital input/output pin.
		I	**V_{BUS} —** Monitors the presence of USB bus power. **Note:** This signal must be HIGH for USB reset to occur.
		I	**AD0[4] —** A/D converter 0, input 4.
P1[31]/SCK1/ AD0[5]	17[2]	I/O	**P1[31] —** General purpose digital input/output pin.
		I/O	**SCK1 —** Serial Clock for SSP1.
		I	**AD0[5] —** A/D converter 0, input 5.
P2[0] to P2[31]		I/O	**Port 2:** Port 2 is a 32-bit I/O port with individual direction controls for each bit. The operation of port 2 pins depends upon the pin function selected via the pin connect block. Some port pins are not available on the LQFP80 package.
P2[0]/PWM1[1]/ TXD1	60[1]	I/O	**P2[0] —** General purpose digital input/output pin.
		O	**PWM1[1] —** Pulse Width Modulator 1, channel 1 output.
		O	**TXD1 —** Transmitter output for UART1.
P2[1]/PWM1[2]/ RXD1	59[1]	I/O	**P2[1] —** General purpose digital input/output pin.
		O	**PWM1[2] —** Pulse Width Modulator 1, channel 2 output.
		I	**RXD1 —** Receiver input for UART1.
P2[2]/PWM1[3]/ CTS1/ TRACEDATA[3]	58[1]	I/O	**P2[2] —** General purpose digital input/output pin.
		O	**PWM1[3] —** Pulse Width Modulator 1, channel 3 output.
		I	**CTS1 —** Clear to Send input for UART1.
		O	**TRACEDATA[3] —** Trace data, bit 3.
P2[3]/PWM1[4]/ DCD1/ TRACEDATA[2]	55[1]	I/O	**P2[3] —** General purpose digital input/output pin.
		O	**PWM1[4] —** Pulse Width Modulator 1, channel 4 output.
		I	**DCD1 —** Data Carrier Detect input for UART1.
		O	**TRACEDATA[2] —** Trace data, bit 2.
P2[4]/PWM1[5]/ DSR1/ TRACEDATA[1]	54[1]	I/O	**P2[4] —** General purpose digital input/output pin.
		O	**PWM1[5] —** Pulse Width Modulator 1, channel 5 output.
		I	**DSR1 —** Data Set Ready input for UART1.
		O	**TRACEDATA[1] —** Trace data, bit 1.
P2[5]/PWM1[6]/ DTR1/ TRACEDATA[0]	53[1]	I/O	**P2[5] —** General purpose digital input/output pin.
		O	**PWM1[6] —** Pulse Width Modulator 1, channel 6 output.
		O	**DTR1 —** Data Terminal Ready output for UART1. Can also be configured to be an RS-485/EIA-485 output enable signal.
		O	**TRACEDATA[0] —** Trace data, bit 0.

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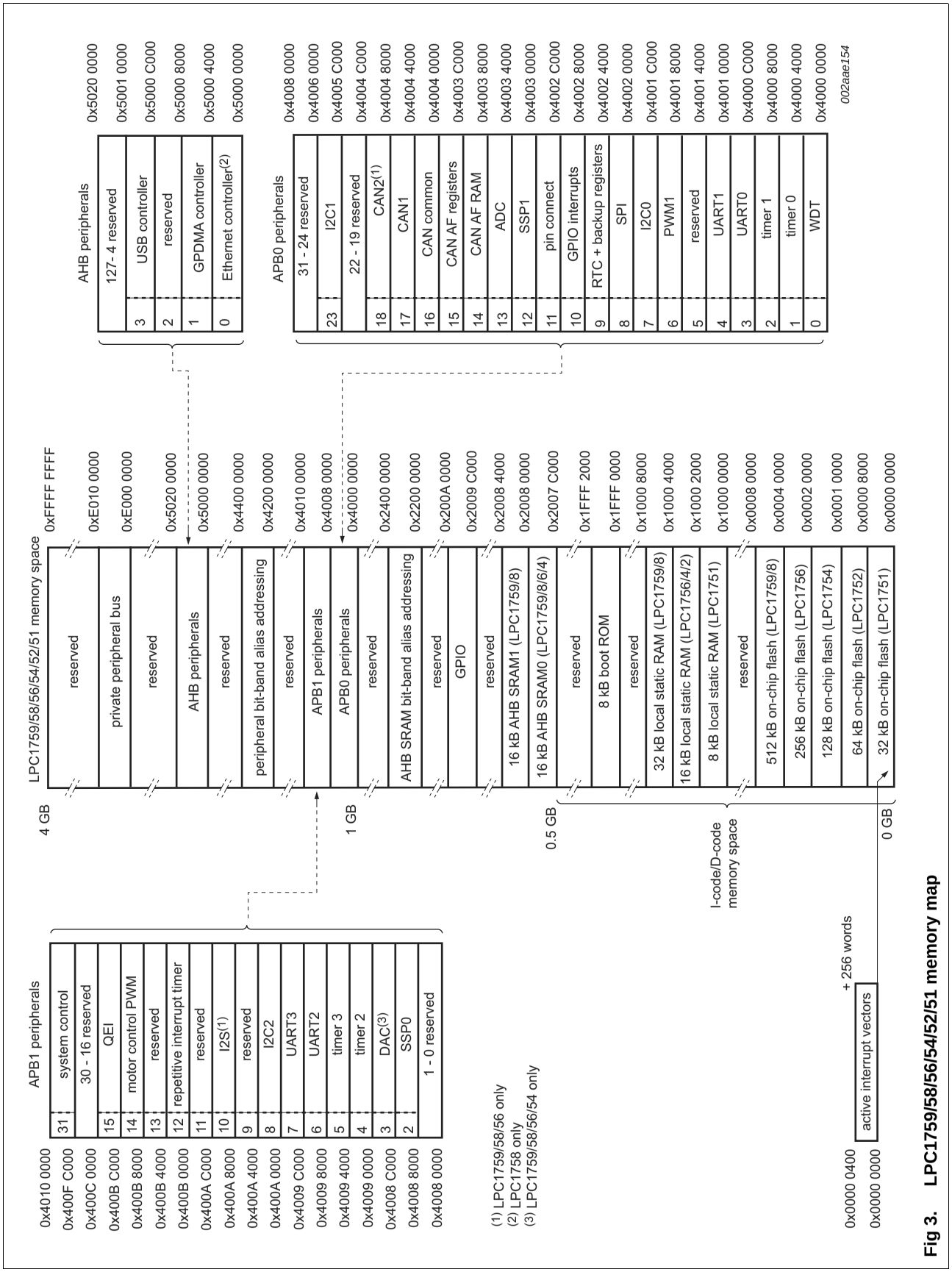

Fig 3. LPC1759/58/56/54/52/51 memory map

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8.13.1 Features

- One or two CAN controllers and buses.
- Data rates to 1 Mbit/s on each bus.
- 32-bit register and RAM access.
- Compatible with *CAN specification 2.0B, ISO 11898-1*.
- Global Acceptance Filter recognizes standard (11-bit) and extended-frame (29-bit) receive identifiers for all CAN buses.
- Acceptance Filter can provide FullCAN-style automatic reception for selected Standard Identifiers.
- FullCAN messages can generate interrupts.

8.14 12-bit ADC

The LPC1759/58/56/54/52/51 contain one ADC. It is a single 12-bit successive approximation ADC with six channels and DMA support.

8.14.1 Features

- 12-bit successive approximation ADC.
- Input multiplexing among 6 pins.
- Power-down mode.
- Measurement range VREFN to VREFP.
- 12-bit conversion rate: 200 kHz.
- Individual channels can be selected for conversion.
- Burst conversion mode for single or multiple inputs.
- Optional conversion on transition of input pin or Timer Match signal.
- Individual result registers for each ADC channel to reduce interrupt overhead.
- DMA support.

8.15 10-bit DAC (LPC1759/58/56/54 only)

The DAC allows to generate a variable analog output. The maximum output value of the DAC is VREFP.

8.15.1 Features

- 10-bit DAC
- Resistor string architecture
- Buffered output
- Power-down mode
- Selectable output drive
- Dedicated conversion timer
- DMA support

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The *I²S-bus specification* defines a 3-wire serial bus using one data line, one clock line, and one word select signal. The basic I²S connection has one master, which is always the master, and one slave. The I²S-bus interface provides a separate transmit and receive channel, each of which can operate as either a master or a slave.

8.20.1 Features

- The interface has separate input/output channels each of which can operate in master or slave mode.
- Capable of handling 8-bit, 16-bit, and 32-bit word sizes.
- Mono and stereo audio data supported.
- The sampling frequency can range from 16 kHz to 96 kHz (16, 22.05, 32, 44.1, 48, 96) kHz.
- Support for an audio master clock.
- Configurable word select period in master mode (separately for I²S input and output).
- Two 8-word FIFO data buffers are provided, one for transmit and one for receive.
- Generates interrupt requests when buffer levels cross a programmable boundary.
- Two DMA requests, controlled by programmable buffer levels. These are connected to the GPDMA block.
- Controls include reset, stop and mute options separately for I²S input and I²S output.

8.21 General purpose 32-bit timers/external event counters

The LPC1759/58/56/54/52/51 include four 32-bit timer/counters. The timer/counter is designed to count cycles of the system derived clock or an externally-supplied clock. It can optionally generate interrupts, generate timed DMA requests, or perform other actions at specified timer values, based on four match registers. Each timer/counter also includes two capture inputs to trap the timer value when an input signal transitions, optionally generating an interrupt.

8.21.1 Features

- A 32-bit timer/counter with a programmable 32-bit prescaler.
- Counter or timer operation.
- One 32-bit capture channel for timer 0 and two capture channels for timer 1. The capture channels can take a snapshot of the timer value when an input signal transitions. A capture event may also generate an interrupt.
- Four 32-bit match registers that allow:
  - Continuous operation with optional interrupt generation on match.
  - Stop timer on match with optional interrupt generation.
  - Reset timer on match with optional interrupt generation.
- Up to four external outputs corresponding to match registers, with the following capabilities:
  - Set LOW on match.
  - Set HIGH on match.
  - Toggle on match.

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8.28 RTC and backup registers

The RTC is a set of counters for measuring time when system power is on, and optionally when it is off. The RTC on the LPC1759/58/56/54/52/51 is designed to have extremely low power consumption, i.e. less than 1 μA. The RTC will typically run from the main chip power supply, conserving battery power while the rest of the device is powered up. When operating from a battery, the RTC will continue working down to 2.1 V. Battery power can be provided from a standard 3 V Lithium button cell.

An ultra-low power 32 kHz oscillator will provide a 1 Hz clock to the time counting portion of the RTC, moving most of the power consumption out of the time counting function.

The RTC includes a calibration mechanism to allow fine-tuning the count rate in a way that will provide less than 1 second per day error when operated at a constant voltage and temperature.

The RTC contains a small set of backup registers (20 bytes) for holding data while the main part of the LPC1759/58/56/54/52/51 is powered off.

The RTC includes an alarm function that can wake up the LPC1759/58/56/54/52/51 from all reduced power modes with a time resolution of 1 s.

8.28.1 Features

- Measures the passage of time to maintain a calendar and clock.
- Ultra low power design to support battery powered systems.
- Provides Seconds, Minutes, Hours, Day of Month, Month, Year, Day of Week, and Day of Year.
- Dedicated power supply pin can be connected to a battery or to the main 3.3 V.
- Periodic interrupts can be generated from increments of any field of the time registers.
- Backup registers (20 bytes) powered by VBAT.
- RTC power supply is isolated from the rest of the chip.

8.29 Clocking and power control

8.29.1 Crystal oscillators

The LPC1759/58/56/54/52/51 include three independent oscillators. These are the main oscillator, the IRC oscillator, and the RTC oscillator. Each oscillator can be used for more than one purpose as required in a particular application. Any of the three clock sources can be chosen by software to drive the main PLL and ultimately the CPU.

Following reset, the LPC1759/58/56/54/52/51 will operate from the Internal RC oscillator until switched by software. This allows systems to operate without any external crystal and the bootloader code to operate at a known frequency.

See Figure 4 for an overview of the LPC1759/58/56/54/52/51 clock generation.

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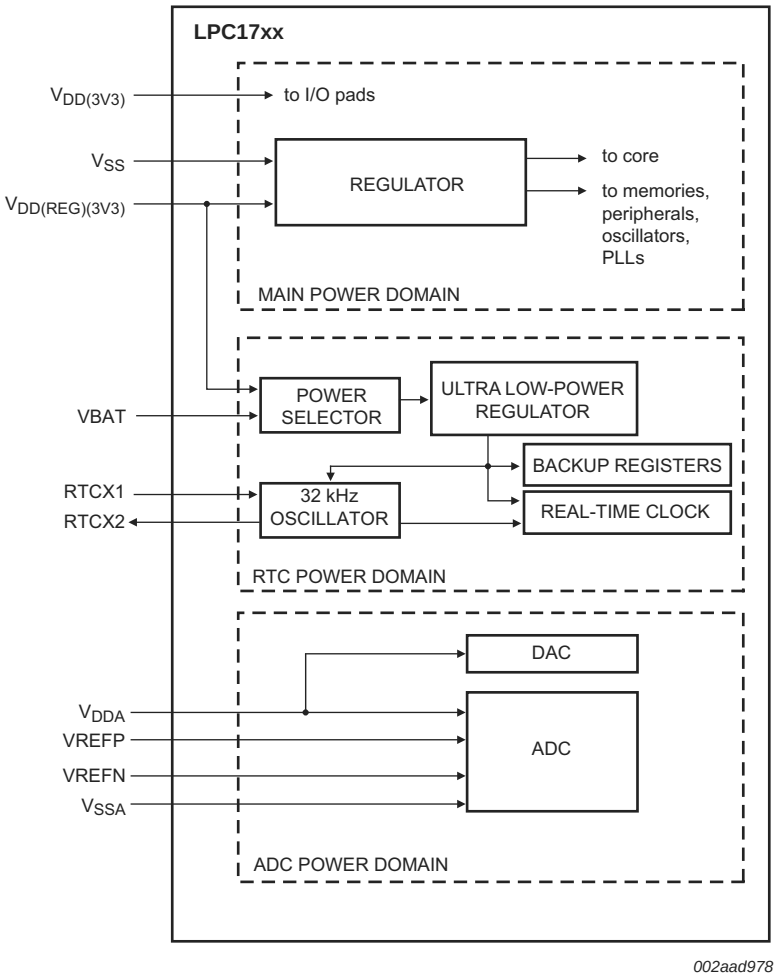

Fig 5. Power distribution

8.30 System control

8.30.1 Reset

Reset has four sources on the LPC17xx: the $\overline{\text{RESET}}$ pin, the Watchdog reset, power-on reset (POR), and the BrownOut Detection (BOD) circuit. The $\overline{\text{RESET}}$ pin is a Schmitt trigger input pin. Assertion of chip Reset by any source, once the operating voltage attains a usable level, causes the $\overline{\text{RSTOUT}}$ pin to go LOW and starts the wake-up timer (see description in Section 8.29.4). The wake-up timer ensures that reset remains asserted until the external Reset is de-asserted, the oscillator is running, a fixed number of clocks have passed, and the flash controller has completed its initialization. Once reset is de-asserted, or, in case of a BOD-triggered reset, once the voltage rises above the BOD threshold, the $\overline{\text{RSTOUT}}$ pin goes HIGH.

When the internal Reset is removed, the processor begins executing at address 0, which is initially the Reset vector mapped from the boot block. At that point, all of the processor and peripheral registers have been initialized to predetermined values.

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10. Thermal characteristics

10.1 Thermal characteristics

The average chip junction temperature, T_J (°C), can be calculated using the following equation:

$$T_J = T_{amb} + (P_D \times R_{th(j-a)}) \quad (1)$$

- T_{amb} = ambient temperature (°C),
- $R_{th(j-a)}$ = the package junction-to-ambient thermal resistance (°C/W)
- P_D = sum of internal and I/O power dissipation

The internal power dissipation is the product of I_{DD} and V_{DD}. The I/O power dissipation of the I/O pins is often small and many times can be negligible. However it can be significant in some applications.

Table 6. Thermal resistance (±15 %)

Symbol	Parameter	Conditions	Max/Min	Unit
LQFP80				
$R_{th(j-a)}$	thermal resistance from junction to ambient	JEDEC (4.5 in × 4 in); still air	39.46	°C/W
		Single-layer (4.5 in × 3 in); still air	59.39	°C/W
$R_{th(j-c)}$	thermal resistance from junction to case		6.769	°C/W

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[15] TCK/SWDCLK pin needs to be externally pulled LOW.

[16] V_{DDA} = 3.3 V; T_{amb} = 25 °C.

[17] The ADC is powered if the PDN bit in the AD0CR register is set to 1. See *LPC17xx user manual UM10360*.

[18] The ADC is in Power-down mode if the PDN bit in the AD0CR register is set to 0. See *LPC17xx user manual UM10360*.

[19] $V_{i(VREFP)}$ = 3.3 V; T_{amb} = 25 °C.

[20] Including voltage on outputs in 3-state mode.

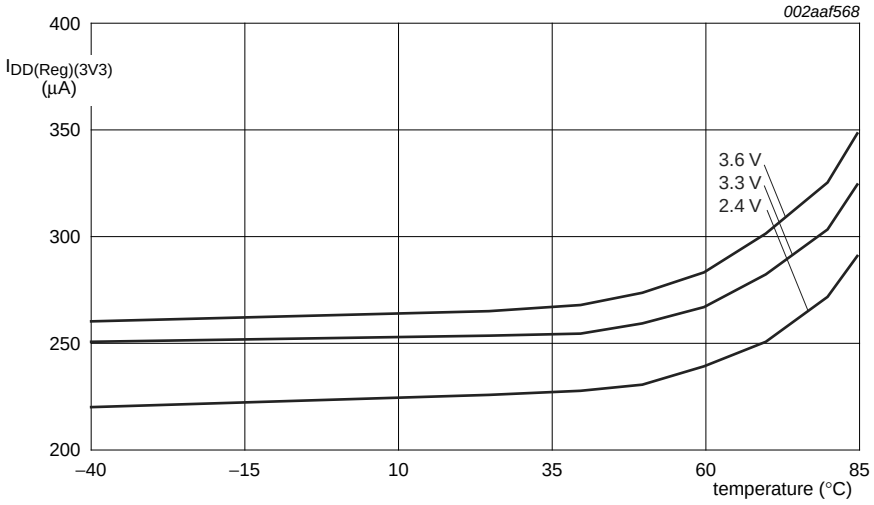
[21] $V_{DD(3V3)}$ supply voltage ≥ 2.4 V.

[22] 3-state outputs go into 3-state mode in Deep power-down mode.

[23] Allowed as long as the current limit does not exceed the maximum current allowed by the device.

[24] Includes external resistors of 33 Ω ± 1 % on D+ and D−.

11.1 Power consumption



Conditions: $V_{DD(Reg)(3V3)}$ = 3.3 V; BOD disabled.

Fig 6. Deep-sleep mode: Typical regulator supply current $I_{DD(Reg)(3V3)}$ versus temperature

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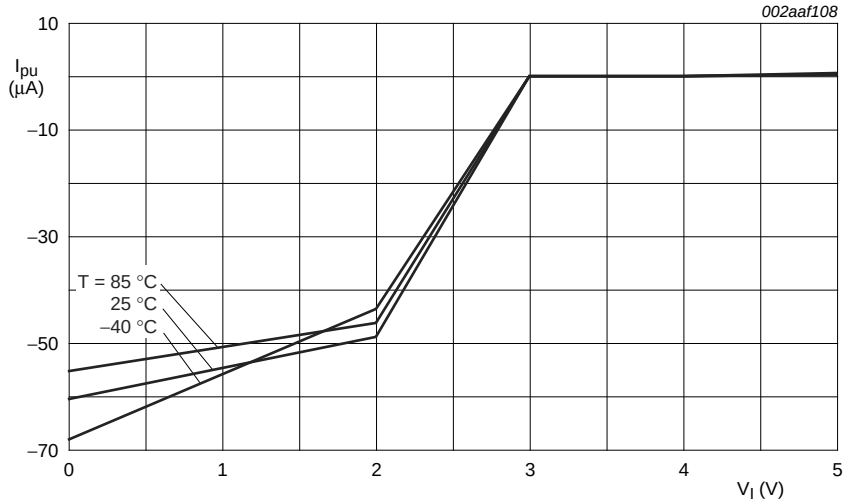
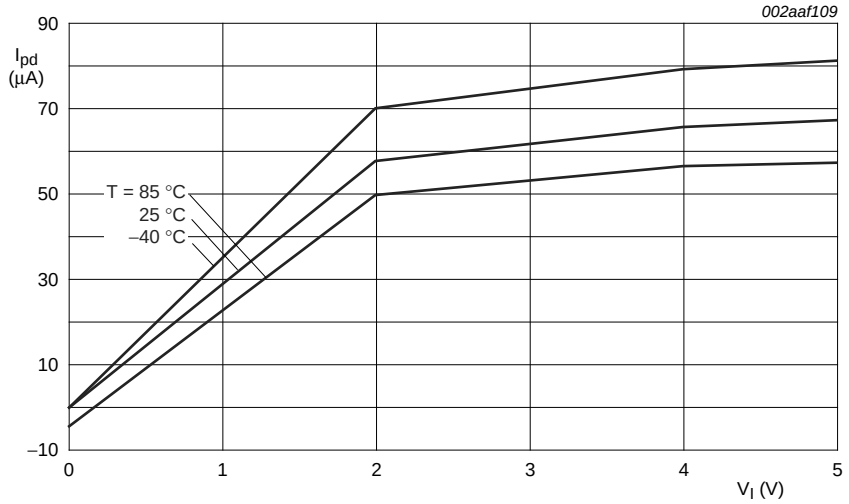


Conditions: $V_{DD(REG)(3V3)} = V_{DD(3V3)} = 3.3$ V; standard port pins.

Fig 12. Typical pull-up current I_{pu} versus input voltage V_I



Conditions: $V_{DD(REG)(3V3)} = V_{DD(3V3)} = 3.3$ V; standard port pins.

Fig 13. Typical pull-down current I_{pd} versus input voltage V_I

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12. Dynamic characteristics

12.1 Flash memory

Table 9. Flash characteristics

T_{amb} = −40 °C to +85 °C, unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
N_{endu}	endurance		[1]	10000	100000	-	cycles
t_{ret}	retention time	powered		10	-	-	years
		unpowered		20	-	-	years
t_{er}	erase time	sector or multiple consecutive sectors		95	100	105	ms
t_{prog}	programming time		[2]	0.95	1	1.05	ms

[1] Number of program/erase cycles.

[2] Programming times are given for writing 256 bytes from RAM to the flash. Data must be written to the flash in blocks of 256 bytes.

12.2 External clock

Table 10. Dynamic characteristic: external clock

T_{amb} = −40 °C to +85 °C; $V_{DD(3V3)}$ over specified ranges.[1]

Symbol	Parameter	Conditions		Min	Typ[2]	Max	Unit
f_{osc}	oscillator frequency			1	-	25	MHz
$T_{cy(clk)}$	clock cycle time			40	-	1000	ns
t_{CHCX}	clock HIGH time			$T_{cy(clk)} \times 0.4$	-	-	ns
t_{CLCX}	clock LOW time			$T_{cy(clk)} \times 0.4$	-	-	ns
t_{CLCH}	clock rise time			-	-	5	ns
t_{CHCL}	clock fall time			-	-	5	ns

[1] Parameters are valid over operating temperature range unless otherwise specified.

[2] Typical ratings are not guaranteed. The values listed are at room temperature (25 °C), nominal supply voltages.

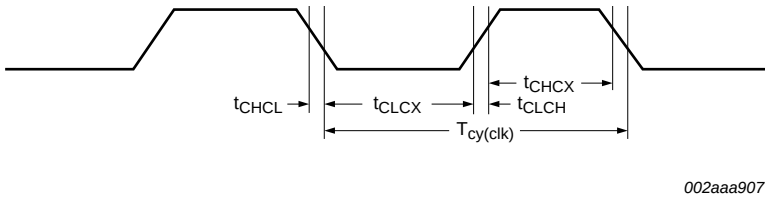

Fig 14. External clock timing (with an amplitude of at least $V_{i(RMS)}$ = 200 mV)

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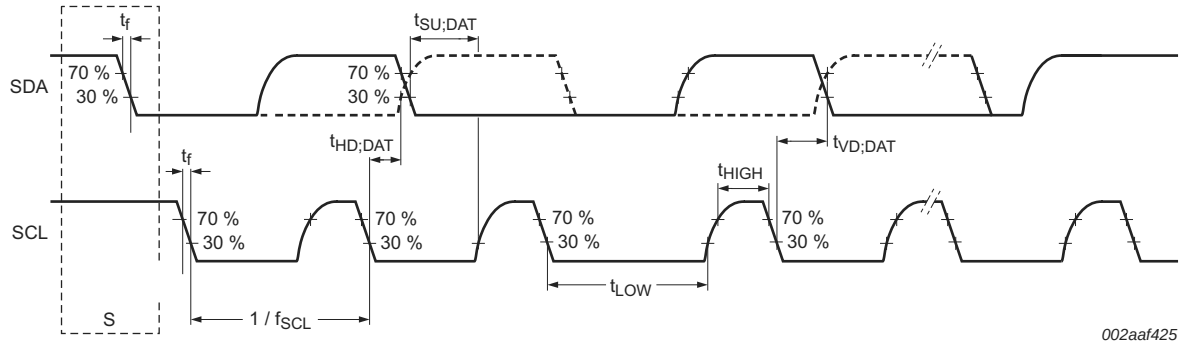

Fig 16. I²C-bus pins clock timing

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12.6 I²S-bus interface (LPC1759/58/56 only)

Table 14. Dynamic characteristics: I²S-bus interface pins

T_{amb} = −40 °C to +85 °C.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
common to input and output							
t_r	rise time		[1]	-	-	35	ns
t_f	fall time		[1]	-	-	35	ns
t_{WH}	pulse width HIGH	on pins I2STX_CLK and I2SRX_CLK	[1]	$0.495 \times T_{cy(clk)}$	-	-	-
t_{WL}	pulse width LOW	on pins I2STX_CLK and I2SRX_CLK	[1]	-	-	$0.505 \times T_{cy(clk)}$	ns
output							
$t_{v(Q)}$	data output valid time	on pin I2STX_SDA;	[1]	-	-	30	ns
		on pin I2STX_WS	[1]	-	-	30	ns
input							
$t_{su(D)}$	data input set-up time	on pin I2SRX_SDA	[1]	3.5	-	-	ns
$t_{h(D)}$	data input hold time	on pin I2SRX_SDA	[1]	4.0	-	-	ns

[1] CCLK = 20 MHz; peripheral clock to the I²S-bus interface PCLK = $^{CCLK}/_{4}$; $T_{cy(clk)}$ = 1600 ns, corresponds to the SCK signal in the *I²S-bus specification*.

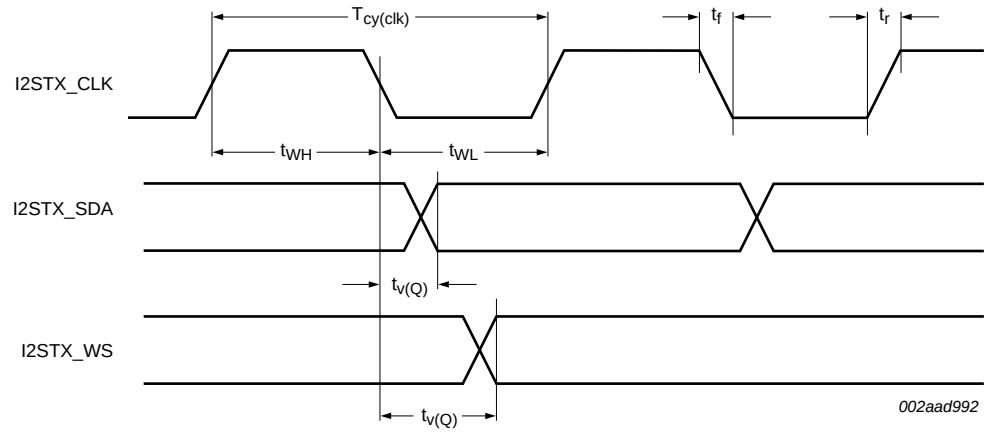

Fig 17. I²S-bus timing (output)

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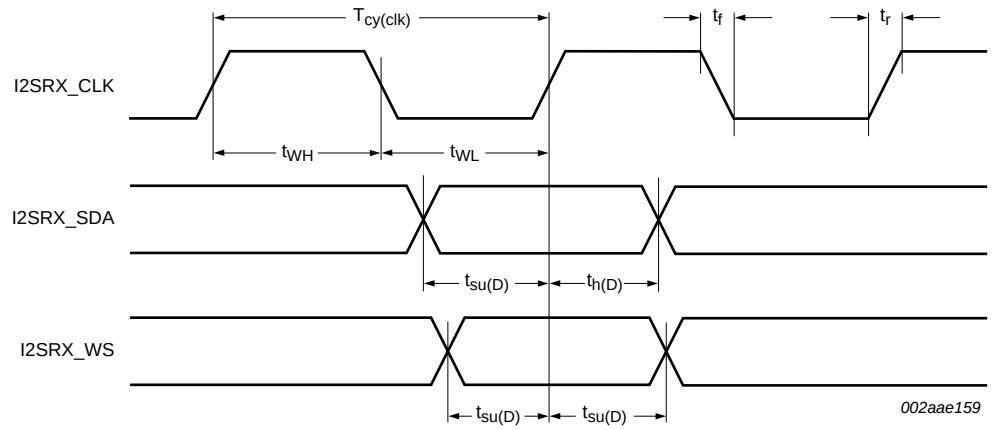

Fig 18. I²S-bus timing (input)

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12.8 USB interface

Table 16. Dynamic characteristics: USB pins (full-speed)

C_L = 50 pF; R_{pu} = 1.5 kΩ on D+ to $V_{DD(3V3)}$; 3.0 V ≤ $V_{DD(3V3)}$ ≤ 3.6 V.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
t_r	rise time	10 % to 90 %		8.5	-	13.8	ns
t_f	fall time	10 % to 90 %		7.7	-	13.7	ns
t_{FRFM}	differential rise and fall time matching	t_r / t_f		-	-	109	%
V_{CRS}	output signal crossover voltage			1.3	-	2.0	V
t_{FEOPT}	source SE0 interval of EOP	see Figure 21		160	-	175	ns
t_{FDEOP}	source jitter for differential transition to SE0 transition	see Figure 21		−2	-	+5	ns
t_{JR1}	receiver jitter to next transition			−18.5	-	+18.5	ns
t_{JR2}	receiver jitter for paired transitions	10 % to 90 %		−9	-	+9	ns
t_{EOPR1}	EOP width at receiver	must reject as EOP; see Figure 21	[1]	40	-	-	ns
t_{EOPR2}	EOP width at receiver	must accept as EOP; see Figure 21	[1]	82	-	-	ns

[1] Characterized but not implemented as production test. Guaranteed by design.

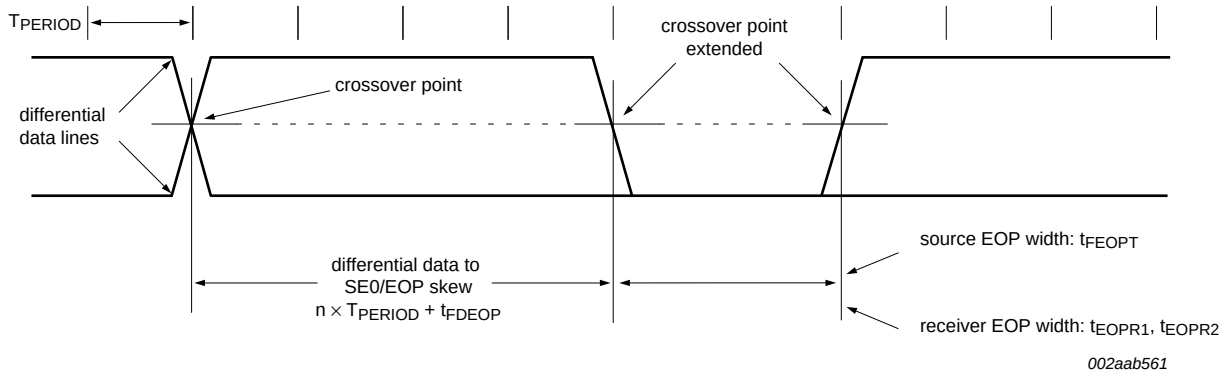

Fig 21. Differential data-to-EOP transition skew and EOP width

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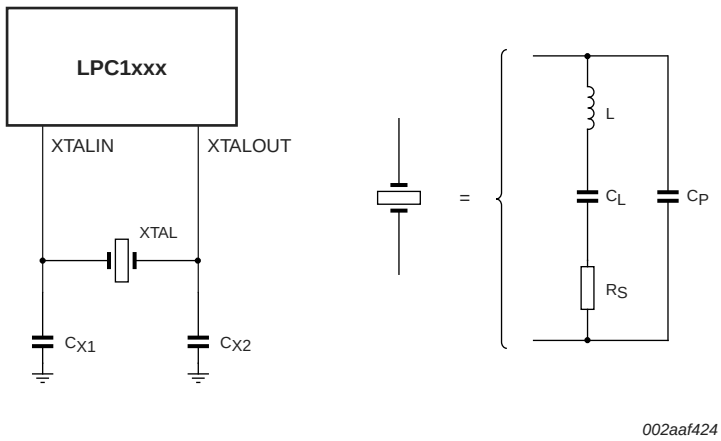

Fig 35. Oscillator modes and models: oscillation mode of operation and external crystal model used for C_{X1}/C_{X2} evaluation

Table 22. Recommended values for C_{X1}/C_{X2} in oscillation mode (crystal and external components parameters): low frequency mode

Fundamental oscillation frequency F_{OSC}	Crystal load capacitance C_L	Maximum crystal series resistance R_S	External load capacitors C_{X1}/C_{X2}
1 MHz to 5 MHz	10 pF	< 300 Ω	18 pF, 18 pF
	20 pF	< 300 Ω	39 pF, 39 pF
	30 pF	< 300 Ω	57 pF, 57 pF
5 MHz to 10 MHz	10 pF	< 300 Ω	18 pF, 18 pF
	20 pF	< 200 Ω	39 pF, 39 pF
	30 pF	< 100 Ω	57 pF, 57 pF
10 MHz to 15 MHz	10 pF	< 160 Ω	18 pF, 18 pF
	20 pF	< 60 Ω	39 pF, 39 pF
15 MHz to 20 MHz	10 pF	< 80 Ω	18 pF, 18 pF

Table 23. Recommended values for C_{X1}/C_{X2} in oscillation mode (crystal and external components parameters): high frequency mode

Fundamental oscillation frequency F_{OSC}	Crystal load capacitance C_L	Maximum crystal series resistance R_S	External load capacitors C_{X1}, C_{X2}
15 MHz to 20 MHz	10 pF	< 180 Ω	18 pF, 18 pF
	20 pF	< 100 Ω	39 pF, 39 pF
20 MHz to 25 MHz	10 pF	< 160 Ω	18 pF, 18 pF
	20 pF	< 80 Ω	39 pF, 39 pF

15.3 XTAL Printed-Circuit Board (PCB) layout guidelines

The crystal should be connected on the PCB as close as possible to the oscillator input and output pins of the chip. Take care that the load capacitors C_{x1}, C_{x2}, and C_{x3} in case of third overtone crystal usage have a common ground plane. The external components must also be connected to the ground plain. Loops must be made as small as possible in

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18. Abbreviations

Table 25. Abbreviations

Acronym	Description
ADC	Analog-to-Digital Converter
AHB	Advanced High-performance Bus
AMBA	Advanced Microcontroller Bus Architecture
APB	Advanced Peripheral Bus
BOD	BrownOut Detection
CAN	Controller Area Network
DAC	Digital-to-Analog Converter
DMA	Direct Memory Access
EOP	End Of Packet
GPIO	General Purpose Input/Output
IRC	Internal RC
IrDA	Infrared Data Association
JTAG	Joint Test Action Group
MAC	Media Access Control
MIIM	Media Independent Interface Management
OTG	On-The-Go
PHY	Physical Layer
PLL	Phase-Locked Loop
PWM	Pulse Width Modulator
RMII	Reduced Media Independent Interface
SE0	Single Ended Zero
SPI	Serial Peripheral Interface
SSI	Serial Synchronous Interface
SSP	Synchronous Serial Port
TTL	Transistor-Transistor Logic
UART	Universal Asynchronous Receiver/Transmitter
USB	Universal Serial Bus

19. References

[1] LPC176x/5x User manual UM10360:
http://www.nxp.com/documents/user_manual/UM10360.pdf

[2] LPC175x Errata sheet:
http://www.nxp.com/documents/errata_sheet/ES_LPC175X.pdf

[3] Technical note ADC design guidelines:
http://www.nxp.com/documents/technical_note/TN00009.pdf

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