



Welcome to [E-XFL.COM](#)

### What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

### Applications of "[Embedded - Microcontrollers](#)"

#### Details

Product Status	Active
Core Processor	ARM® Cortex®-M3
Core Size	32-Bit Single-Core
Speed	48MHz
Connectivity	I <sup>2</sup> C, IrDA, SmartCard, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, LCD, POR, PWM, WDT
Number of I/O	50
Program Memory Size	512KB (512K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	128K x 8
Voltage - Supply (Vcc/Vdd)	1.98V ~ 3.8V
Data Converters	A/D 8x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-TQFP
Supplier Device Package	64-TQFP (10x10)
Purchase URL	<a href="https://www.e-xfl.com/product-detail/silicon-labs/efm32gg942f512g-e-qfp64">https://www.e-xfl.com/product-detail/silicon-labs/efm32gg942f512g-e-qfp64</a>

### 2.1.18 Low Energy Timer (LETIMER)

The unique LETIMER<sup>™</sup>, the Low Energy Timer, is a 16-bit timer that is available in energy mode EM2 in addition to EM1 and EM0. Because of this, it can be used for timing and output generation when most of the device is powered down, allowing simple tasks to be performed while the power consumption of the system is kept at an absolute minimum. The LETIMER can be used to output a variety of waveforms with minimal software intervention. It is also connected to the Real Time Counter (RTC), and can be configured to start counting on compare matches from the RTC.

### 2.1.19 Pulse Counter (PCNT)

The Pulse Counter (PCNT) can be used for counting pulses on a single input or to decode quadrature encoded inputs. It runs off either the internal LFACLK or the PCNTn\_S0IN pin as external clock source. The module may operate in energy mode EM0 - EM3.

### 2.1.20 Analog Comparator (ACMP)

The Analog Comparator is used to compare the voltage of two analog inputs, with a digital output indicating which input voltage is higher. Inputs can either be one of the selectable internal references or from external pins. Response time and thereby also the current consumption can be configured by altering the current supply to the comparator.

### 2.1.21 Voltage Comparator (VCMP)

The Voltage Supply Comparator is used to monitor the supply voltage from software. An interrupt can be generated when the supply falls below or rises above a programmable threshold. Response time and thereby also the current consumption can be configured by altering the current supply to the comparator.

### 2.1.22 Analog to Digital Converter (ADC)

The ADC is a Successive Approximation Register (SAR) architecture, with a resolution of up to 12 bits at up to one million samples per second. The integrated input mux can select inputs from 8 external pins and 6 internal signals.

### 2.1.23 Digital to Analog Converter (DAC)

The Digital to Analog Converter (DAC) can convert a digital value to an analog output voltage. The DAC is fully differential rail-to-rail, with 12-bit resolution. It has two single ended output buffers which can be combined into one differential output. The DAC may be used for a number of different applications such as sensor interfaces or sound output.

### 2.1.24 Operational Amplifier (OPAMP)

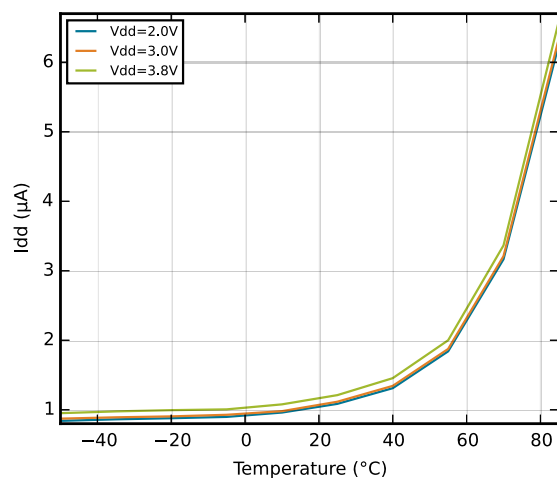
The EFM32GG942 features 3 Operational Amplifiers. The Operational Amplifier is a versatile general purpose amplifier with rail-to-rail differential input and rail-to-rail single ended output. The input can be set to pin, DAC or OPAMP, whereas the output can be pin, OPAMP or ADC. The current is programmable and the OPAMP has various internal configurations such as unity gain, programmable gain using internal resistors etc.

### 2.1.25 Low Energy Sensor Interface (LESENSE)

The Low Energy Sensor Interface (LESENSE<sup>™</sup>), is a highly configurable sensor interface with support for up to 4 individually configurable sensors. By controlling the analog comparators and DAC, LESENSE is capable of supporting a wide range of sensors and measurement schemes, and can for instance measure LC sensors, resistive sensors and capacitive sensors. LESENSE also includes a programmable

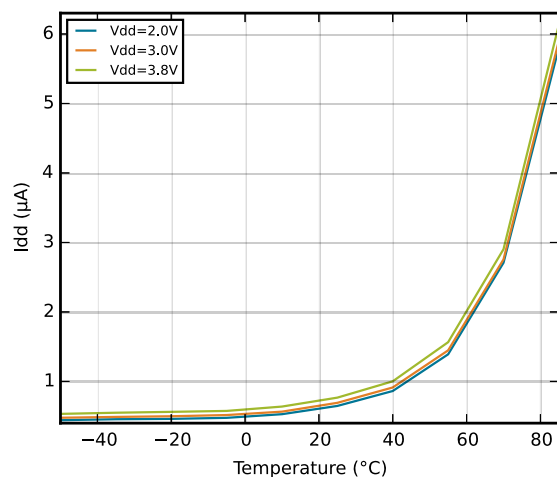
### 3.4.1 EM2 Current Consumption

**Figure 3.1. EM2 current consumption. RTC<sup>1</sup> prescaled to 1 Hz, 32.768 kHz LFRCO.**



### 3.4.2 EM3 Current Consumption

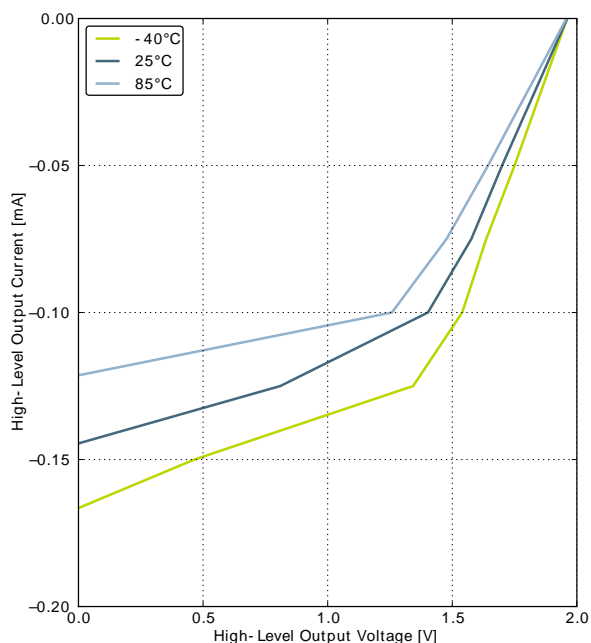
**Figure 3.2. EM3 current consumption.**



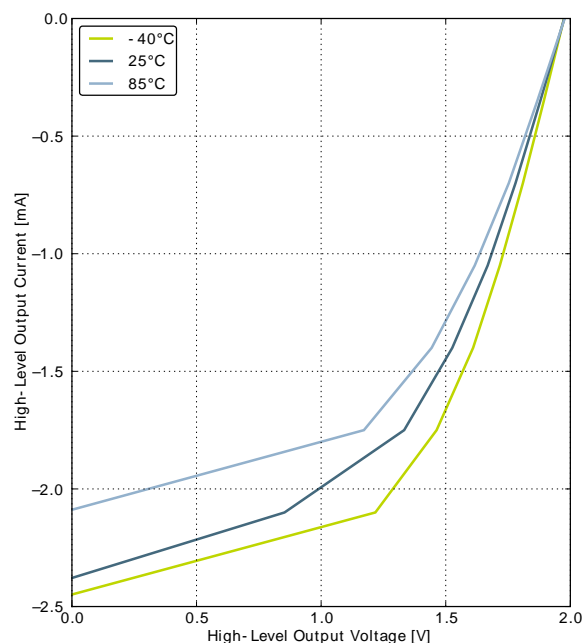
<sup>1</sup>Using backup RTC.

**Table 3.5. Power Management**

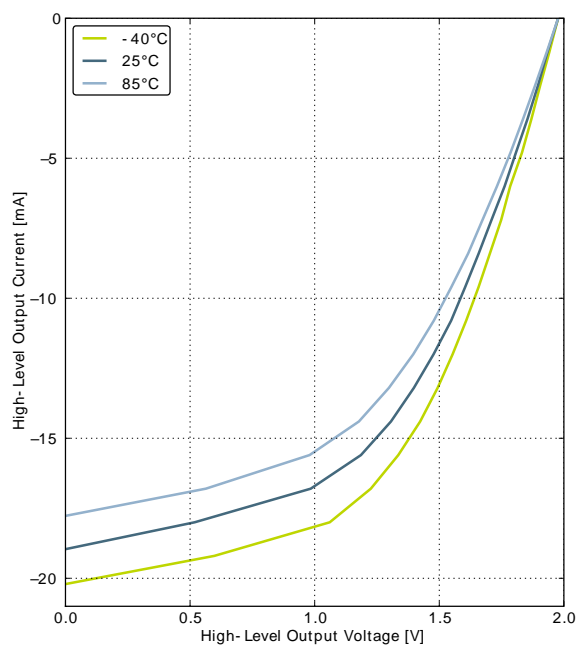
Symbol	Parameter	Condition	Min	Typ	Max	Unit
V <sub>BODextthr-</sub>	BOD threshold on falling external supply voltage	EM0	1.74		1.96	V
		EM2	1.74		1.98	V
V <sub>BODintthr-</sub>	BOD threshold on falling internally regulated supply voltage		1.57		1.70	V
V <sub>BODextthr+</sub>	BOD threshold on rising external supply voltage			1.85	1.98	V
V <sub>PORthr+</sub>	Power-on Reset (POR) threshold on rising external supply voltage				1.98	V
t <sub>RESET</sub>	Delay from reset is released until program execution starts	Applies to Power-on Reset, Brown-out Reset and pin reset.		163		μs
C <sub>DECOUPLE</sub>	Voltage regulator decoupling capacitor.	X5R capacitor recommended. Apply between DECOUPLE pin and GROUND		1		μF
C <sub>USB_VREGO</sub>	USB voltage regulator out decoupling capacitor.	X5R capacitor recommended. Apply between USB_VREGO pin and GROUND		1		μF
C <sub>USB_VREGI</sub>	USB voltage regulator in decoupling capacitor.	X5R capacitor recommended. Apply between USB_VREGI pin and GROUND		4.7		μF

**Figure 3.5. Typical High-Level Output Current, 2V Supply Voltage**

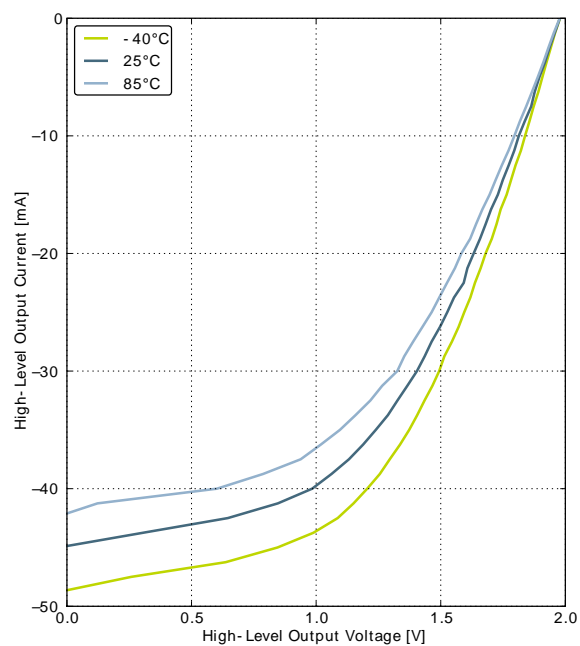
GPIO\_Px\_CTRL DRIVEMODE = LOWEST



GPIO\_Px\_CTRL DRIVEMODE = LOW



GPIO\_Px\_CTRL DRIVEMODE = STANDARD



GPIO\_Px\_CTRL DRIVEMODE = HIGH

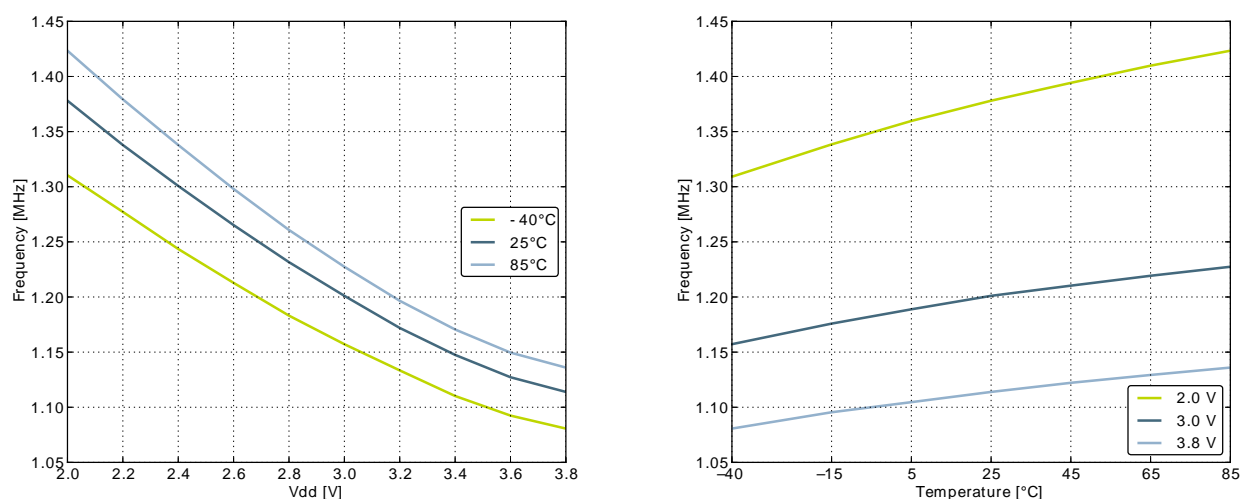
Symbol	Parameter	Condition	Min	Typ	Max	Unit
$I_{\text{HFRCO}}$	Current consumption (Production test condition = 14MHz)	$f_{\text{HFRCO}} = 28 \text{ MHz}$		165	190	$\mu\text{A}$
		$f_{\text{HFRCO}} = 21 \text{ MHz}$		134	155	$\mu\text{A}$
		$f_{\text{HFRCO}} = 14 \text{ MHz}$		106	120	$\mu\text{A}$
		$f_{\text{HFRCO}} = 11 \text{ MHz}$		94	110	$\mu\text{A}$
		$f_{\text{HFRCO}} = 6.6 \text{ MHz}$		77	90	$\mu\text{A}$
		$f_{\text{HFRCO}} = 1.2 \text{ MHz}$		25	32	$\mu\text{A}$
$\text{TUNESTEP}_{\text{HFRCO}}$	Frequency step for LSB change in TUNING value			0.3 <sup>3</sup>		%

<sup>1</sup>For devices with prod. rev. < 19, Typ = 7MHz and Min/Max values not applicable.

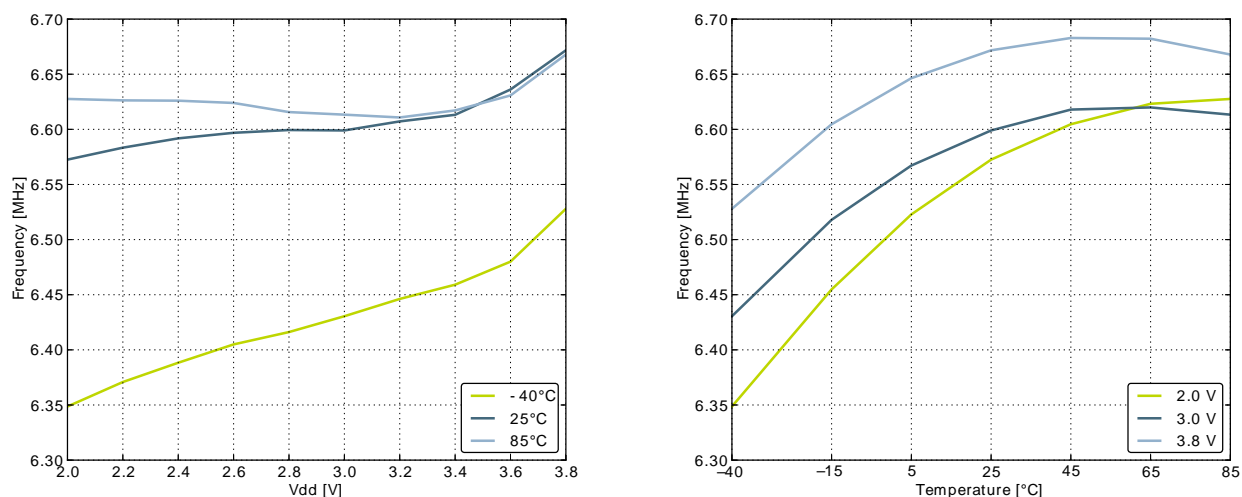
<sup>2</sup>For devices with prod. rev. < 19, Typ = 1MHz and Min/Max values not applicable.

<sup>3</sup>The TUNING field in the CMU\_HFRCOCTRL register may be used to adjust the HFRCO frequency. There is enough adjustment range to ensure that the frequency bands above 7 MHz will always have some overlap across supply voltage and temperature. By using a stable frequency reference such as the LFXO or HFXO, a firmware calibration routine can vary the TUNING bits and the frequency band to maintain the HFRCO frequency at any arbitrary value between 7 MHz and 28 MHz across operating conditions.

**Figure 3.11. Calibrated HFRCO 1 MHz Band Frequency vs Supply Voltage and Temperature**



**Figure 3.12. Calibrated HFRCO 7 MHz Band Frequency vs Supply Voltage and Temperature**



### 3.9.6 ULFRCO

**Table 3.13. ULFRCO**

Symbol	Parameter	Condition	Min	Typ	Max	Unit
$f_{ULFRCO}$	Oscillation frequency	25°C, 3V	0.70		1.75	kHz
$TC_{ULFRCO}$	Temperature coefficient			0.05		%/°C
$VC_{ULFRCO}$	Supply voltage coefficient			-18.2		%/V

## 3.10 Analog Digital Converter (ADC)

**Table 3.14. ADC**

Symbol	Parameter	Condition	Min	Typ	Max	Unit
$V_{ADCIN}$	Input voltage range	Single ended	0		$V_{REF}$	V
		Differential	$-V_{REF}/2$		$V_{REF}/2$	V
$V_{ADCREFIN}$	Input range of external reference voltage, single ended and differential		1.25		$V_{DD}$	V
$V_{ADCREFIN\_CH7}$	Input range of external negative reference voltage on channel 7	See $V_{ADCREFIN}$	0		$V_{DD} - 1.1$	V
$V_{ADCREFIN\_CH6}$	Input range of external positive reference voltage on channel 6	See $V_{ADCREFIN}$	0.625		$V_{DD}$	V
$V_{ADCCMIN}$	Common mode input range		0		$V_{DD}$	V
$I_{ADCIN}$	Input current	2pF sampling capacitors		<100		nA
$CMRR_{ADC}$	Analog input common mode rejection ratio			65		dB
$I_{ADC}$	Average active current	1 MSamples/s, 12 bit, external reference		351		μA
		10 kSamples/s 12 bit, internal 1.25 V reference, WARMUP-MODE in ADCn_CTRL set to 0b00		67		μA
		10 kSamples/s 12 bit, internal 1.25 V reference, WARMUP-MODE in ADCn_CTRL set to 0b01		63		μA
		10 kSamples/s 12 bit, internal 1.25 V reference, WARMUP-MODE in ADCn_CTRL set to 0b10		64		μA
$I_{ADCREF}$	Current consumption of internal voltage reference	Internal voltage reference		65		μA

Symbol	Parameter	Condition	Min	Typ	Max	Unit
C <sub>ADCIN</sub>	Input capacitance			2		pF
R <sub>ADCIN</sub>	Input ON resistance		1			MOhm
R <sub>ADCFILT</sub>	Input RC filter resistance			10		kOhm
C <sub>ADCFILT</sub>	Input RC filter/de-coupling capacitance			250		fF
f <sub>ADCCLK</sub>	ADC Clock Frequency				13	MHz
t <sub>ADCCONV</sub>	Conversion time	6 bit	7			ADC-CLK Cycles
		8 bit	11			ADC-CLK Cycles
		12 bit	13			ADC-CLK Cycles
t <sub>ADCACQ</sub>	Acquisition time	Programmable	1		256	ADC-CLK Cycles
t <sub>ADCACQVDD3</sub>	Required acquisition time for VDD/3 reference		2			μs
t <sub>ADCSTART</sub>	Startup time of reference generator and ADC core in NORMAL mode			5		μs
	Startup time of reference generator and ADC core in KEEPADCWARM mode			1		μs
SNR <sub>ADC</sub>	Signal to Noise Ratio (SNR)	1 MSamples/s, 12 bit, single ended, internal 1.25V reference		59		dB
		1 MSamples/s, 12 bit, single ended, internal 2.5V reference		63		dB
		1 MSamples/s, 12 bit, single ended, V <sub>DD</sub> reference		65		dB
		1 MSamples/s, 12 bit, differential, internal 1.25V reference		60		dB
		1 MSamples/s, 12 bit, differential, internal 2.5V reference		65		dB
		1 MSamples/s, 12 bit, differential, 5V reference		54		dB
		1 MSamples/s, 12 bit, differential, V <sub>DD</sub> reference		67		dB
		1 MSamples/s, 12 bit, differential, 2xV <sub>DD</sub> reference		69		dB



Symbol	Parameter	Condition	Min	Typ	Max	Unit
		200 kSamples/s, 12 bit, differential, $2xV_{DD}$ reference		69		dB
SFDR <sub>ADC</sub>	Spurious-Free Dynamic Range (SFDR)	1 MSamples/s, 12 bit, single ended, internal 1.25V reference		64		dBc
		1 MSamples/s, 12 bit, single ended, internal 2.5V reference		76		dBc
		1 MSamples/s, 12 bit, single ended, $V_{DD}$ reference		73		dBc
		1 MSamples/s, 12 bit, differential, internal 1.25V reference		66		dBc
		1 MSamples/s, 12 bit, differential, internal 2.5V reference		77		dBc
		1 MSamples/s, 12 bit, differential, $V_{DD}$ reference		76		dBc
		1 MSamples/s, 12 bit, differential, $2xV_{DD}$ reference		75		dBc
		1 MSamples/s, 12 bit, differential, 5V reference		69		dBc
		200 kSamples/s, 12 bit, single ended, internal 1.25V reference		75		dBc
		200 kSamples/s, 12 bit, single ended, internal 2.5V reference		75		dBc
		200 kSamples/s, 12 bit, single ended, $V_{DD}$ reference		76		dBc
		200 kSamples/s, 12 bit, differential, internal 1.25V reference		79		dBc
		200 kSamples/s, 12 bit, differential, internal 2.5V reference		79		dBc
		200 kSamples/s, 12 bit, differential, 5V reference		78		dBc
		200 kSamples/s, 12 bit, differential, $V_{DD}$ reference	68	79		dBc
		200 kSamples/s, 12 bit, differential, $2xV_{DD}$ reference		79		dBc
V <sub>ADCOFFSET</sub>	Offset voltage	After calibration, single ended		0.3		mV
		After calibration, differential	-3	0.3	3	mV
TGRAD <sub>ADCTH</sub>	Thermometer output gradient			-1.92		mV/°C
				-6.3		ADC Codes/°C
DNL <sub>ADC</sub>	Differential non-linearity (DNL)	$V_{DD}=3.0\text{ V}$ , external 2.5V reference	-1	±0.7	4	LSB
INL <sub>ADC</sub>	Integral non-linearity (INL), End point method			±1.2	±3.0	LSB
MC <sub>ADC</sub>	No missing codes		11.999 <sup>1</sup>	12		bits

Symbol	Parameter	Condition	Min	Typ	Max	Unit
GAIN <sub>ED</sub>	Gain error drift	1.25V reference		0.01 <sup>2</sup>	0.033 <sup>3</sup>	%/°C
		2.5V reference		0.01 <sup>2</sup>	0.03 <sup>3</sup>	%/°C
OFFSET <sub>ED</sub>	Offset error drift	1.25V reference		0.2 <sup>2</sup>	0.7 <sup>3</sup>	LSB/°C
		2.5V reference		0.2 <sup>2</sup>	0.62 <sup>3</sup>	LSB/°C

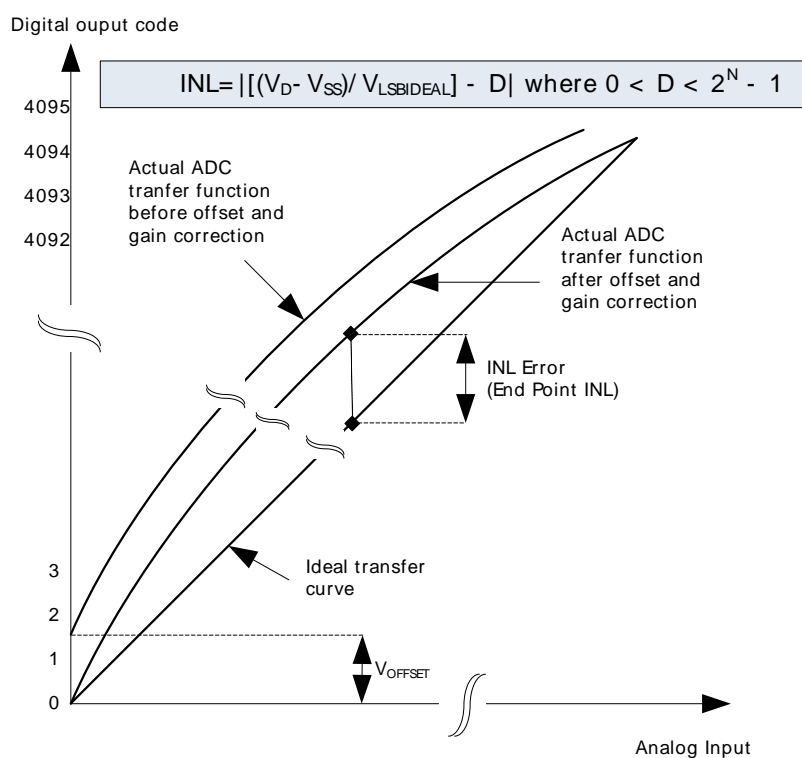
<sup>1</sup>On the average every ADC will have one missing code, most likely to appear around 2048 +/- n\*512 where n can be a value in the set {-3, -2, -1, 1, 2, 3}. There will be no missing code around 2048, and in spite of the missing code the ADC will be monotonic at all times so that a response to a slowly increasing input will always be a slowly increasing output. Around the one code that is missing, the neighbour codes will look wider in the DNL plot. The spectra will show spurs on the level of -78dBc for a full scale input for chips that have the missing code issue.

<sup>2</sup>Typical numbers given by  $\text{abs}(\text{Mean}) / (85 - 25)$ .

<sup>3</sup>Max number given by  $(\text{abs}(\text{Mean}) + 3 \times \text{stddev}) / (85 - 25)$ .

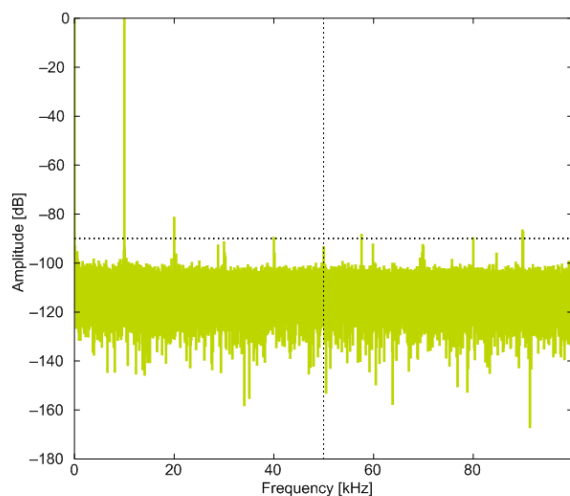
The integral non-linearity (INL) and differential non-linearity parameters are explained in Figure 3.17 (p. 32) and Figure 3.18 (p. 33) , respectively.

**Figure 3.17. Integral Non-Linearity (INL)**

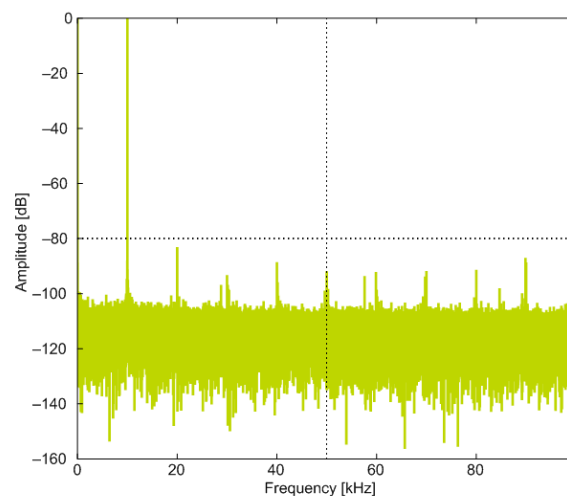


### 3.10.1 Typical performance

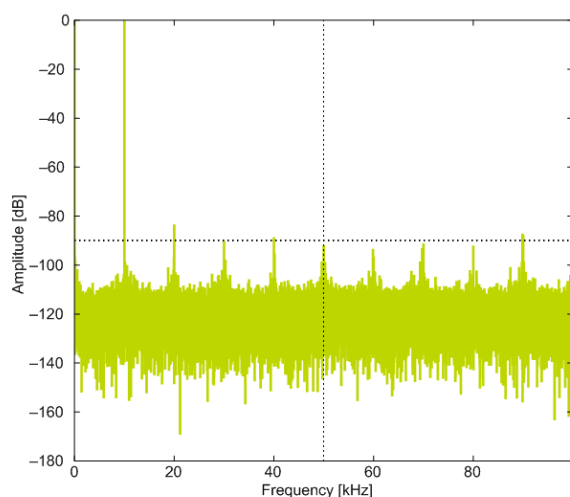
Figure 3.19. ADC Frequency Spectrum,  $V_{dd} = 3V$ , Temp = 25°C



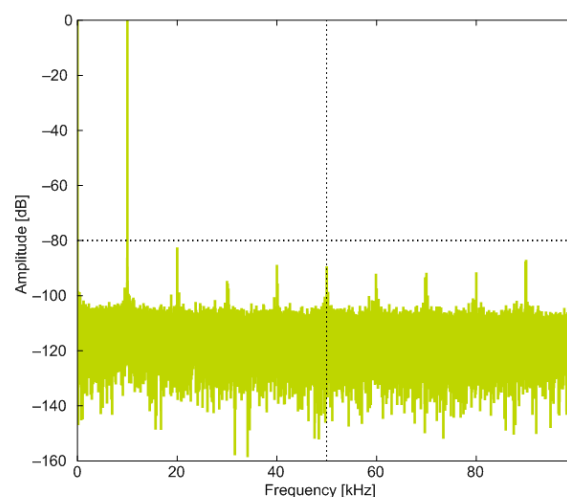
1.25V Reference



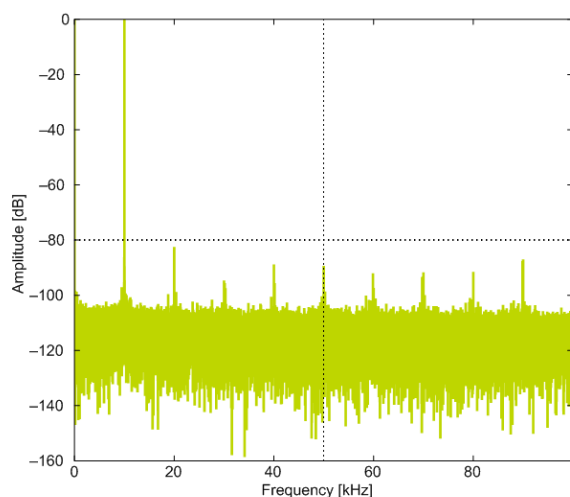
2.5V Reference



2XVDDVSS Reference



5VDIFF Reference



VDD Reference

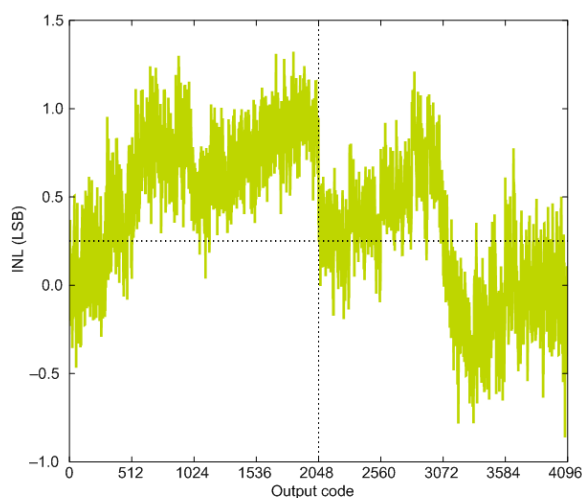
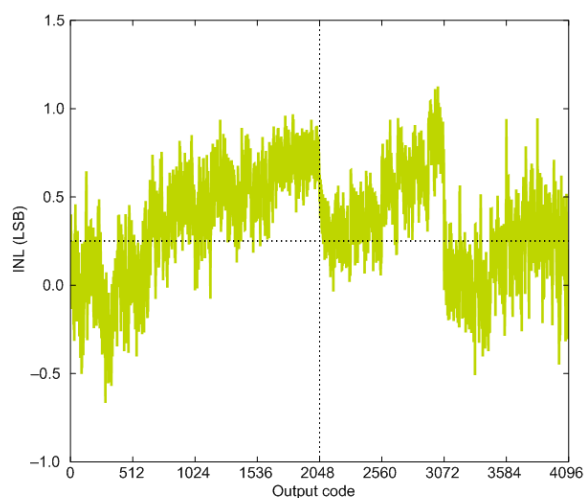
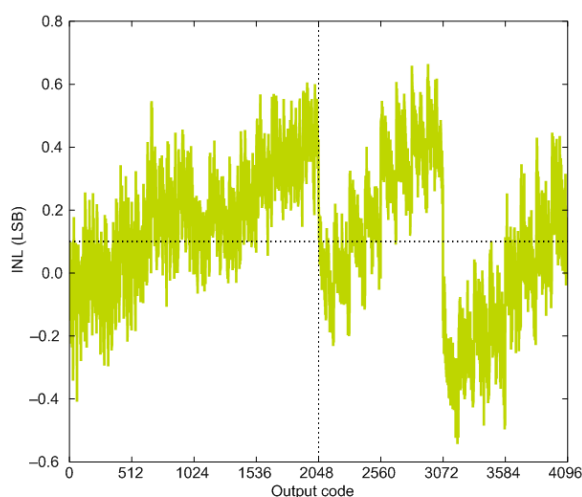
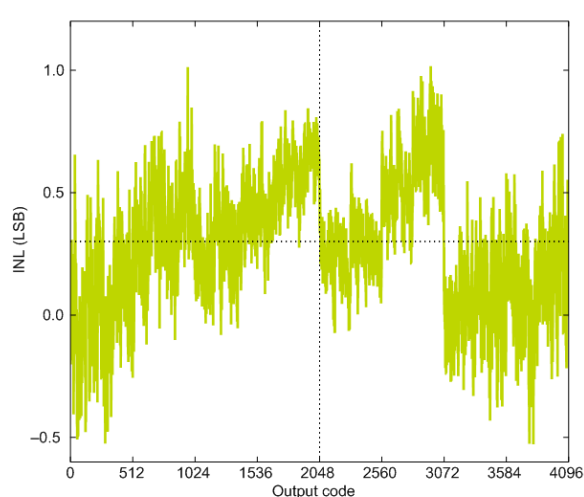
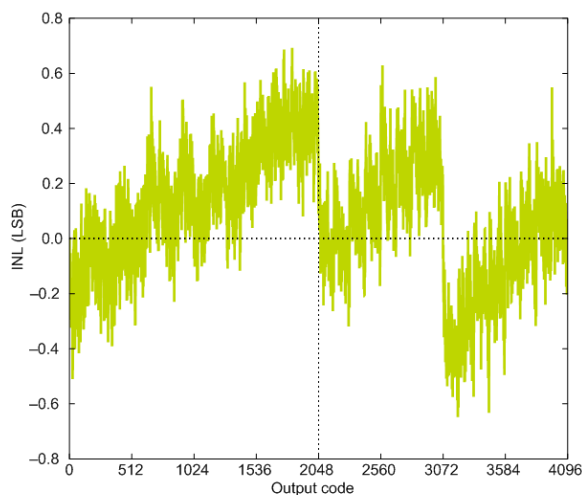
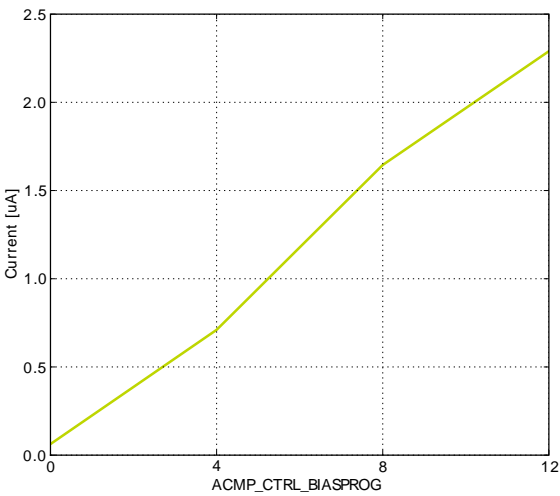
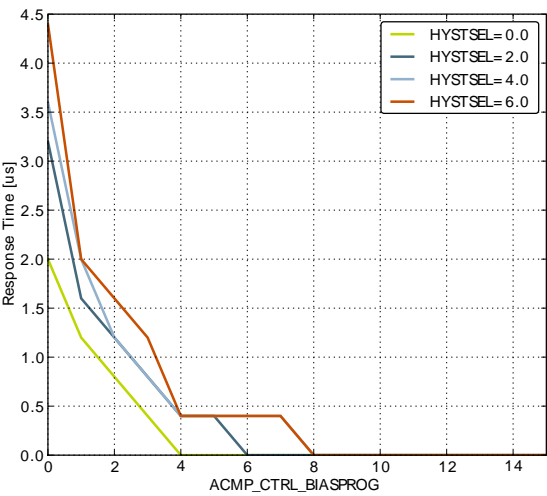
**Figure 3.20. ADC Integral Linearity Error vs Code, V<sub>dd</sub> = 3V, Temp = 25°C****1.25V Reference****2.5V Reference****2XVDDVSS Reference****5VDIFF Reference****VDD Reference**

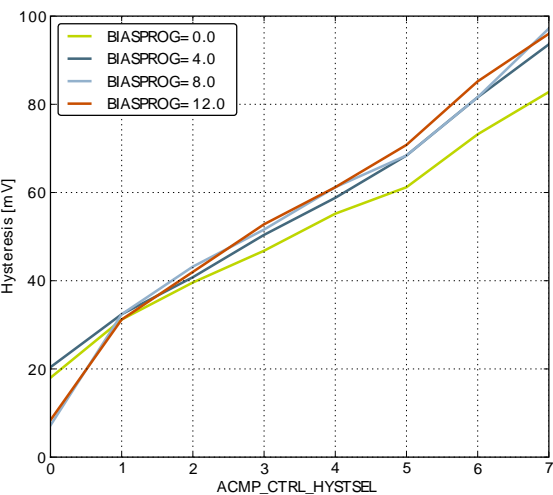
Figure 3.30. ACMP Characteristics, Vdd = 3V, Temp = 25°C, FULLBIAS = 0, HALFBIAS = 1



Current consumption, HYSTSEL = 4



Response time



Hysteresis

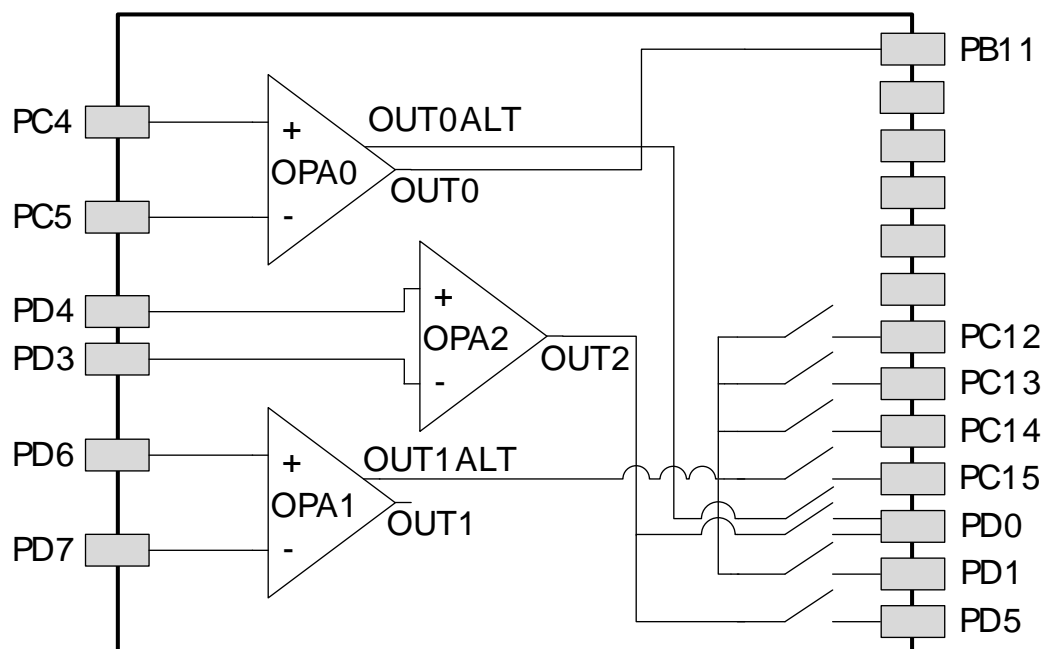
Alternate	LOCATION							
Functionality	0	1	2	3	4	5	6	Description
LCD_COM0	PE4							LCD driver common line number 0.
LCD_COM1	PE5							LCD driver common line number 1.
LCD_COM2	PE6							LCD driver common line number 2.
LCD_COM3	PE7							LCD driver common line number 3.
LCD_SEG0	PF2							LCD segment line 0. Segments 0, 1, 2 and 3 are controlled by SEGEN0.
LCD_SEG3	PF5							LCD segment line 3. Segments 0, 1, 2 and 3 are controlled by SEGEN0.
LCD_SEG4	PE8							LCD segment line 4. Segments 4, 5, 6 and 7 are controlled by SEGEN1.
LCD_SEG5	PE9							LCD segment line 5. Segments 4, 5, 6 and 7 are controlled by SEGEN1.
LCD_SEG6	PE10							LCD segment line 6. Segments 4, 5, 6 and 7 are controlled by SEGEN1.
LCD_SEG7	PE11							LCD segment line 7. Segments 4, 5, 6 and 7 are controlled by SEGEN1.
LCD_SEG8	PE12							LCD segment line 8. Segments 8, 9, 10 and 11 are controlled by SEGEN2.
LCD_SEG9	PE13							LCD segment line 9. Segments 8, 9, 10 and 11 are controlled by SEGEN2.
LCD_SEG10	PE14							LCD segment line 10. Segments 8, 9, 10 and 11 are controlled by SEGEN2.
LCD_SEG11	PE15							LCD segment line 11. Segments 8, 9, 10 and 11 are controlled by SEGEN2.
LCD_SEG13	PA0							LCD segment line 13. Segments 12, 13, 14 and 15 are controlled by SEGEN3.
LCD_SEG14	PA1							LCD segment line 14. Segments 12, 13, 14 and 15 are controlled by SEGEN3.
LCD_SEG15	PA2							LCD segment line 15. Segments 12, 13, 14 and 15 are controlled by SEGEN3.
LCD_SEG16	PA3							LCD segment line 16. Segments 16, 17, 18 and 19 are controlled by SEGEN4.
LCD_SEG17	PA4							LCD segment line 17. Segments 16, 17, 18 and 19 are controlled by SEGEN4.
LCD_SEG18	PA5							LCD segment line 18. Segments 16, 17, 18 and 19 are controlled by SEGEN4.
LCD_SEG20/ LCD_COM4	PB3							LCD segment line 20. Segments 20, 21, 22 and 23 are controlled by SEGEN5. This pin may also be used as LCD COM line 4
LCD_SEG21/ LCD_COM5	PB4							LCD segment line 21. Segments 20, 21, 22 and 23 are controlled by SEGEN5. This pin may also be used as LCD COM line 5
LCD_SEG22/ LCD_COM6	PB5							LCD segment line 22. Segments 20, 21, 22 and 23 are controlled by SEGEN5. This pin may also be used as LCD COM line 6
LCD_SEG23/ LCD_COM7	PB6							LCD segment line 23. Segments 20, 21, 22 and 23 are controlled by SEGEN5. This pin may also be used as LCD COM line 7
LES_ALTEX0	PD6							LESENSE alternate exite output 0.
LES_ALTEX1	PD7							LESENSE alternate exite output 1.
LES_ALTEX2	PA3							LESENSE alternate exite output 2.
LES_ALTEX3	PA4							LESENSE alternate exite output 3.
LES_ALTEX4	PA5							LESENSE alternate exite output 4.

**Table 4.3. GPIO Pinout**

Port	Pin 15	Pin 14	Pin 13	Pin 12	Pin 11	Pin 10	Pin 9	Pin 8	Pin 7	Pin 6	Pin 5	Pin 4	Pin 3	Pin 2	Pin 1	Pin 0
Port A	-	PA14	PA13	PA12	-	-	-	-	-	-	PA5	PA4	PA3	PA2	PA1	PA0
Port B	-	PB14	PB13	-	PB11	-	-	PB8	PB7	PB6	PB5	PB4	PB3	-	-	-
Port C	-	-	-	-	-	-	-	-	PC7	PC6	PC5	PC4	-	-	-	-
Port D	-	-	-	-	-	-	-	PD8	PD7	PD6	PD5	PD4	PD3	PD2	PD1	PD0
Port E	PE15	PE14	PE13	PE12	PE11	PE10	PE9	PE8	PE7	PE6	PE5	PE4	-	-	-	-
Port F	-	-	-	PF12	PF11	PF10	-	-	-	-	PF5	-	-	PF2	PF1	PF0

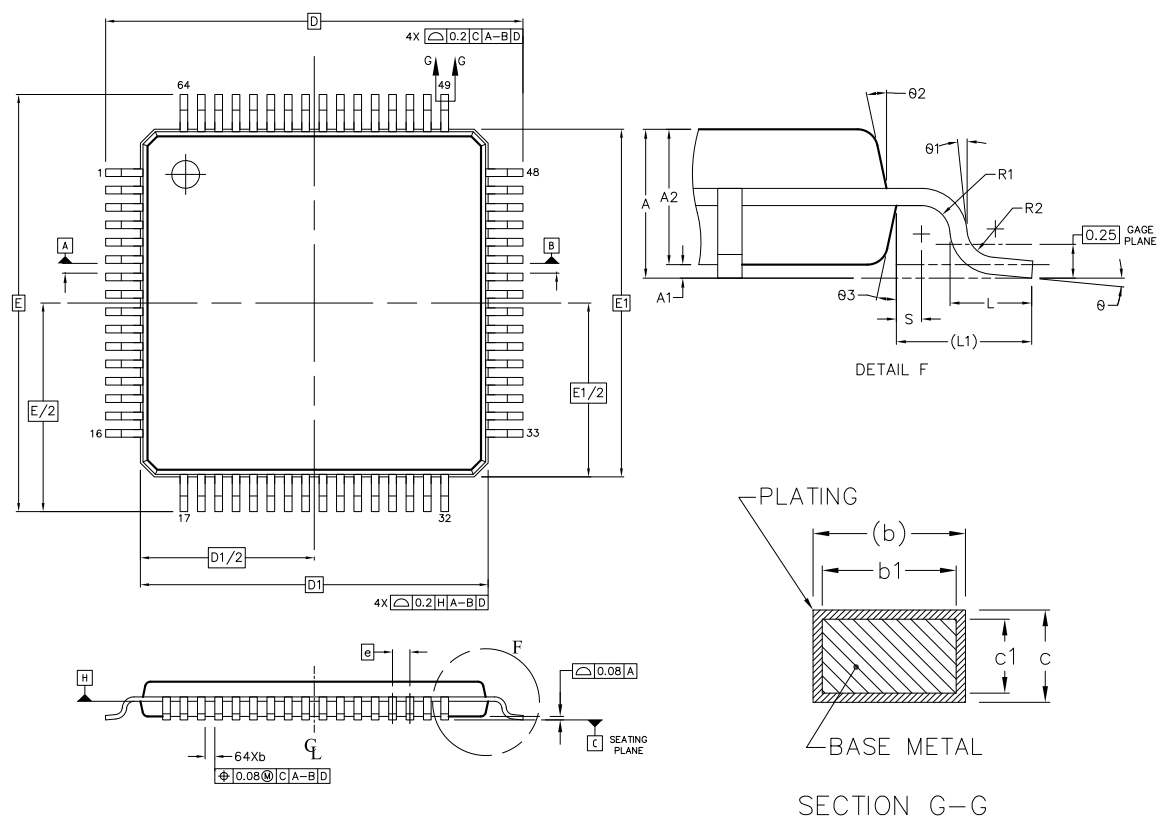
## 4.4 Opamp Pinout Overview

The specific opamp terminals available in *EFM32GG942* is shown in Figure 4.2 (p. 59) .

**Figure 4.2. Opamp Pinout**

## 4.5 TQFP64 Package

**Figure 4.3. TQFP64**



Rev: 98SP64023A\_X01\_17MAR2011

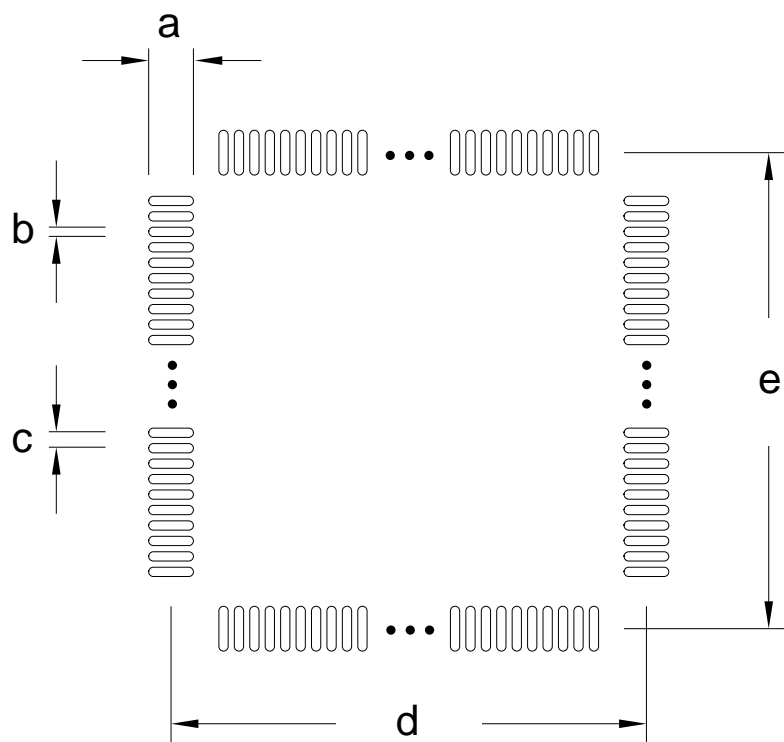
**Note:**

1. All dimensions & tolerancing confirm to ASME Y14.5M-1994.
2. The top package body size may be smaller than the bottom package body size.
3. Datum 'A,B', and 'B' to be determined at datum plane 'H'.
4. To be determined at seating place 'C'.
5. Dimension 'D1' and 'E1' do not include mold protrusions. Allowable protrusion is 0.25mm per side. 'D1' and 'E1' are maximum plastic body size dimension including mold mismatch. Dimension 'D1' and 'E1' shall be determined at datum plane 'H'.
6. Detail of Pin 1 indicatifier are option all but must be located within the zone indicated.
7. Dimension 'b' does not include dambar protrusion. Allowable dambar protrusion shall not cause the lead width to exceed the maximum 'b' dimension by more than 0.08 mm. Dambar can not be located on the lower radius or the foot. Minimum space between protrusion and an adjacent lead is 0.07 mm
8. Exact shape of each corner is optional.
9. These dimension apply to the flat section of the lead between 0.10 mm and 0.25 mm from the lead tip.
10. All dimensions are in millimeters.

**Table 4.4. QFP64 (Dimensions in mm)**

DIM	MIN	NOM	MAX	DIM	MIN	NOM	MAX
A	-	1.10	1.20	L1	-		
A1	0.05	-	0.15	R1	0.08	-	-
A2	0.95	1.00	1.05	R2	0.08	-	0.20



**Figure 5.2. TQFP64 PCB Solder Mask****Table 5.2. QFP64 PCB Solder Mask Dimensions (Dimensions in mm)**

Symbol	Dim. (mm)
a	1.72
b	0.42
c	0.50
d	11.50
e	11.50

## 7 Revision History

### 7.1 Revision 1.40

March 21st, 2016

Added clarification on conditions for  $INL_{ADC}$  and  $DNL_{ADC}$  parameters.

Reduced maximum and typical current consumption for all EM0 entries except 48 MHz in the Current Consumption table in the Electrical Characteristics section.

Increased maximum specifications for EM2 current, EM3 current, and EM4 current in the Current Consumption table in the Electrical Characteristics section.

Increased typical specification for EM2 and EM3 current at 85 C in the Current Consumption table in the Electrical Characteristics section.

Added EM2, EM3, and EM4 current consumption vs. temperature graphs.

Added a new EM2 entry and specified the existing specification is for EM0 for the BOD threshold on falling external supply voltage in the Power Management table in the Electrical Characteristics section.

Reduced maximum input leakage current in the GPIO table in the Electrical Characteristics section.

Added a maximum current consumption specification to the LFRCO table in the Electrical Characteristics section.

Added maximum specifications for the active current including references for two channels to the DAC table in the Electrical Characteristics section.

Increased the maximum specification for DAC offset voltage in the DAC table in the Electrical Characteristics section.

Increased the typical specifications for active current with  $FULLBIAS=1$  and capacitive sense internal resistance in the ACMP table in the Electrical Characteristics section.

Added minimum and maximum specifications and updated the typical value for the VCMP offset voltage in the VCMP table in the Electrical Characteristics section.

Removed the maximum specification and reduced the typical value for hysteresis in the VCMP table in the Electrical Characteristics section.

Updated all graphs in the Electrical Characteristics section to display data for 2.0 V as the minimum voltage.

### 7.2 Revision 1.30

May 23rd, 2014

Removed "preliminary" markings

Updated HFRCO figures.

Corrected single power supply voltage minimum value from 1.85V to 1.98V.

Updated Current Consumption information.

Updated Power Management information.

Updated power requirements in the Power Management section.

Removed minimum load capacitance figure and table. Added reference to application note.

Other minor corrections.

## 7.6 Revision 1.00

September 11th, 2012

Updated the HFRCO 1 MHz band typical value to 1.2 MHz.

Updated the HFRCO 7 MHz band typical value to 6.6 MHz.

Other minor corrections.

## 7.7 Revision 0.98

May 25th, 2012

Corrected EM3 current consumption in the Electrical Characteristics section.

## 7.8 Revision 0.96

February 28th, 2012

Added reference to errata document.

Corrected TQFP64 package drawing.

Updated PCB land pattern, solder mask and stencil design.

## 7.9 Revision 0.95

September 28th, 2011

Flash configuration for Giant Gecko is now 1024KB or 512KB. For flash sizes below 512KB, see the Leopard Gecko Family.

Corrected operating voltage from 1.8 V to 1.85 V.

Added rising POR level to Electrical Characteristics section.

Updated Minimum Load Capacitance ( $C_{LFXOL}$ ) Requirement For Safe Crystal Startup.

Added Gain error drift and Offset error drift to ADC table.

Added Opamp pinout overview.

Added reference to errata document.

Corrected TQFP64 package drawing.

Updated PCB land pattern, solder mask and stencil design.

# A Disclaimer and Trademarks

## A.1 Disclaimer

*Silicon Laboratories intends to provide customers with the latest, accurate, and in-depth documentation of all peripherals and modules available for system and software implementers using or intending to use the Silicon Laboratories products. Characterization data, available modules and peripherals, memory sizes and memory addresses refer to each specific device, and "Typical" parameters provided can and do vary in different applications. Application examples described herein are for illustrative purposes only. Silicon Laboratories reserves the right to make changes without further notice and limitation to product information, specifications, and descriptions herein, and does not give warranties as to the accuracy or completeness of the included information. Silicon Laboratories shall have no liability for the consequences of use of the information supplied herein. This document does not imply or express copyright licenses granted hereunder to design or fabricate any integrated circuits. The products must not be used within any Life Support System without the specific written consent of Silicon Laboratories. A "Life Support System" is any product or system intended to support or sustain life and/or health, which, if it fails, can be reasonably expected to result in significant personal injury or death. Silicon Laboratories products are generally not intended for military applications. Silicon Laboratories products shall under no circumstances be used in weapons of mass destruction including (but not limited to) nuclear, biological or chemical weapons, or missiles capable of delivering such weapons.*

## A.2 Trademark Information

Silicon Laboratories Inc., Silicon Laboratories, Silicon Labs, SiLabs and the Silicon Labs logo, CMEMS®, EFM, EFM32, EFR, Energy Micro, Energy Micro logo and combinations thereof, "the world's most energy friendly microcontrollers", Ember®, EZLink®, EZMac®, EZRadio®, EZRadioPRO®, DSPLL®, ISO-modem®, Precision32®, ProSLIC®, SiPHY®, USBXpress® and others are trademarks or registered trademarks of Silicon Laboratories Inc. ARM, CORTEX, Cortex-M3 and THUMB are trademarks or registered trademarks of ARM Holdings. Keil is a registered trademark of ARM Limited. All other products or brand names mentioned herein are trademarks of their respective holders.

## B Contact Information

**Silicon Laboratories Inc.**

400 West Cesar Chavez

Austin, TX 78701

Please visit the Silicon Labs Technical Support web page:

<http://www.silabs.com/support/pages/contacttechnicalsupport.aspx>

and register to submit a technical support request.