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Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

Details

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Product Status	Active
Core Processor	ARM® Cortex®-M3
Core Size	32-Bit Single-Core
Speed	48MHz
Connectivity	I ² C, IrDA, SmartCard, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, LCD, POR, PWM, WDT
Number of I/O	50
Program Memory Size	512KB (512K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	128K x 8
Voltage - Supply (Vcc/Vdd)	1.98V ~ 3.8V
Data Converters	A/D 8x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-TQFP
Supplier Device Package	64-TQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/silicon-labs/efm32gg942f512g-e-qfp64r

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2 System Summary

2.1 System Introduction

The EFM32 MCUs are the world's most energy friendly microcontrollers. With a unique combination of the powerful 32-bit ARM Cortex-M3, innovative low energy techniques, short wake-up time from energy saving modes, and a wide selection of peripherals, the EFM32GG microcontroller is well suited for any battery operated application as well as other systems requiring high performance and low-energy consumption. This section gives a short introduction to each of the modules in general terms and also shows a summary of the configuration for the EFM32GG942 devices. For a complete feature set and in-depth information on the modules, the reader is referred to the *EFM32GG Reference Manual*.

A block diagram of the EFM32GG942 is shown in Figure 2.1 (p. 3) .



Figure 2.1. Block Diagram

2.1.1 ARM Cortex-M3 Core

The ARM Cortex-M3 includes a 32-bit RISC processor which can achieve as much as 1.25 Dhrystone MIPS/MHz. A Memory Protection Unit with support for up to 8 memory segments is included, as well as a Wake-up Interrupt Controller handling interrupts triggered while the CPU is asleep. The EFM32 implementation of the Cortex-M3 is described in detail in *EFM32 Cortex-M3 Reference Manual*.

2.1.2 Debug Interface (DBG)

This device includes hardware debug support through a 2-pin serial-wire debug interface and an Embedded Trace Module (ETM) for data/instruction tracing. In addition there is also a 1-wire Serial Wire Viewer pin which can be used to output profiling information, data trace and software-generated messages.

3.9 Oscillators

3.9.1 LFXO

Table 3.8. LFXO

Symbol	Parameter	Condition	Min	Тур	Max	Unit
f _{LFXO}	Supported nominal crystal frequency			32.768		kHz
ESR _{LFXO}	Supported crystal equivalent series re- sistance (ESR)			30	120	kOhm
C _{LFXOL}	Supported crystal external load range		X ¹		25	pF
DC _{LFXO}	Duty cycle		48	50	53.5	%
I _{LFXO}	Current consump- tion for core and buffer after startup.	ESR=30 kOhm, C _L =10 pF, LFXOBOOST in CMU_CTRL is 1		190		nA
t _{LFXO}	Start- up time.	ESR=30 kOhm, C _L =10 pF, 40% - 60% duty cycle has been reached, LFXOBOOST in CMU_CTRL is 1		400		ms

¹See Minimum Load Capacitance (C_{LFXOL}) Requirement For Safe Crystal Startup in energyAware Designer in Simplicity Studio

For safe startup of a given crystal, the Configurator tool in Simplicity Studio contains a tool to help users configure both load capacitance and software settings for using the LFXO. For details regarding the crystal configuration, the reader is referred to application note "AN0016 EFM32 Oscillator Design Consideration".

3.9.2 HFXO

Table 3.9. HFXO

Symbol	Parameter	Condition	Min	Тур	Мах	Unit
f _{HFXO}	Supported nominal crystal Frequency		4		48	MHz
	Supported crystal	Crystal frequency 48 MHz			50	Ohm
ESR _{HFXO}	equivalent series re-	Crystal frequency 32 MHz		30	60	Ohm
	sistance (ESR)	Crystal frequency 4 MHz		400	1500	Ohm
9 _{mHFXO}	The transconduc- tance of the HFXO input transistor at crystal startup	HFXOBOOST in CMU_CTRL equals 0b11	20			mS
C _{HFXOL}	Supported crystal external load range		5		25	pF
	Current consump-	4 MHz: ESR=400 Ohm, C _L =20 pF, HFXOBOOST in CMU_CTRL equals 0b11		85		μA
HFX0	tion for HEXO after startup	32 MHz: ESR=30 Ohm, C _L =10 pF, HFXOBOOST in CMU_CTRL equals 0b11		165		μA
t _{HFXO}	Startup time	32 MHz: ESR=30 Ohm, C _L =10 pF, HFXOBOOST in CMU_CTRL equals 0b11		400		μs

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Symbol	Parameter	Condition	Min	Тур	Max	Unit
C _{ADCIN}	Input capacitance			2		pF
R _{ADCIN}	Input ON resistance		1			MOhm
R _{ADCFILT}	Input RC filter resis- tance			10		kOhm
C _{ADCFILT}	Input RC filter/de- coupling capaci- tance			fF		
f _{ADCCLK}	ADC Clock Fre- quency				13	MHz
		6 bit	7			ADC- CLK Cycles
t _{ADCCONV}	Conversion time	8 bit	11			ADC- CLK Cycles
		12 bit	13			ADC- CLK Cycles
t _{ADCACQ}	Acquisition time	Programmable	256	ADC- CLK Cycles		
t _{ADCACQVDD3}	Required acquisi- tion time for VDD/3 reference		2			μs
	Startup time of ref- erence generator and ADC core in NORMAL mode			5		μs
tadcstart	Startup time of ref- erence generator and ADC core in KEEPADCWARM mode			1		μs
		1 MSamples/s, 12 bit, single ended, internal 1.25V refer- ence		59		dB
		1 MSamples/s, 12 bit, single ended, internal 2.5V reference		63		dB
		1 MSamples/s, 12 bit, single ended, V _{DD} reference		65		dB
SNRADC	Signal to Noise Ra-	1 MSamples/s, 12 bit, differen- tial, internal 1.25V reference		60		dB
	10 (JNK)	1 MSamples/s, 12 bit, differen- tial, internal 2.5V reference		65		dB
		1 MSamples/s, 12 bit, differen- tial, 5V reference		54		dB
		1 MSamples/s, 12 bit, differential, V_{DD} reference		67		dB
		1 MSamples/s, 12 bit, differential, $2xV_{DD}$ reference		69		dB



Symbol	Parameter	Condition	Min	Тур	Max	Unit
		200 kSamples/s, 12 bit, differ- ential, 2xV _{DD} reference		69		dB
		1 MSamples/s, 12 bit, single ended, internal 1.25V refer- ence		64		dBc
		1 MSamples/s, 12 bit, single ended, internal 2.5V reference		76		dBc
		1 MSamples/s, 12 bit, single ended, V _{DD} reference		73		dBc
		1 MSamples/s, 12 bit, differen- tial, internal 1.25V reference		66		dBc
		1 MSamples/s, 12 bit, differen- tial, internal 2.5V reference		77		dBc
		1 MSamples/s, 12 bit, differen- tial, V _{DD} reference		76		dBc
		1 MSamples/s, 12 bit, differen- tial, 2xV _{DD} reference		75		dBc
SEDRADO	Spurious-Free Dy-	1 MSamples/s, 12 bit, differen- tial, 5V reference		69		dBc
SI DINADC	DR)	200 kSamples/s, 12 bit, sin- gle ended, internal 1.25V refer- ence		75		dBc
		200 kSamples/s, 12 bit, single ended, internal 2.5V reference		75		dBc
		200 kSamples/s, 12 bit, single ended, V _{DD} reference		76		dBc
		200 kSamples/s, 12 bit, differ- ential, internal 1.25V reference		79		dBc
		200 kSamples/s, 12 bit, differ- ential, internal 2.5V reference		79		dBc
		200 kSamples/s, 12 bit, differ- ential, 5V reference		78		dBc
		200 kSamples/s, 12 bit, differ- ential, V _{DD} reference	68	79		dBc
		200 kSamples/s, 12 bit, differ- ential, 2xV _{DD} reference		79		dBc
	Offset voltage	After calibration, single ended		0.3		mV
ADCOFFSET	Cliser voltage	After calibration, differential	-3	0.3	3	mV
				-1.92		mV/°C
TGRAD _{ADCTH}	Thermometer out- put gradient			-6.3		ADC Codes/ °C
DNL _{ADC}	Differential non-lin- earity (DNL)	V _{DD} = 3.0 V, external 2.5V reference	-1	±0.7	4	LSB
INL _{ADC}	Integral non-linear- ity (INL), End point method			±1.2	±3.0	LSB
MC _{ADC}	No missing codes		11.999 ¹	12		bits



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Symbol	Parameter	Condition	Min	Тур	Мах	Unit
CAIN	Gain orror drift	1.25V reference		0.01 ²	0.033 ³	%/°C
GAINED	Gain endrunnt	2.5V reference		0.01 ²	0.03 ³	%/°C
OFFOFT	Offset error drift	1.25V reference		0.2 ²	0.7 ³	LSB/°C
UFFSEIED		2.5V reference		0.2 ²	0.62 ³	LSB/°C

¹On the average every ADC will have one missing code, most likely to appear around 2048 +/- n*512 where n can be a value in the set {-3, -2, -1, 1, 2, 3}. There will be no missing code around 2048, and in spite of the missing code the ADC will be monotonic at all times so that a response to a slowly increasing input will always be a slowly increasing output. Around the one code that is missing, the neighbour codes will look wider in the DNL plot. The spectra will show spurs on the level of -78dBc for a full scale input for chips that have the missing code issue.

²Typical numbers given by abs(Mean) / (85 - 25).

³Max number given by (abs(Mean) + 3x stddev) / (85 - 25).

The integral non-linearity (INL) and differential non-linearity parameters are explained in Figure 3.17 (p. 32) and Figure 3.18 (p. 33), respectively.

Figure 3.17. Integral Non-Linearity (INL)





Figure 3.18. Differential Non-Linearity (DNL)



3.10.1 Typical performance

Figure 3.19. ADC Frequency Spectrum, Vdd = 3V, Temp = 25°C









Figure 3.22. ADC Absolute Offset, Common Mode = Vdd /2



Figure 3.23. ADC Dynamic Performance vs Temperature for all ADC References, Vdd = 3V





Figure 3.24. ADC Temperature sensor readout



3.11 Digital Analog Converter (DAC)

Table 3.15. DAC

Symbol	Parameter	Condition	Min	Тур	Max	Unit
M	Output voltage	VDD voltage reference, single ended	0		V _{DD}	V
V DACOUT	range	VDD voltage reference, differ- ential	-V _{DD}		V _{DD}	V
V _{DACCM}	Output common mode voltage range		0		V _{DD}	V
	Active current in-	500 kSamples/s, 12 bit		400 ¹	600 ¹	μA
I _{DAC}	cluding references	100 kSamples/s, 12 bit		200 ¹	260 ¹	μA
	for 2 channels	1 kSamples/s 12 bit NORMAL		17 ¹	25 ¹	μA
SR _{DAC}	Sample rate			500	ksam- ples/s	
	DAC clock frequen- cy	Continuous Mode			1000	kHz
f _{DAC}		Sample/Hold Mode			250	kHz
		Sample/Off Mode			250	kHz
CYC _{DACCONV}	Clock cyckles per conversion			2		
t _{DACCONV}	Conversion time		2			μs
t _{DACSETTLE}	Settling time			5		μs
		500 kSamples/s, 12 bit, sin- gle ended, internal 1.25V refer- ence		58		dB
SNR _{DAC}	Signal to Noise Ra- tio (SNR)	500 kSamples/s, 12 bit, single ended, internal 2.5V reference		59		dB
		500 kSamples/s, 12 bit, differ- ential, internal 1.25V reference		58		dB

Figure 3.32. SPI Slave Timing



Table 3.24. SPI Slave Timing

Symbol	Parameter	Min	Тур	Max	Unit
t _{SCLK_} sl ^{1 2}	SCKL period	2 * t _{HFPER-} CLK			ns
t _{SCLK_hi} ^{1 2}	SCLK high period	3 * t _{HFPER-} CLK			ns
t _{SCLK_lo} ^{1 2}	SCLK low period	3 * t _{HFPER-} CLK			ns
t _{CS_ACT_MI} ¹²	CS active to MISO	4.00		30.00	ns
t _{CS_DIS_MI} ¹²	CS disable to MISO	4.00		30.00	ns
t _{SU_MO} ¹²	MOSI setup time	4.00			ns
t _{H_MO} ^{1 2}	MOSI hold time	2 + 2* t _{HF-} PERCLK			ns
t _{SCLK_MI} ¹²	SCLK to MISO	9 + t _{HFPER-} CLK		36 + 2*t _{HF-} PERCLK	ns

¹Applies for both CLKPHA = 0 and CLKPHA = 1 (figure only shows CLKPHA = 0)

 $^2\text{Measurement}$ done at 10% and 90% of V_{DD} (figure shows 50% of $\text{V}_{\text{DD}})$

3.18 USB

The USB hardware in the EFM32GG942 passes all tests for USB 2.0 Full Speed certification. See the test-report distributed with application note "AN0046 - USB Hardware Design Guide".

3.19 Digital Peripherals

Table 3.25. Digital Peripherals

Symbol	Parameter	Condition	Min	Тур	Мах	Unit
I _{USART}	USART current	USART idle current, clock en- abled		4.9		μΑ/ MHz
I _{UART}	UART current	UART idle current, clock en- abled		μΑ/ MHz		
I _{LEUART}	LEUART current	LEUART idle current, clock en- abled		140		nA
I _{I2C}	I2C current	I2C idle current, clock enabled		6.1		μΑ/ MHz

4 Pinout and Package

Note

Please refer to the application note "AN0002 EFM32 Hardware Design Considerations" for guidelines on designing Printed Circuit Boards (PCB's) for the EFM32GG942.

4.1 Pinout

The *EFM32GG942* pinout is shown in Figure 4.1 (p. 51) and Table 4.1 (p. 51). Alternate locations are denoted by "#" followed by the location number (Multiple locations on the same pin are split with "/"). Alternate locations can be configured in the LOCATION bitfield in the *_ROUTE register in the module in question.

Figure 4.1. EFM32GG942 Pinout (top view, not to scale)



Table 4.1. Device Pinout

	QFP64 Pin# and Name				
Pin #	Pin Name	Analog	Timers	Communication	Other
1	PA0	LCD_SEG13	TIM0_CC0 #0/1/4	I2C0_SDA #0 LEU0_RX #4	PRS_CH0 #0 GPIO_EM4WU0
2	PA1	LCD_SEG14	TIM0_CC1 #0/1	I2C0_SCL #0	CMU_CLK1 #0 PRS_CH1 #0
3	PA2	LCD_SEG15	TIM0_CC2 #0/1		CMU_CLK0 #0

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Alternate		LOCATION						
Functionality	0	1	2	3	4	5	6	Description
LCD_COM0	PE4							LCD driver common line number 0.
LCD_COM1	PE5							LCD driver common line number 1.
LCD_COM2	PE6							LCD driver common line number 2.
LCD_COM3	PE7							LCD driver common line number 3.
LCD_SEG0	PF2							LCD segment line 0. Segments 0, 1, 2 and 3 are con- trolled by SEGEN0.
LCD_SEG3	PF5							LCD segment line 3. Segments 0, 1, 2 and 3 are con- trolled by SEGEN0.
LCD_SEG4	PE8							LCD segment line 4. Segments 4, 5, 6 and 7 are con- trolled by SEGEN1.
LCD_SEG5	PE9							LCD segment line 5. Segments 4, 5, 6 and 7 are con- trolled by SEGEN1.
LCD_SEG6	PE10							LCD segment line 6. Segments 4, 5, 6 and 7 are con- trolled by SEGEN1.
LCD_SEG7	PE11							LCD segment line 7. Segments 4, 5, 6 and 7 are con- trolled by SEGEN1.
LCD_SEG8	PE12							LCD segment line 8. Segments 8, 9, 10 and 11 are con- trolled by SEGEN2.
LCD_SEG9	PE13							LCD segment line 9. Segments 8, 9, 10 and 11 are con- trolled by SEGEN2.
LCD_SEG10	PE14							LCD segment line 10. Segments 8, 9, 10 and 11 are con- trolled by SEGEN2.
LCD_SEG11	PE15							LCD segment line 11. Segments 8, 9, 10 and 11 are con- trolled by SEGEN2.
LCD_SEG13	PA0							LCD segment line 13. Segments 12, 13, 14 and 15 are controlled by SEGEN3.
LCD_SEG14	PA1							LCD segment line 14. Segments 12, 13, 14 and 15 are controlled by SEGEN3.
LCD_SEG15	PA2							LCD segment line 15. Segments 12, 13, 14 and 15 are controlled by SEGEN3.
LCD_SEG16	PA3							LCD segment line 16. Segments 16, 17, 18 and 19 are controlled by SEGEN4.
LCD_SEG17	PA4							LCD segment line 17. Segments 16, 17, 18 and 19 are controlled by SEGEN4.
LCD_SEG18	PA5							LCD segment line 18. Segments 16, 17, 18 and 19 are controlled by SEGEN4.
LCD_SEG20/ LCD_COM4	PB3							LCD segment line 20. Segments 20, 21, 22 and 23 are controlled by SEGEN5. This pin may also be used as LCD COM line 4
LCD_SEG21/ LCD_COM5	PB4							LCD segment line 21. Segments 20, 21, 22 and 23 are controlled by SEGEN5. This pin may also be used as LCD COM line 5
LCD_SEG22/ LCD_COM6	PB5							LCD segment line 22. Segments 20, 21, 22 and 23 are controlled by SEGEN5. This pin may also be used as LCD COM line 6
LCD_SEG23/ LCD_COM7	PB6							LCD segment line 23. Segments 20, 21, 22 and 23 are controlled by SEGEN5. This pin may also be used as LCD COM line 7
LES_ALTEX0	PD6							LESENSE alternate exite output 0.
LES_ALTEX1	PD7							LESENSE alternate exite output 1.
LES_ALTEX2	PA3							LESENSE alternate exite output 2.
LES_ALTEX3	PA4							LESENSE alternate exite output 3.
LES_ALTEX4	PA5							LESENSE alternate exite output 4.



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Alternate			LOC					
Functionality	0	1	2	3	4	5	6	Description
US0_CS	PE13	PE4			PB14	PB14		USART0 chip select input / output.
								USART0 Asynchronous Receive.
US0_RX	PE11	PE6		PE12	PB8			USART0 Synchronous mode Master Input / Slave Output (MISO).
US0_TX	PE10	PE7		PE13	PB7			USART0 Asynchronous Transmit.Also used as receive in- put in half duplex communication. USART0 Synchronous mode Master Output / Slave Input (MOSI).
US1_CLK	PB7	PD2	PF0					USART1 clock input / output.
US1_CS	PB8	PD3	PF1					USART1 chip select input / output.
								USART1 Asynchronous Receive.
US1_RX		PD1	PD6					USART1 Synchronous mode Master Input / Slave Output (MISO).
US1 TX		PD0	PD7					USART1 Asynchronous Transmit.Also used as receive in- put in half duplex communication.
								USART1 Synchronous mode Master Output / Slave Input (MOSI).
US2_CLK	PC4	PB5						USART2 clock input / output.
US2_CS	PC5	PB6						USART2 chip select input / output.
US2_RX		PB4						USART2 Asynchronous Receive. USART2 Synchronous mode Master Input / Slave Output (MISO).
US2_TX		PB3						USART2 Asynchronous Transmit.Also used as receive in- put in half duplex communication. USART2 Synchronous mode Master Output / Slave Input
								(MOSI).
USB_DM	PF10							USB D- pin.
USB_DMPU	PD2							USB D- Pullup control.
USB_DP	PF11							USB D+ pin.
USB_ID	PF12							USB ID pin. Used in OTG mode.
USB_VBUS	USB_VBUS							USB 5 V VBUS input.
USB_VBUSEN	PF5							USB 5 V VBUS enable.
USB_VREGI	USB_VREGI							USB Input to internal 3.3 V regulator
USB_VREGO	USB_VREGO							USB Decoupling for internal 3.3 V USB regulator and reg- ulator output

4.3 GPIO Pinout Overview

The specific GPIO pins available in *EFM32GG942* is shown in Table 4.3 (p. 59). Each GPIO port is organized as 16-bit ports indicated by letters A through F, and the individual pin on this port is indicated by a number from 15 down to 0.

4.5 TQFP64 Package

Figure 4.3. TQFP64



Note:

- 1. All dimensions & tolerancing confirm to ASME Y14.5M-1994.
- 2. The top package body size may be smaller than the bottom package body size.
- 3. Datum 'A,B', and 'B' to be determined at datum plane 'H'.
- 4. To be determined at seating place 'C'.
- 5. Dimension 'D1' and 'E1' do not include mold protrusions. Allowable protrusion is 0.25mm per side. 'D1' and 'E1' are maximum plastic body size dimension including mold mismatch. Dimension 'D1' and 'E1' shall be determined at datum plane 'H'.
- 6. Detail of Pin 1 indicatifier are option all but must be located within the zone indicated.
- 7. Dimension 'b' does not include dambar protrusion. Allowable dambar protrusion shall not cause the lead width to exceed the maximum 'b' dimension by more than 0.08 mm. Dambar can not be located on the lower radius or the foot. Minimum space between protrusion and an adjacent lead is 0.07 mm
- 8. Exact shape of each corner is optional.
- 9. These dimension apply to the flat section of the lead between 0.10 mm and 0.25 mm from the lead tip. 10All dimensions are in millimeters.

DIM	MIN	NOM	MAX	DIM	MIN	NOM	MAX
A	-	1.10	1.20	L1		-	
A1	0.05	-	0.15	R1	0.08	-	-
A2	0.95	1.00	1.05	R2	0.08	-	0.20

Table 4.4. QFP64 (Dimensions in mm)

DIM	MIN	NOM	MAX	DIM	MIN	NOM	MAX
b	0.17	0.22	0.27	S	0.20	-	-
b1	0.17	0.20	0.23	θ	0°	3.5°	7°
с	0.09	-	0.20	θ1	0°	-	-
C1	0.09	-	0.16	θ2	11°	12°	13°
D	12.0 BSC			θ3	11°	12°	13°
D1		10.0 BSC					
е		0.50 BSC					
E	12.0 BSC						
E1	10.0 BSC						
L	0.45	0.60	0.75				

The TQFP64 Package is 10 by 10 mm in size and has a 0.5 mm pin pitch.

The TQFP64 Package uses Nickel-Palladium-Gold preplated leadframe.

All EFM32 packages are RoHS compliant and free of Bromine (Br) and Antimony (Sb).

For additional Quality and Environmental information, please see: http://www.silabs.com/support/quality/pages/default.aspx

5 PCB Layout and Soldering

5.1 Recommended PCB Layout

Figure 5.1. TQFP64 PCB Land Pattern



Table 5.1. QFP64 PCB Land Pattern Dimensions (Dimensions in mm)

Symbol	Dim. (mm)	Symbol	Pin number	Symbol	Pin number
а	1.60	P1	1	P6	48
b	0.30	P2	16	P7	49
с	0.50	P3	17	P8	64
d	11.50	P4	32	-	-
е	11.50	P5	33	-	-

Updated power requirements in the Power Management section.

Removed minimum load capacitance figure and table. Added reference to application note.

Other minor corrections.

7.6 Revision 1.00

September 11th, 2012

Updated the HFRCO 1 MHz band typical value to 1.2 MHz.

Updated the HFRCO 7 MHz band typical value to 6.6 MHz.

Other minor corrections.

7.7 Revision 0.98

May 25th, 2012

Corrected EM3 current consumption in the Electrical Characteristics section.

7.8 Revision 0.96

February 28th, 2012

Added reference to errata document.

Corrected TQFP64 package drawing.

Updated PCB land pattern, solder mask and stencil design.

7.9 Revision 0.95

September 28th, 2011

Flash configuration for Giant Gecko is now 1024KB or 512KB. For flash sizes below 512KB, see the Leopard Gecko Family.

Corrected operating voltage from 1.8 V to 1.85 V.

Added rising POR level to Electrical Characteristics section.

Updated Minimum Load Capacitance (C_{LFXOL}) Requirement For Safe Crystal Startup.

Added Gain error drift and Offset error drift to ADC table.

Added Opamp pinout overview.

Added reference to errata document.

Corrected TQFP64 package drawing.

Updated PCB land pattern, solder mask and stencil design.

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5.3. QFP64 PCB Stencil Design Dimensions (Dimensions in mm)	64



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