Welcome to E-XFL.COM

Understanding Embedded - CPLDs (Complex Programmable Logic Devices)

Embedded - CPLDs, or Complex Programmable Logic Devices, are highly versatile digital logic devices used in electronic systems. These programmable components are designed to perform complex logical operations and can be customized for specific applications. Unlike fixed-function ICs, CPLDs offer the flexibility to reprogram their configuration, making them an ideal choice for various embedded systems. They consist of a set of logic gates and programmable interconnects, allowing designers to implement complex logic circuits without needing custom hardware.

Applications of Embedded - CPLDs

Details	
Product Status	Obsolete
Programmable Type	EE PLD
Delay Time tpd(1) Max	15 ns
Voltage Supply - Internal	3V ~ 3.6V
Number of Logic Elements/Blocks	-
Number of Macrocells	8
Number of Gates	-
Number of I/O	-
Operating Temperature	0°C ~ 75°C (TA)
Mounting Type	Surface Mount
Package / Case	20-LCC (J-Lead)
Supplier Device Package	20-PLCC (9x9)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/gal16lv8c-15ljn

GAL16LV8

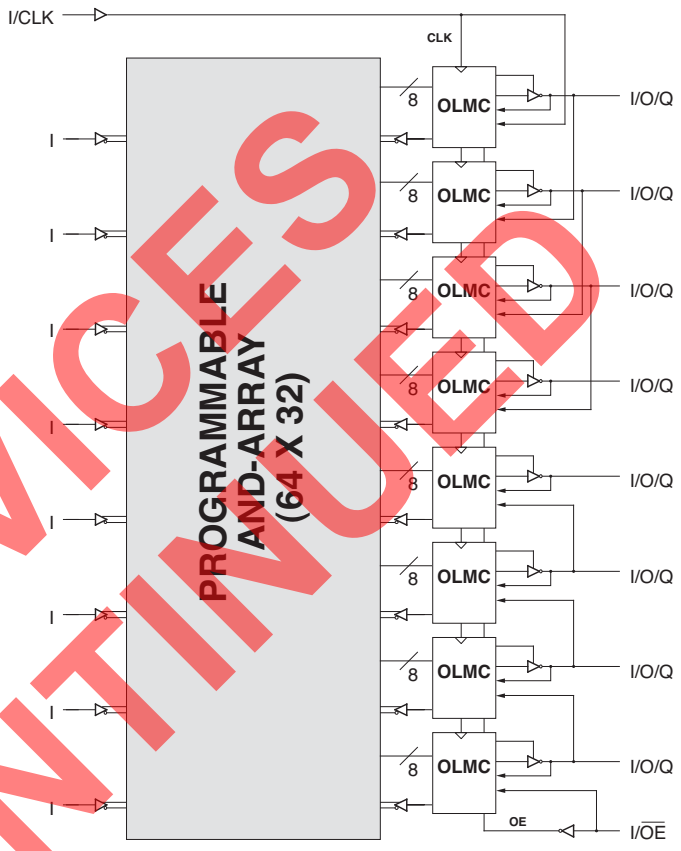
Low Voltage E²CMOS PLD Generic Array Logic™

Lead-Free Package Options Available!

Features

- **HIGH PERFORMANCE E²CMOS® TECHNOLOGY**
  - — 3.5 ns Maximum Propagation Delay
  - — Fmax = 250 MHz
  - — 2.5 ns Maximum from Clock Input to Data Output
  - — UltraMOS® Advanced CMOS Technology
- **3.3V LOW VOLTAGE 16V8 ARCHITECTURE**
  - — JEDEC-Compatible 3.3V Interface Standard
  - — 5V Compatible Inputs
  - — I/O Interfaces with Standard 5V TTL Devices (GAL16LV8C)
- **ACTIVE PULL-UPS ON ALL PINS (GAL16LV8D Only)**
- **E² CELL TECHNOLOGY**
  - — Reconfigurable Logic
  - — Reprogrammable Cells
  - — 100% Tested/100% Yields
  - — High Speed Electrical Erasure (<100ms)
  - — 20 Year Data Retention
- **EIGHT OUTPUT LOGIC MACROCELLS**
  - — Maximum Flexibility for Complex Logic Designs
  - — Programmable Output Polarity
- **PRELOAD AND POWER-ON RESET OF ALL REGISTERS**
  - — 100% Functional Testability
- **APPLICATIONS INCLUDE:**
  - — Glue Logic for 3.3V Systems
  - — DMA Control
  - — State Machine Control
  - — High Speed Graphics Processing
  - — Standard Logic Speed Upgrade
- **ELECTRONIC SIGNATURE FOR IDENTIFICATION**
- **LEAD-FREE PACKAGE OPTIONS**

Functional Block Diagram



Description

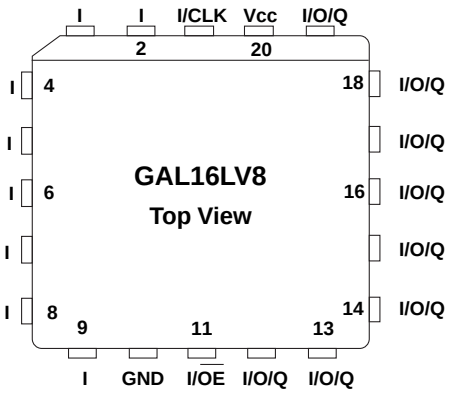
The GAL16LV8D, at 3.5 ns maximum propagation delay time, provides the highest speed performance available in the PLD market. The GAL16LV8C can interface with both 3.3V and 5V signal levels. The GAL16LV8 is manufactured using Lattice Semiconductor's advanced 3.3V E²CMOS process, which combines CMOS with Electrically Erasable (E²) floating gate technology. High speed erase times (<100ms) allow the devices to be reprogrammed quickly and efficiently.

The 3.3V GAL16LV8 uses the same industry standard 16V8 architecture as its 5V counterpart and supports all architectural features such as combinatorial or registered macrocell operations.

Unique test circuitry and reprogrammable cells allow complete AC, DC, and functional testing during manufacture. As a result, Lattice Semiconductor delivers 100% field programmability and functionality of all GAL products. In addition, 100 erase/write cycles and data retention in excess of 20 years are specified.

Pin Configuration

PLCC



LATTICE SEMICONDUCTOR CORP., 5555 Northeast Moore Ct., Hillsboro, Oregon 97124, U.S.A.
Tel. (503) 268-8000; 1-800-LATTICE; FAX (503) 268-8556; http://www.latticesemi.com

August 2004

GAL16LV8 Ordering Information

Conventional Packaging
Commercial Grade Specifications

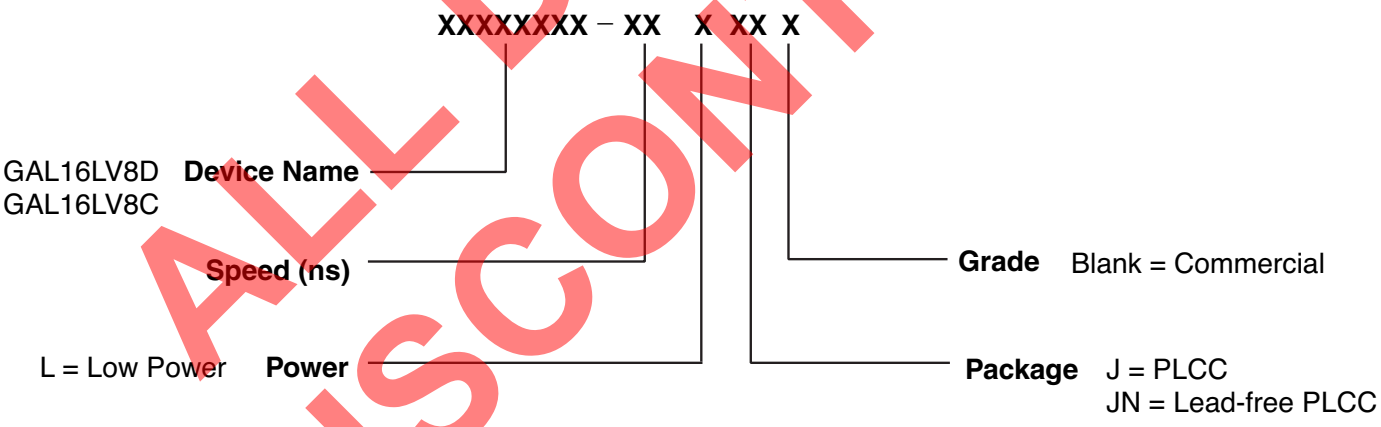
Tpd (ns)	Tsu (ns)	Tco (ns)	Icc (mA)	Ordering #	Package
3.5	3	2.5	70	GAL16LV8D-3LJ	20-Lead PLCC
5	4	3	70	GAL16LV8D-5LJ	20-Lead PLCC
7.5	6	5	65	GAL16LV8C-7LJ[1]	20-Lead PLCC
10	7	7	65	GAL16LV8C-10LJ	20-Lead PLCC
15	12	10	65	GAL16LV8C-15LJ	20-Lead PLCC

Lead-Free Packaging
Commercial Grade Specifications

Tpd (ns)	Tsu (ns)	Tco (ns)	Icc (mA)	Ordering #	Package
3.5	3	2.5	70	GAL16LV8D-3LJN	Lead-Free 20-Lead PLCC
5	4	3	70	GAL16LV8D-5LJN	Lead-Free 20-Lead PLCC
7.5	6	5	65	GAL16LV8C-7LJN[1]	Lead-Free 20-Lead PLCC
10	7	7	65	GAL16LV8C-10LJN	Lead-Free 20-Lead PLCC
15	12	10	65	GAL16LV8C-15LJN	Lead-Free 20-Lead PLCC

1. Discontinued per PCN #06-07. Contact Rochester Electronics for available inventory.

Part Number Description



Output Logic Macrocell (OLMC)

The following discussion pertains to configuring the output logic macrocell. It should be noted that actual implementation is accomplished by development software/hardware and is completely transparent to the user.

There are three global OLMC configuration modes possible: **simple**, **complex**, and **registered**. Details of each of these modes are illustrated in the following pages. Two global bits, SYN and AC0, control the mode configuration for all macrocells. The XOR bit of each macrocell controls the polarity of the output in any of the three modes, while the AC1 bit of each of the macrocells controls the input/output configuration. These two global and 16 individual architecture bits define all possible configurations in a GAL16LV8. The information given on these architecture bits is only to give a better understanding of the device. Compiler software will transparently set these architecture bits from the pin definitions, so the user should not need to directly manipulate these architecture bits.

The following is a list of the PAL architectures that the GAL16LV8 can emulate. It also shows the OLMC mode under which the GAL16LV8 emulates the PAL architecture.

PAL Architectures Emulated by GAL16LV8	GAL16LV8 Global OLMC Mode
16R8	Registered
16R6	Registered
16R4	Registered
16RP8	Registered
16RP6	Registered
16RP4	Registered
16L8	Complex
16H8	Complex
16P8	Complex
10L8	Simple
12L6	Simple
14L4	Simple
16L2	Simple
10H8	Simple
12H6	Simple
14H4	Simple
16H2	Simple
10P8	Simple
12P6	Simple
14P4	Simple
16P2	Simple

Compiler Support for OLMC

Software compilers support the three different global OLMC modes as different device types. These device types are listed in the table below. Most compilers have the ability to automatically select the device type, generally based on the register usage and output enable (OE) usage. Register usage on the device forces the software to choose the registered mode. All combinatorial outputs with OE controlled by the product term will force the software to choose the complex mode. The software will choose the simple mode only when all outputs are dedicated combinatorial without OE control. The different device types listed in the table can be used to override the automatic device selection by the software. For further details, refer to the compiler software manuals.

When using compiler software to configure the device, the user must pay special attention to the following restrictions in each mode. In **registered mode** pin 1 and pin 11 are permanently configured as clock and output enable, respectively. These pins cannot be configured as dedicated inputs in the registered mode.

In **complex mode** pin 1 and pin 11 become dedicated inputs and use the feedback paths of pin 19 and pin 12 respectively. Because of this feedback path usage, pin 19 and pin 12 do not have the feedback option in this mode.

In **simple mode** all feedback paths of the output pins are routed via the adjacent pins. In doing so, the two inner most pins (pins 15 and 16) will not have the feedback option as these pins are always configured as dedicated combinatorial output.

	Registered	Complex	Simple	Auto Mode Select
ABEL	P16V8R	P16V8C	P16V8AS	P16V8
CUPL	G16V8MS	G16V8MA	G16V8AS	G16V8
LOG/iC	GAL16V8_R	GAL16V8_C7	GAL16V8_C8	GAL16V8
OrCAD-PLD	"Registered"[1]	"Complex"[1]	"Simple"[1]	GAL16V8A
PLDesigner	P16V8R[2]	P16V8C[2]	P16V8C[2]	P16V8A
TANGO-PLD	G16V8R	G16V8C	G16V8AS[3]	G16V8

1) Used with **Configuration** keyword.
2) Prior to Version 2.0 support.
3) Supported on Version 1.20 or later.

Registered Mode

In the Registered mode, macrocells are configured as dedicated registered outputs or as I/O functions.

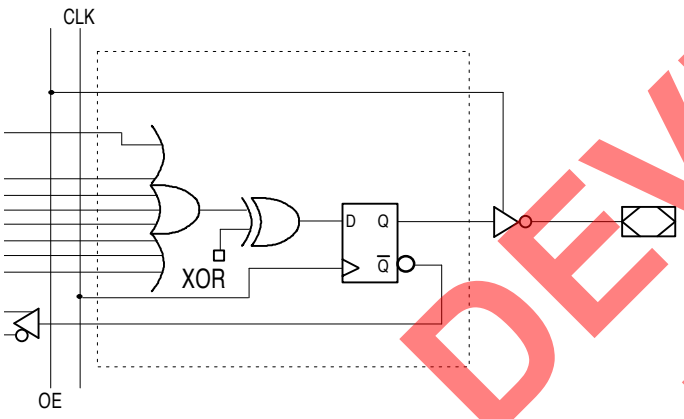
Architecture configurations available in this mode are similar to the common 16R8 and 16RP4 devices with various permutations of polarity, I/O and register placement.

All registered macrocells share common clock and output enable control pins. Any macrocell can be configured as registered or I/O. Up to eight registers or up to eight I/Os are possible in this mode.

Dedicated input or output functions can be implemented as subsets of the I/O function.

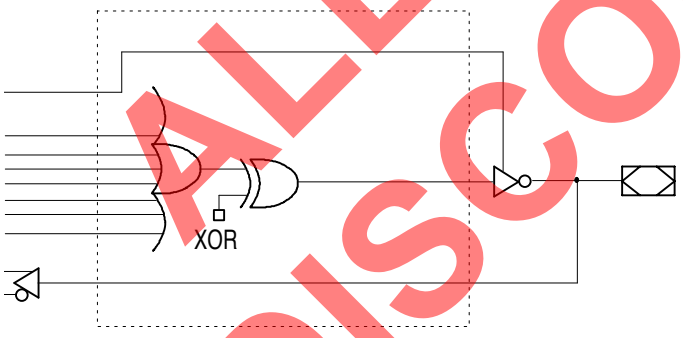
Registered outputs have eight product terms per output. I/Os have seven product terms per output.

The JEDEC fuse numbers, including the User Electronic Signature (UES) fuses and the Product Term Disable (PTD) fuses, are shown on the logic diagram on the following page.



Registered Configuration for Registered Mode

- SYN=0.
- AC0=1.
- XOR=0 defines Active Low Output.
- XOR=1 defines Active High Output.
- AC1=0 defines this output configuration.
- Pin 1 controls common CLK for the registered outputs.
- Pin 11 controls common $\overline{OE}$ for the registered outputs.
- Pin 1 & Pin 11 are permanently configured as CLK & $\overline{OE}$ for registered output configuration.



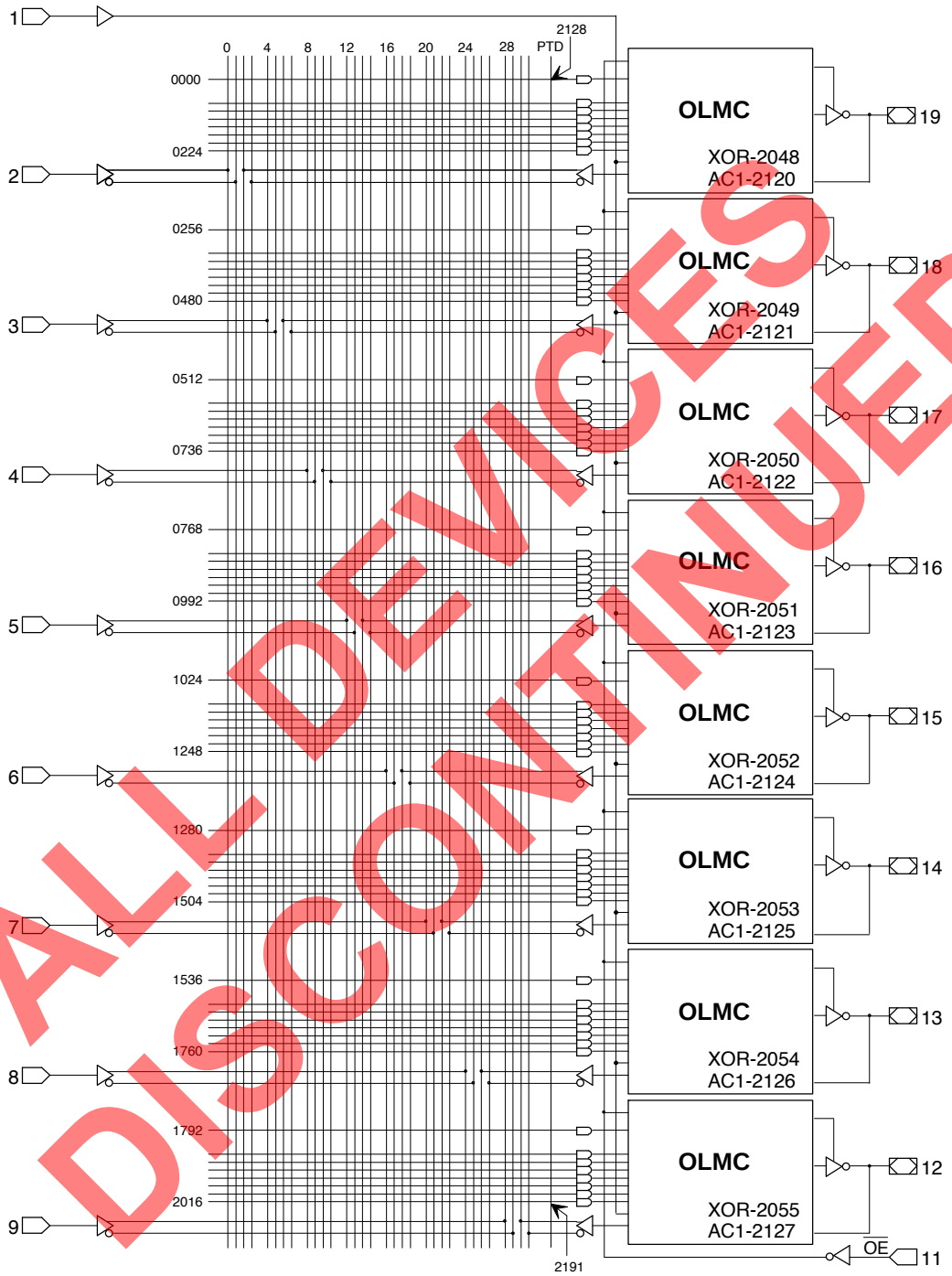
Combinatorial Configuration for Registered Mode

- SYN=0.
- AC0=1.
- XOR=0 defines Active Low Output.
- XOR=1 defines Active High Output.
- AC1=1 defines this output configuration.
- Pin 1 & Pin 11 are permanently configured as CLK & $\overline{OE}$ for registered output configuration.

Note: The development software configures all of the architecture control bits and checks for proper pin usage automatically.

Registered Mode Logic Diagram

PLCC Package Pinout



64-USER ELECTRONIC SIGNATURE FUSES

2056, 2057, ...	.... 2118, 2119
Byte 7	Byte 6 .... Byte 1	Byte 0

MSB LSB

SYN-2192
AC0-2193

Complex Mode

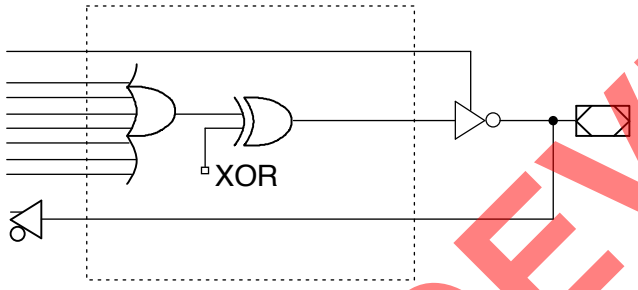
In the Complex mode, macrocells are configured as output only or I/O functions.

Architecture configurations available in this mode are similar to the common 16L8 and 16P8 devices with programmable polarity in each macrocell.

Up to six I/Os are possible in this mode. Dedicated inputs or outputs can be implemented as subsets of the I/O function. The two outer most macrocells (pins 12 & 19) do not have input capability. Designs requiring eight I/Os can be implemented in the Registered mode.

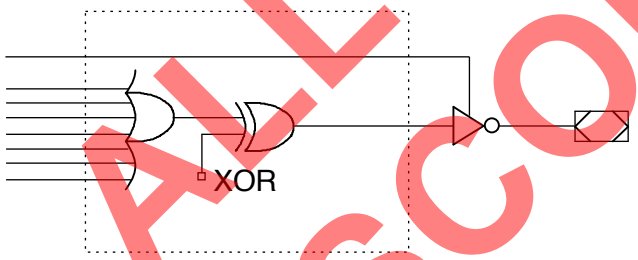
All macrocells have seven product terms per output. One product term is used for programmable output enable control. Pins 1 and 11 are always available as data inputs into the AND array.

The JEDEC fuse numbers including the UES fuses and PTD fuses are shown on the logic diagram on the following page.



Combinatorial I/O Configuration for Complex Mode

- SYN=1.
- AC0=1.
- XOR=0 defines Active Low Output.
- XOR=1 defines Active High Output.
- AC1=1.
- Pin 13 through Pin 18 are configured to this function.



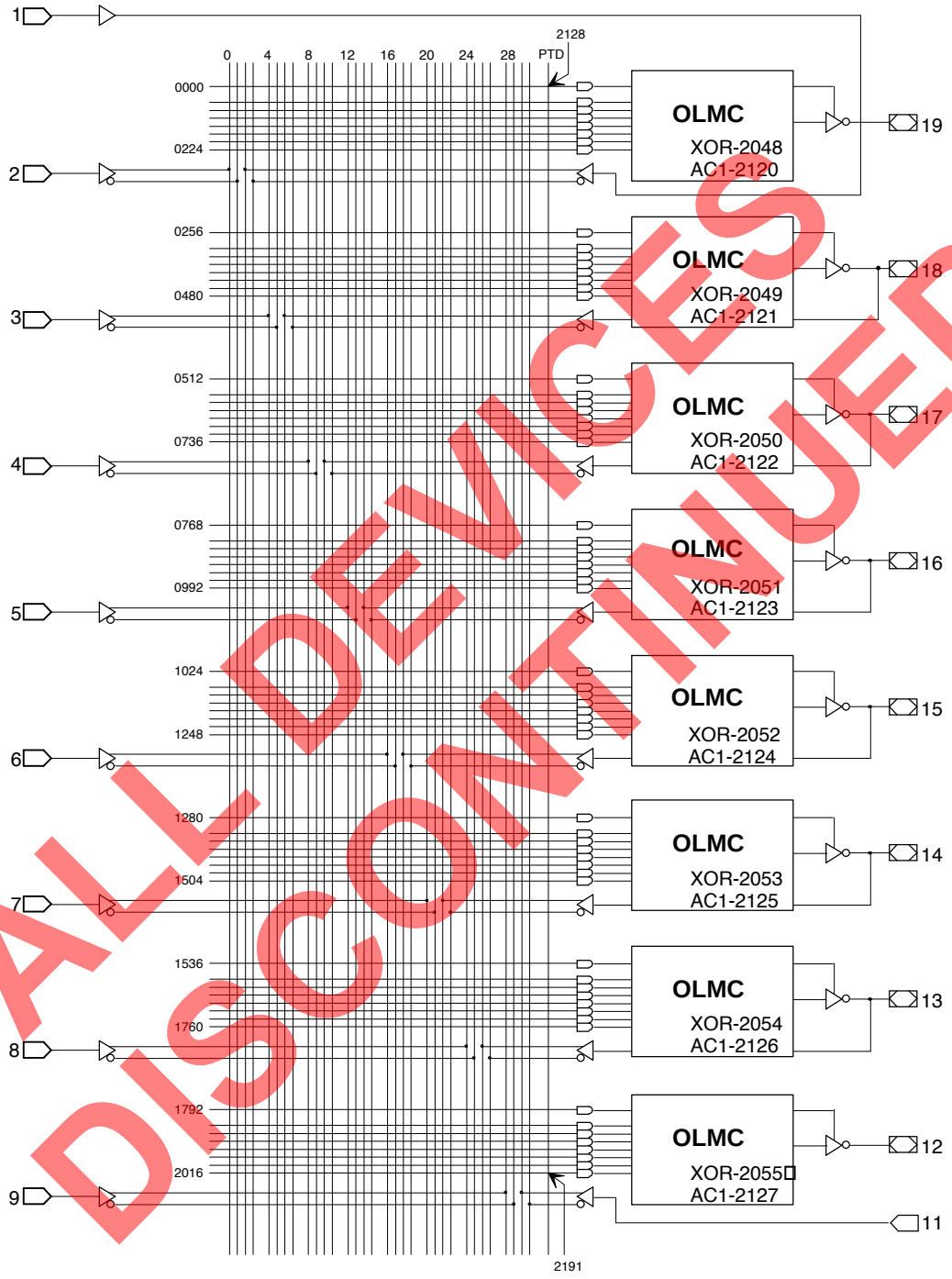
Combinatorial Output Configuration for Complex Mode

- SYN=1.
- AC0=1.
- XOR=0 defines Active Low Output.
- XOR=1 defines Active High Output.
- AC1=1.
- Pin 12 and Pin 19 are configured to this function.

Note: The development software configures all of the architecture control bits and checks for proper pin usage automatically.

Complex Mode Logic Diagram

PLCC Package Pinout



Simple Mode

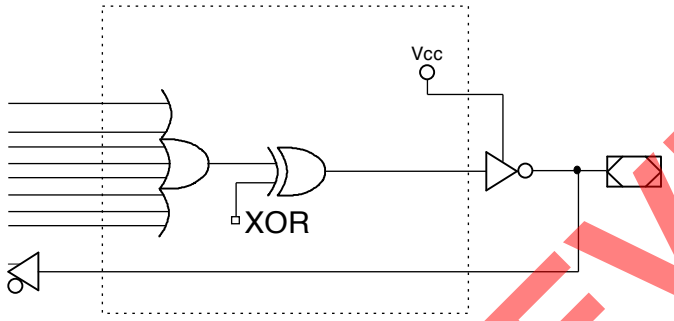
In the Simple mode, macrocells are configured as dedicated inputs or as dedicated, always active, combinatorial outputs.

Architecture configurations available in this mode are similar to the common 10L8 and 12P6 devices with many permutations of generic output polarity or input choices.

All outputs in the simple mode have a maximum of eight product terms that can control the logic. In addition, each output has programmable polarity.

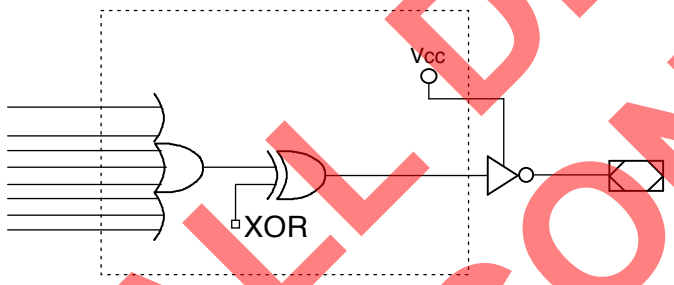
Pins 1 and 11 are always available as data inputs into the AND array. The center two macrocells (pins 15 & 16) cannot be used as input or I/O pins, and are only available as dedicated outputs.

The JEDEC fuse numbers including the UES fuses and PTD fuses are shown on the logic diagram.



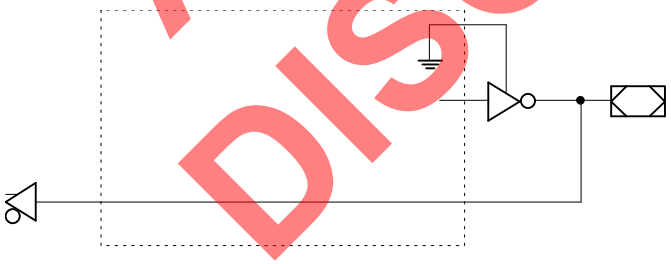
Combinatorial Output with Feedback Configuration for Simple Mode

- SYN=1.
- AC0=0.
- XOR=0 defines Active Low Output.
- XOR=1 defines Active High Output.
- AC1=0 defines this configuration.
- All OLMC **except** pins 15 & 16 can be configured to this function.



Combinatorial Output Configuration for Simple Mode

- SYN=1.
- AC0=0.
- XOR=0 defines Active Low Output.
- XOR=1 defines Active High Output.
- AC1=0 defines this configuration.
- Pins 15 & 16 are permanently configured to this function.



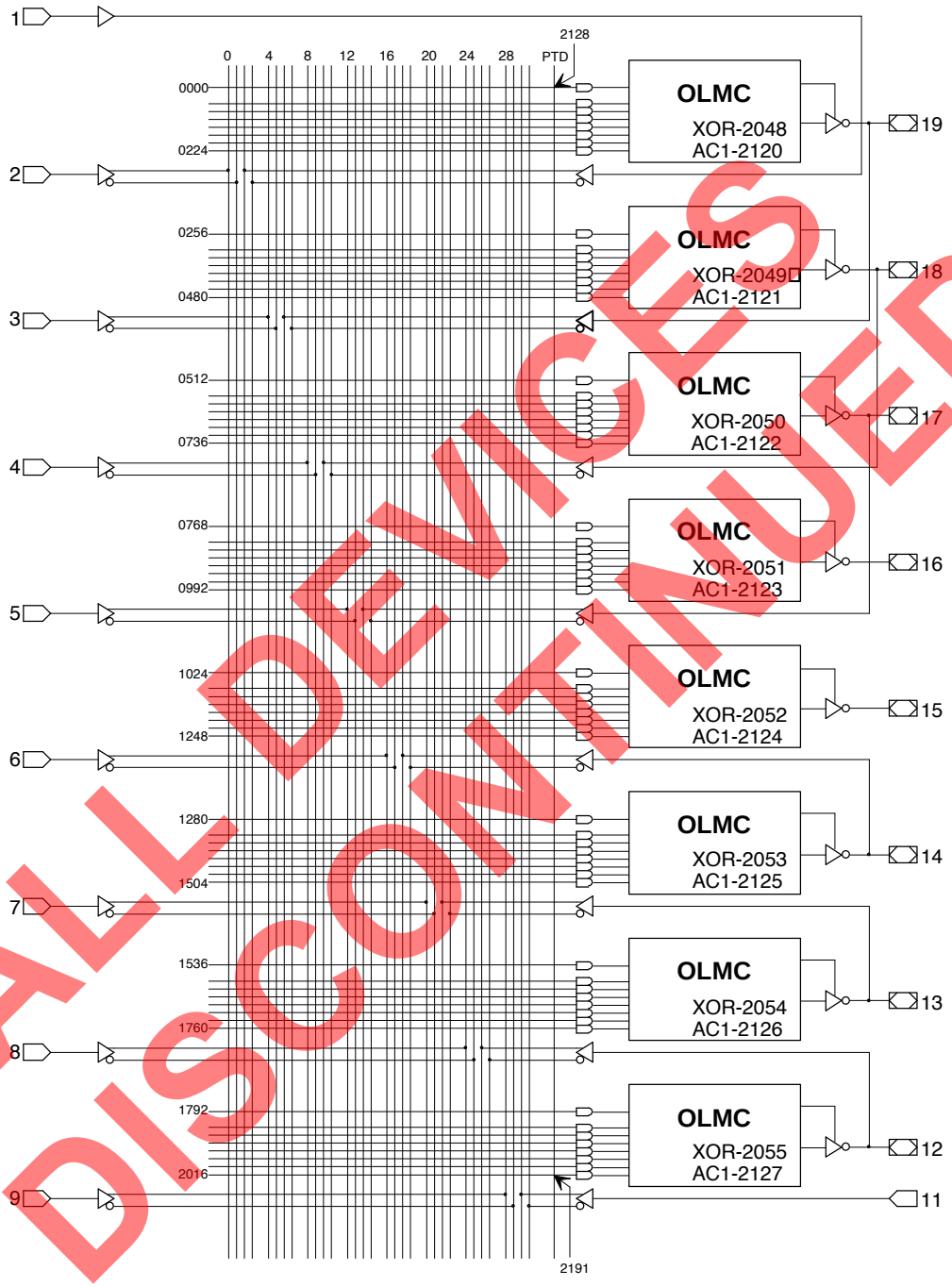
Dedicated Input Configuration for Simple Mode

- SYN=1.
- AC0=0.
- XOR=0 defines Active Low Output.
- XOR=1 defines Active High Output.
- AC1=1 defines this configuration.
- All OLMC **except** pins 15 & 16 can be configured to this function.

Note: The development software configures all of the architecture control bits and checks for proper pin usage automatically.

Simple Mode Logic Diagram

PLCC Package Pinout



64-USER ELECTRONIC SIGNATURE FUSES

2056, 2057, ...			.... 2118, 2119
Byte 7	Byte 6	.... Byte 1	Byte 0
MSB			LSB

SYN-2192
AC0-2193

AC Switching Characteristics

Over Recommended Operating Conditions

PARAMETER	TEST COND[1].	DESCRIPTION	COM -3 MIN.	COM -3 MAX.	COM -5 MIN.	COM -5 MAX.	UNITS
tpd[2]	A	Input or I/O to Combinational Output	1	3.5	1	5	ns
tco[2]	A	Clock to Output Delay	1	2.5	1	3	ns
tcf[3]	—	Clock to Feedback Delay	—	2	—	2	ns
tsu	—	Setup Time, Input or Feedback before Clock↑	3	—	4	—	ns
th	—	Hold Time, Input or Feedback after Clock↑	0	—	0	—	ns
fmax[4]	A	Maximum Clock Frequency with External Feedback, 1/(tsu + tco)	180	—	142.8	—	MHz
	A	Maximum Clock Frequency with Internal Feedback, 1/(tsu + tcf)	200	—	166	—	MHz
	A	Maximum Clock Frequency with No Feedback	250	—	166	—	MHz
twh[4]	—	Clock Pulse Duration, High	2	—	3	—	ns
twl[4]	—	Clock Pulse Duration, Low	2	—	3	—	ns
ten	B	Input or I/O to Output Enabled	—	4.5	—	6	ns
	B	$\overline{OE}$ to Output Enabled	—	3.5	—	5	ns
tdis	C	Input or I/O to Output Disabled	—	4.5	—	6	ns
	C	$\overline{OE}$ to Output Disabled	—	3.5	—	5	ns

1) Refer to **Switching Test Conditions** section.
2) Minimum values for tpd and tco are not 100% tested but established by characterization.
3) Calculated from fmax with internal feedback. Refer to **fmax Descriptions** section.
4) Refer to **fmax Descriptions** section. Characterized but not 100% tested.

Capacitance (T_A = 25°C, f = 1.0 MHz)

SYMBOL	PARAMETER	TYPICAL	UNITS	TEST CONDITIONS
C_I	Input Capacitance	5	pF	V_{CC} = 3.3V, V_I = 0V
$C_{I/O}$	I/O Capacitance	5	pF	V_{CC} = 3.3V, $V_{I/O}$ = 0V

Absolute Maximum Ratings(1)

Supply voltage V_{CC} ..... –0.5 to +5.6V
Input voltage applied ..... –0.5 to +5.6V
Off-state output voltage applied ..... –0.5 to +5.6V
Storage Temperature ..... –65 to 150°C
Ambient Temperature with
Power Applied ..... –55 to 125°C

1. Stresses above those listed under the "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress only ratings and functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied (while programming, follow the programming specifications).

Recommended Operating Conditions

Commercial Devices:
Ambient Temperature (T_A) ..... 0 to 75°C
Supply voltage (V_{CC})
with Respect to Ground ..... +3.0 to +3.6V

DC Electrical Characteristics

Over Recommended Operating Conditions (Unless Otherwise Specified)

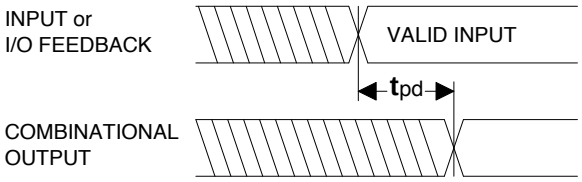
SYMBOL	PARAMETER	CONDITION	MIN.	TYP.[2]	MAX.	UNITS
V_{IL}	Input Low Voltage		Vss – 0.5	—	0.8	V
V_{IH}	Input High Voltage		2.0	—	5.25	V
I_{IL}	Input or I/O Low Leakage Current	$0V \le V_{IN} \le V_{IL}$ (MAX.)	—	—	-10	µA
I_{IH}	Input or I/O High Leakage Current	$(V_{CC} - 0.2)V \le V_{IN} \le V_{CC}$	—	—	10	µA
		$V_{CC} \le V_{IN} \le 5.25V$	—	—	30	mA
V_{OL}	Output Low Voltage	I_{OL} = MAX. Vin = V_{IL} or V_{IH}	—	—	0.4	V
		I_{OL} = 500 µA Vin = V_{IL} or V_{IH}	—	—	0.2	V
V_{OH}	Output High Voltage	I_{OH} = MAX. Vin = V_{IL} or V_{IH}	2.4	—	—	V
		I_{OH} = -500 µA Vin = V_{IL} or V_{IH}	Vcc-0.45	—	—	V
		I_{OH} = -100 µA Vin = V_{IL} or V_{IH}	Vcc-0.2	—	—	V
I_{OL}	Low Level Output Current		—	—	8	mA
I_{OH}	High Level Output Current		—	—	-4	mA
I_{OS}[1]	Output Short Circuit Current	V_{CC} = 3.3V V_{OUT} = 0.5V T_A = 25°C	-10	—	-60	mA

COMMERCIAL

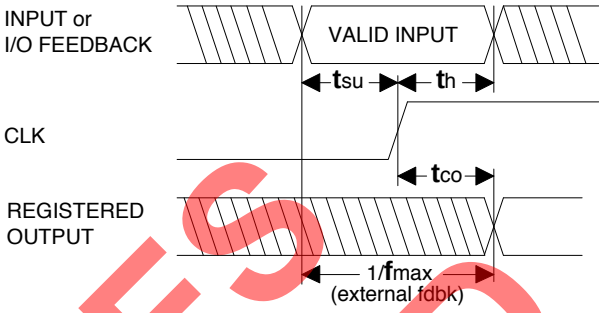
I_{CC}	Operating Power Supply Current	V_{IL} = 0.0V V_{IH} = 3.0V f_{toggle} = 1MHz Outputs Open	—	45	65	mA

1) One output at a time for a maximum duration of one second. Vout = 0.5V was selected to avoid test problems by tester ground degradation. Characterized but not 100% tested.
2) Typical values are at Vcc = 3.3V and T_A = 25 °C

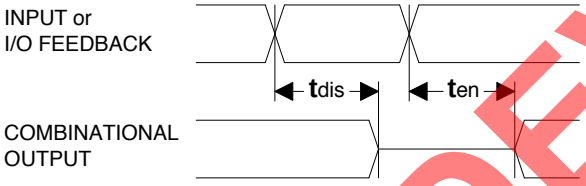
Switching Waveforms



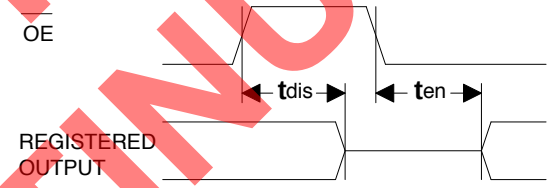
Combinatorial Output



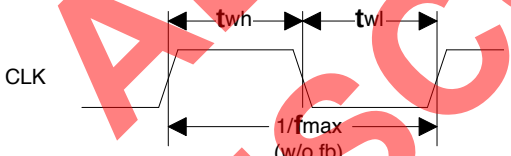
Registered Output



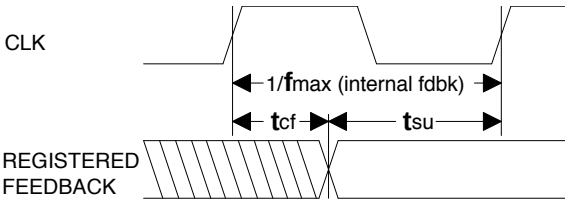
Input or I/O to Output Enable/Disable



$\overline{OE}$ to Output Enable/Disable

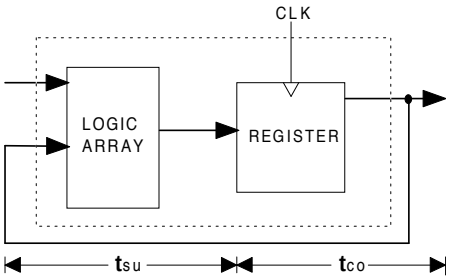


Clock Width



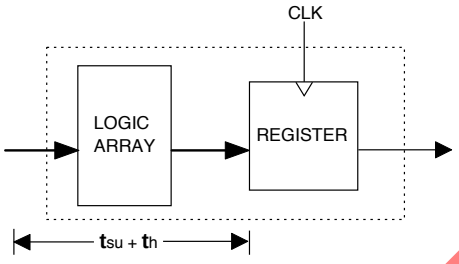
fmax with Feedback

fmax Descriptions



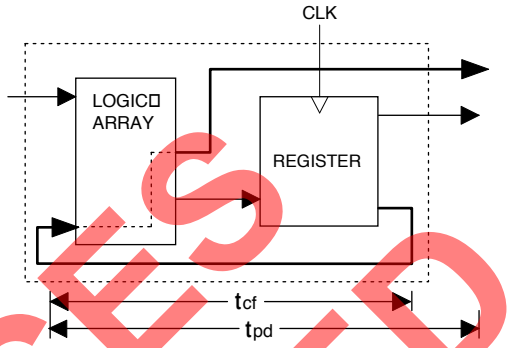
fmax with External Feedback 1/(tsu+tco)

Note: fmax with external feedback is calculated from measured tsu and tco.



fmax with No Feedback

Note: fmax with no feedback may be less than 1/(twh + twl). This is to allow for a clock duty cycle of other than 50%.



fmax with Internal Feedback 1/(tsu+tcf)

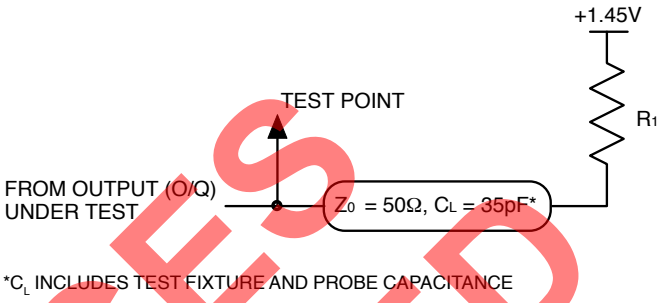
Note: tcf is a calculated value, derived by subtracting tsu from the period of fmax w/internal feedback (tcf = 1/fmax - tsu). The value of tcf is used primarily when calculating the delay from clocking a register to a combinatorial output (through registered feedback), as shown above. For example, the timing from clock to a combinatorial output is equal to tcf + tpd.

GAL16LV8D: Switching Test Conditions

Input Pulse Levels	GND to 3.0V
Input Rise and Fall Times	1.5ns 10% – 90%
Input Timing Reference Levels	1.5V
Output Timing Reference Levels	1.5V
Output Load	See Figure

GAL16LV8D Output Load Conditions (see figure)

Test Condition		R_1	C_L
A		50Ω	35pF
B	High Z to Active High at 1.9V	50Ω	35pF
	High Z to Active Low at 1.0V	50Ω	35pF
C	Active High to High Z at 1.9V	50Ω	35pF
	Active Low to High Z at 1.0V	50Ω	35pF



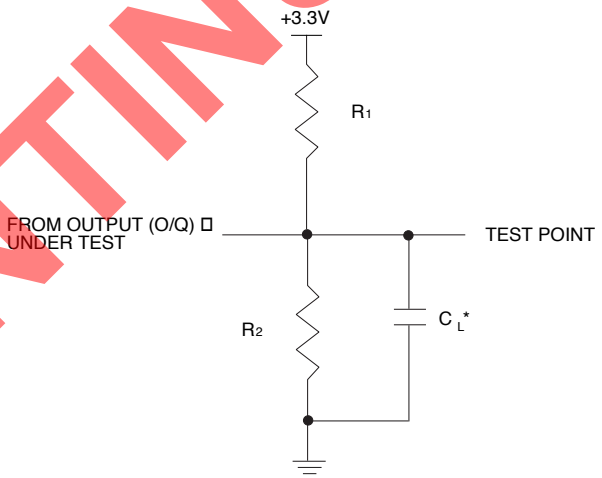
GAL16LV8C: Switching Test Conditions

Input Pulse Levels	GND to 3.0V
Input Rise and Fall Times	1.5ns 10% – 90%
Input Timing Reference Levels	1.5V
Output Timing Reference Levels	1.5V
Output Load	See Figure

3-state levels are measured 0.5V from steady-state active level.

GAL16LV8C Output Load Conditions (see figure)

Test Condition		R_1	R_2	C_L
A		316Ω	348Ω	35pF
B	Active High	316Ω	348Ω	35pF
	Active Low	316Ω	348Ω	35pF
C	Active High	316Ω	348Ω	5pF
	Active Low	316Ω	348Ω	5pF



Electronic Signature

An electronic signature is provided in every GAL16LV8 device. It contains 64 bits of reprogrammable memory that can contain user defined data. Some uses include user ID codes, revision numbers, or inventory control. The signature data is always available to the user independent of the state of the security cell.

NOTE: The electronic signature is included in checksum calculations. Changing the electronic signature will alter the checksum.

Security Cell

A security cell is provided in the GAL16LV8 devices to prevent unauthorized copying of the array patterns. Once programmed, this cell prevents further read access to the functional bits in the device. This cell can only be erased by re-programming the device, so the original configuration can never be examined once this cell is programmed. The Electronic Signature is always available to the user, regardless of the state of this control cell.

Latch-Up Protection

GAL16LV8 devices are designed with an on-board charge pump to negatively bias the substrate. The negative bias minimizes the potential of latch-up caused by negative input undershoots.

Device Programming

GAL devices are programmed using a Lattice Semiconductor-approved Logic Programmer, available from a number of manufacturers. Complete programming of the device takes only a few seconds. Erasing of the device is transparent to the user, and is done automatically as part of the programming cycle.

Output Register Preload

When testing state machine designs, all possible states and state transitions must be verified in the design, not just those required in the normal machine operations. This is because, in system operation, certain events occur that may throw the logic into an illegal state (power-up, line voltage glitches, brown-outs, etc.). To test a design for proper treatment of these conditions, a way must be provided to break the feedback paths, and force any desired (i.e., illegal) state into the registers. Then the machine can be sequenced and the outputs tested for correct next state conditions.

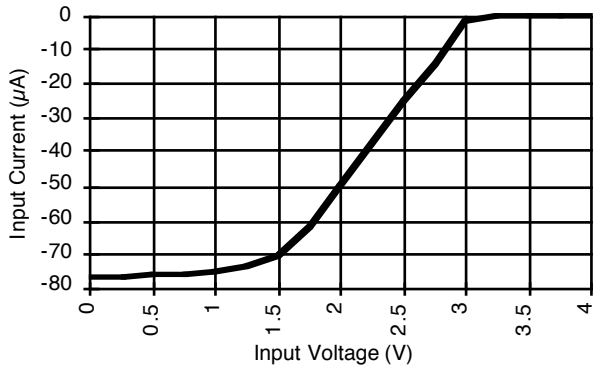
GAL16LV8 devices include circuitry that allows each registered output to be synchronously set either high or low. Thus, any present state condition can be forced for test sequencing. If necessary, approved GAL programmers capable of executing text vectors perform output register preload automatically.

Input Buffers

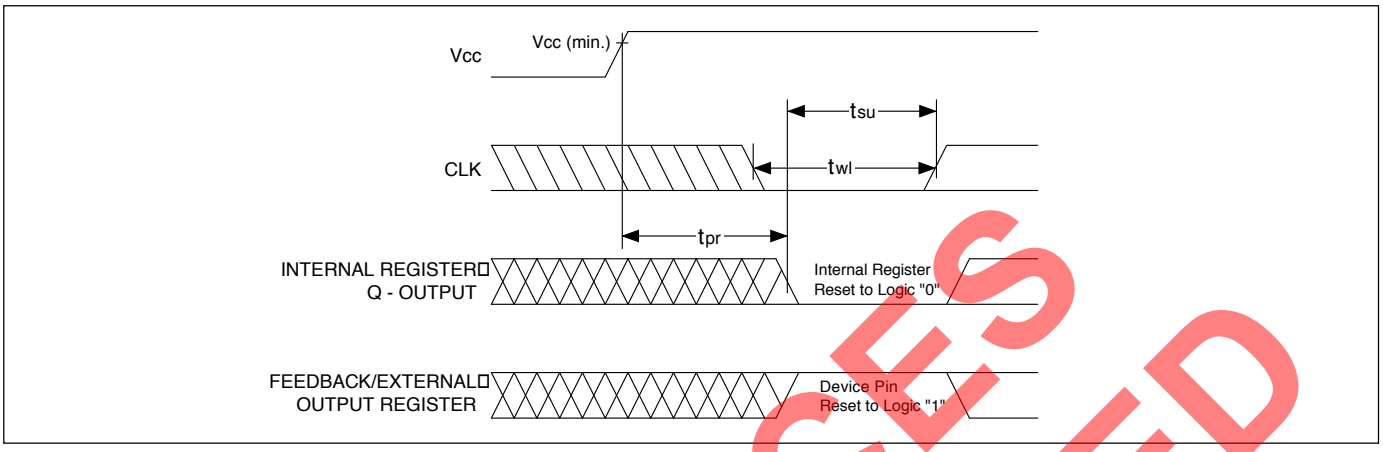
GAL16LV8 devices are designed with TTL level compatible input buffers. These buffers have a characteristically high impedance, and present a much lighter load to the driving logic than bipolar TTL devices.

The GAL16LV8D input and I/O pins have built-in active pull-ups. As a result, unused inputs and I/O's will float to a TTL "high" (logical "1"). Lattice Semiconductor recommends that all unused inputs and tri-stated I/O pins be connected to another active input, V_{CC}, or Ground. Doing this will tend to improve noise immunity and reduce I_{CC} for the device.

Typical Input Pull-up Characteristic (GAL16LV8D)

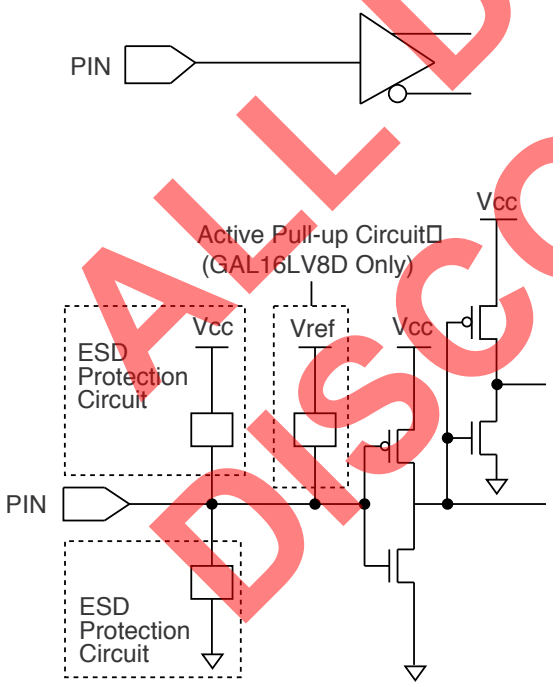


Power-Up Reset



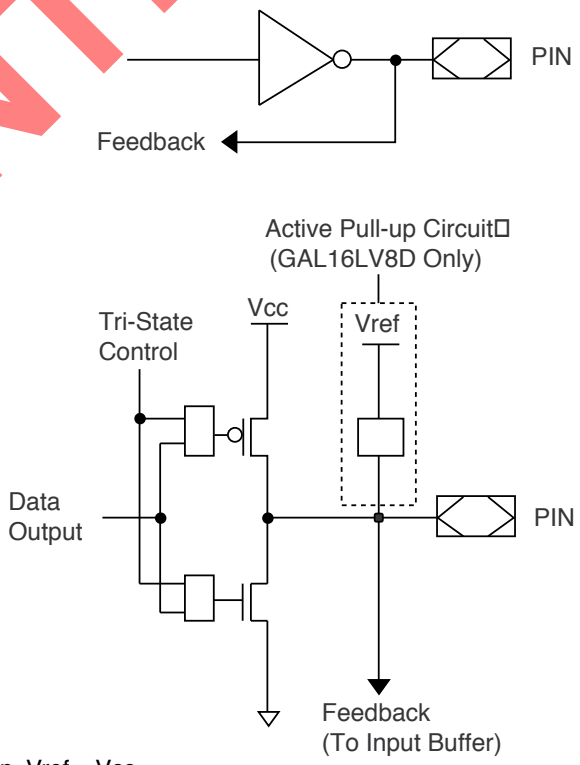
Circuitry within the GAL16LV8 provides a reset signal to all registers during power-up. All internal registers will have their Q outputs set low after a specified time (tpr, 1µs MAX). As a result, the state on the registered output pins (if they are enabled) will always be high on power-up, regardless of the programmed polarity of the output pins. This feature can greatly simplify state machine design by providing a known state on power-up. Because of the asynchronous nature of system power-up, some conditions must be met to provide a valid power-up reset of the device. First, the Vcc rise must be monotonic. Second, the clock input must be at static TTL level as shown in the diagram during power up. The registers will reset within a maximum of tpr time. As in normal system operation, avoid clocking the device until all input and feedback path setup times have been met. The clock must also meet the minimum pulse width requirements.

Input/Output Equivalent Schematics



Typ. Vref = Vcc

Typical Input

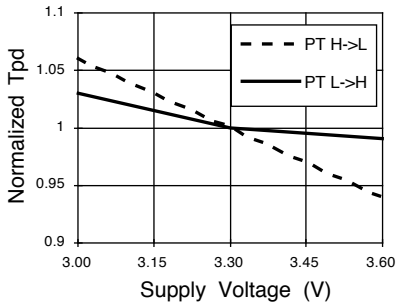


Typ. Vref = Vcc

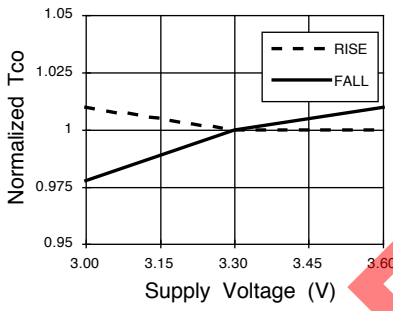
Typical Output

GAL16LV8D: Typical AC and DC Characteristic Diagrams

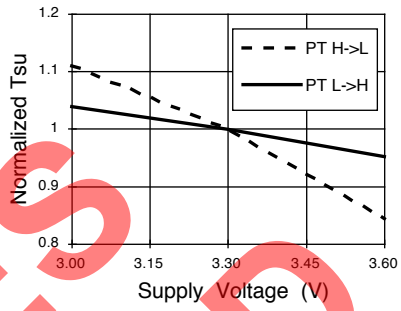
Normalized Tpd vs Vcc



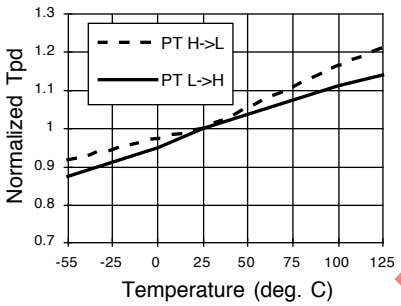
Normalized Tco vs Vcc



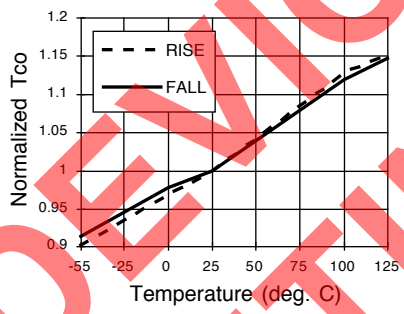
Normalized Tsu vs Vcc



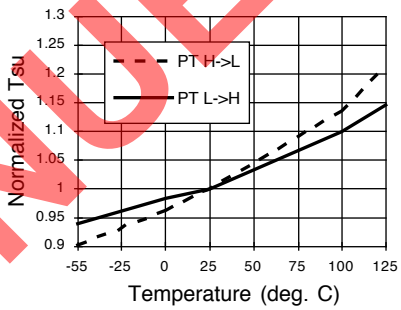
Normalized Tpd vs Temp



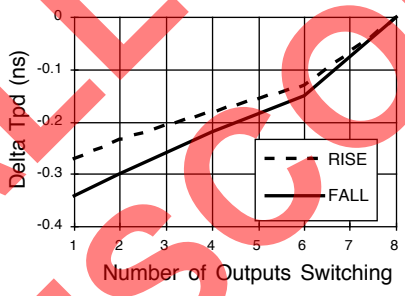
Normalized Tco vs Temp



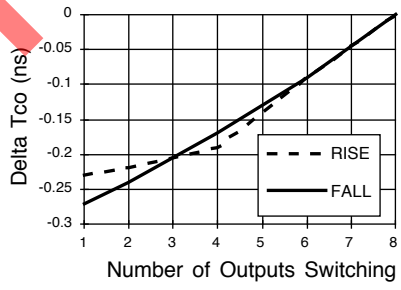
Normalized Tsu vs Temp



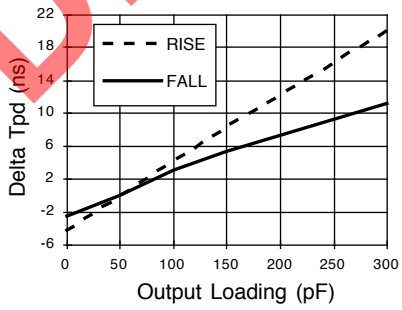
Delta Tpd vs # of Outputs Switching



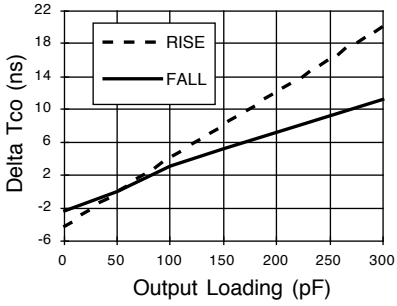
Delta Tco vs # of Outputs Switching



Delta Tpd vs Output Loading

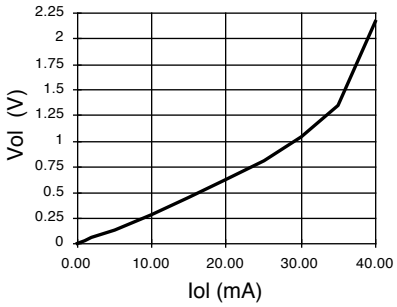


Delta Tco vs Output Loading

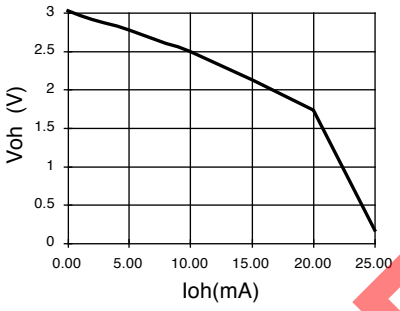


GAL16LV8D: Typical AC and DC Characteristic Diagrams

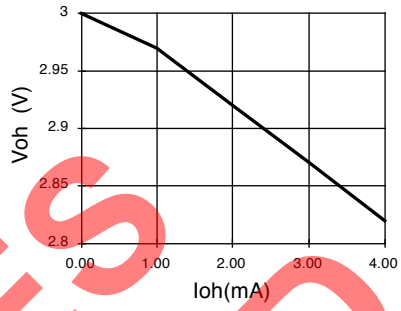
Vol vs Iol



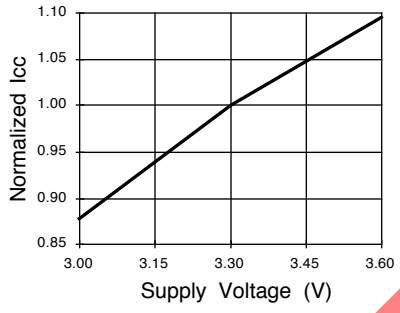
Voh vs Ioh



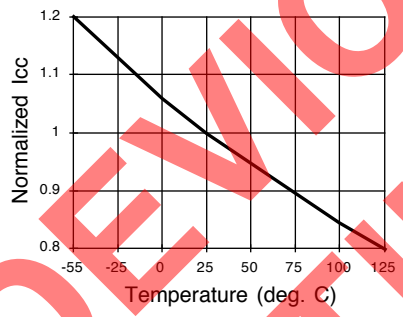
Voh vs Ioh



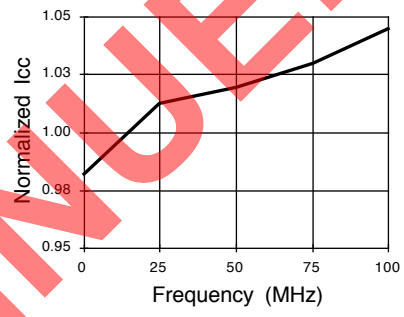
Normalized Icc vs Vcc



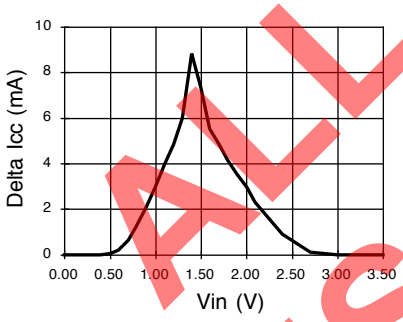
Normalized Icc vs Temp



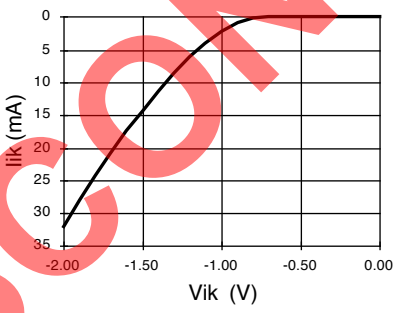
Normalized Icc vs Freq.



Delta Icc vs Vin (1 input)

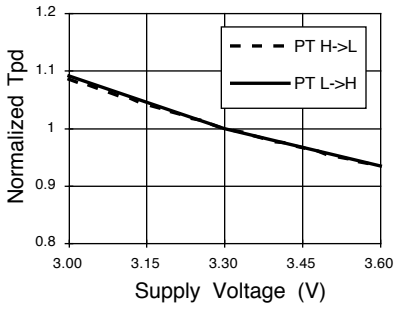


Input Clamp (Vik)

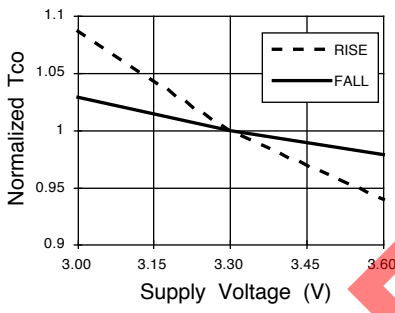


GAL16LV8C: Typical AC and DC Characteristic Diagrams

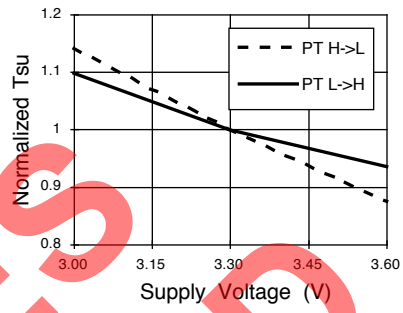
Normalized Tpd vs Vcc



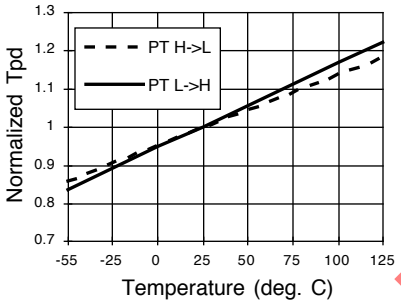
Normalized Tco vs Vcc



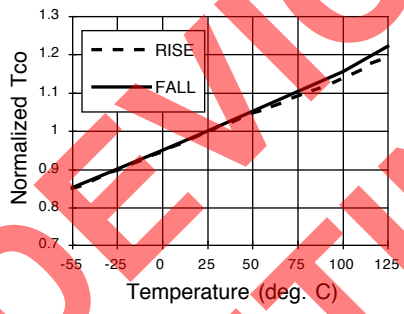
Normalized Tsu vs Vcc



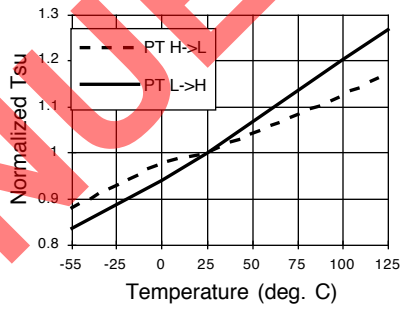
Normalized Tpd vs Temp



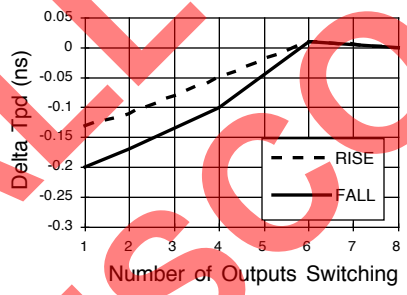
Normalized Tco vs Temp



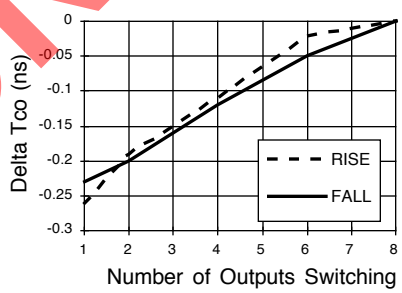
Normalized Tsu vs Temp



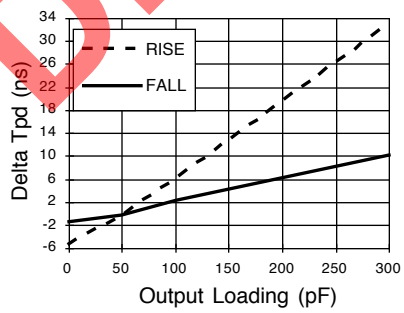
Delta Tpd vs # of Outputs Switching



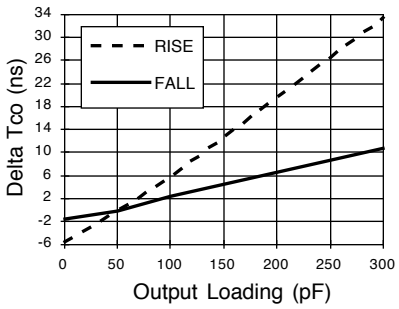
Delta Tco vs # of Outputs Switching



Delta Tpd vs Output Loading

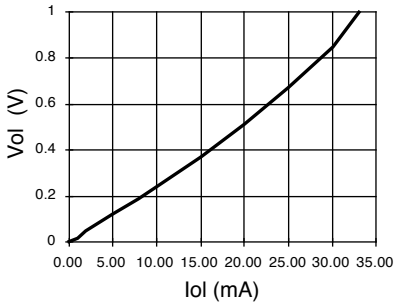


Delta Tco vs Output Loading

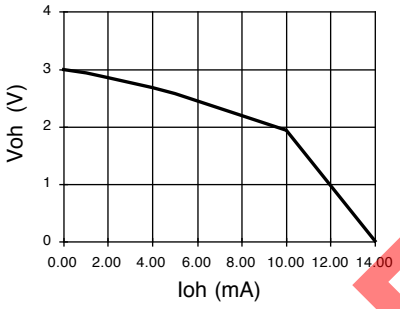


GAL16LV8C: Typical AC and DC Characteristic Diagrams

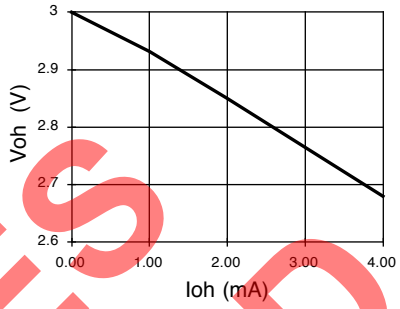
Vol vs Iol



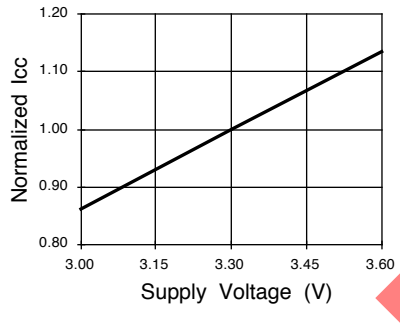
Voh vs Ioh



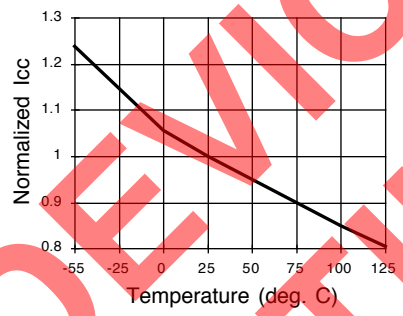
Voh vs Ioh



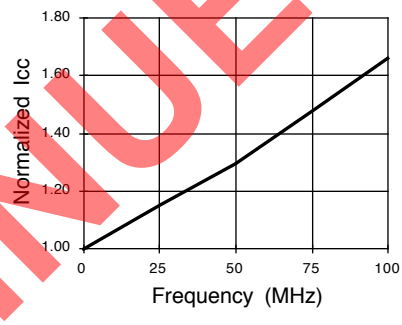
Normalized Icc vs Vcc



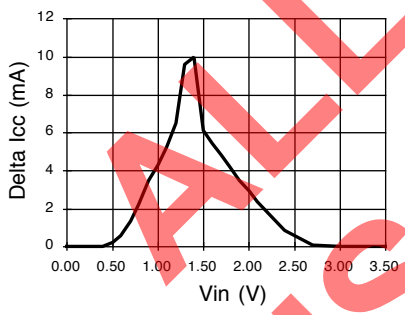
Normalized Icc vs Temp



Normalized Icc vs Freq.



Delta Icc vs Vin (1 input)



Input Clamp (Vik)