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## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Discontinued at Digi-Key |
| Core Processor | 80515 |
| Core Size | 8-Bit |
| Speed | 24MHz |
| Connectivity | I²C, SmartCard, UART/USART, USB |
| Peripherals | LED, POR, WDT |
| Number of I/O | 9 |
| Program Memory Size | 64KB (64K x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | - |
| RAM Size | 2K x 8 |
| Voltage - Supply (Vcc/Vdd) | 2.7V ~ 5.5V |
| Data Converters | - |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 85°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 44-VFQFN Exposed Pad |
| Supplier Device Package | 44-QFN (7x7) |
| Purchase URL | https://www.e-xfl.com/product-detail/analog-devices/73s1215f-44im-f-p |

# Table of Contents

**Internal Data Memory:** The Internal data memory provides 256 bytes (0x00 to 0xFF) of data memory. The internal data memory address is always one byte wide and can be accessed by either direct or indirect addressing. The Special Function Registers occupy the upper 128 bytes**. This SFR area is available only by direct addressing. Indirect addressing accesses the upper 128 bytes of Internal RAM.**

The lower 128 bytes contain working registers and bit-addressable memory. The lower 32 bytes form four banks of eight registers (R0-R7). Two bits on the program memory status word (PSW) select which bank is in use. The next 16 bytes form a block of bit-addressable memory space at bit addresses 0x00-0x7F. All of the bytes in the lower 128 bytes are accessible through direct or indirect addressing. Table 4 shows the internal data memory map.

**Table 4: Internal Data Memory Map**

<table>
<tr><th>Address</th><th>Direct Addressing</th><th>Indirect Addressing</th></tr>
<tr><td>0xFF</td><td rowspan="2">Special Function Registers (SFRs)</td><td rowspan="2">RAM</td></tr>
<tr><td>0x80</td></tr>
<tr><td>0x7F</td><td colspan="2" rowspan="2">Byte-addressable area</td></tr>
<tr><td>0x30</td></tr>
<tr><td>0x2F</td><td colspan="2" rowspan="2">Byte or bit-addressable area</td></tr>
<tr><td>0x20</td></tr>
<tr><td>0x1F</td><td colspan="2" rowspan="2">Register banks R0…R7 (x4)</td></tr>
<tr><td>0x00</td></tr>
</table>

**External Data Memory:** While the 80515 can address up to 64KB of external data memory in the space from 0x0000 to 0xFFFF, only the memory ranges shown in Figure 2 contain physical memory. The 80515 writes into external data memory when the MPU executes a MOVX @Ri,A or MOVX @DPTR,A instruction. The MPU reads external data memory by executing a MOVX A,@Ri or MOVX A,@DPTR instruction.

There are two types of instructions, differing in whether they provide an eight-bit or sixteen-bit indirect address to the external data RAM.

In the first type (MOVX A,@Ri), the contents of R0 or R1, in the current register bank, provide the eight lower-ordered bits of address. This method allows the user access to the first 256 bytes of the 2KB of external data RAM. In the second type of MOVX instruction (MOVX A,@DPTR), the data pointer generates a sixteen-bit address.

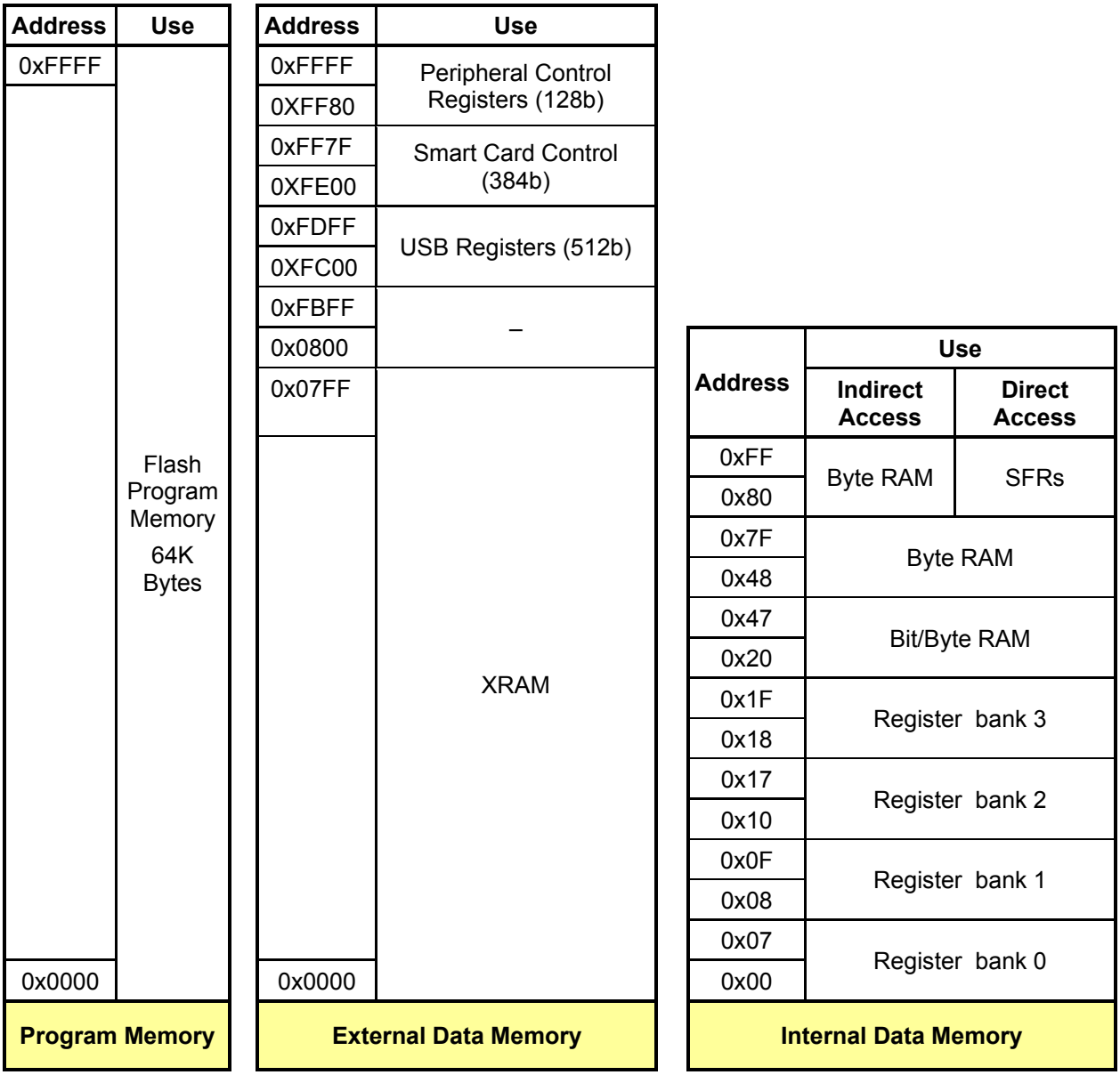



**Figure 2: Memory Map**

**Dual Data Pointer:** The Dual Data Pointer accelerates the block moves of data. The standard DPTR is a 16-bit register that is used to address external memory. In the 80515 core, the standard data pointer is called DPTR, the second data pointer is called DPTR1. The data pointer select bit chooses the active pointer. The data pointer select bit is located at the LSB of the DPS IRAM special function register (DPS.0). DPTR is selected when DPS.0 = 0 and DPTR1 is selected when DPS.0 = 1.

The user switches between pointers by toggling the LSB of the DPS register. All DPTR-related instructions use the currently selected DPTR for any activity.

**Note: The second data pointer may not be supported by certain compilers.**

The master clock control register enables different sections of the clock circuitry and specifies the value of the VCO Mcount divider. The MCLK must be configured to operate at 96MHz to ensure proper operation of some of the peripheral blocks according to the following formula:

MCLK = (Mcount * 2 + 4) * $F_{XTAL}$ = 96MHz

Mcount is configured in the MCLKCtl register must be bound between a value of 1 to 7. The possible crystal or external clock frequencies for getting MCLK = 96MHz are shown in Table 12.

**Table 12: Frequencies and Mcount Values for MCLK = 96MHz**

| $F_{XTAL}$ (MHz) | Mcount (N) |
|---|---|
| 12.00 | 2 |
| 9.60 | 3 |
| 8.00 | 4 |
| 6.86 | 5 |
| 6.00 | 6 |

**Master Clock Control Register (MCLKCtl): 0x8F ← 0x0A**

**Table 13: The MCLKCtl Register**

MSB LSB

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| HSOEN | KBEN | SCEN | USBEN | 32KEN | MCT.2 | MCT.1 | MCT.0 |

| Bit | Symbol | Function |
|---|---|---|
| MCLKCtl.7 | HSOEN | High-speed oscillator disable. When set = 1, disables the high-speed crystal oscillator and VCO/PLL system. Do not set this bit = 1. |
| MCLKCtl.6 | KBEN | 1 = Disable the keypad logic clock. |
| MCLKCtl.5 | SCEN | 1 = Disable the smart card logic clock. |
| MCLKCtl.4 | USBEN | 1 = Disable the USB logic clock. |
| MCLKCtl.3 | 32KEN | 1 = Disable the 32Khz oscillator. When the 32kHz oscillator is enabled, the RTC and other circuits such as debounce clocks are clocked using the 32kHz oscillator output. When disabled, the main oscillator provides the 32kHz clock for the RTC and other circuits. **Note: This bit must be set if there is no 32KHz crystal or the 44 pin package is used. Some internal clocks and circuits will not run if the oscillator is enabled and no crystal is connected.** |
| MCLKCtl.2 | MCT.2 | This value determines the ratio of the VCO frequency (MCLK) to the high-speed crystal oscillator frequency such that:<br>MCLK = (MCount*2 + 4)* $F_{XTAL}$. The default value is MCount = 2h such that MCLK = (2*2 + 4)*12.00MHz = 96MHz. |
| MCLKCtl.1 | MCT.1 | |
| MCLKCtl.0 | MCT.0 | |

The MPU clock that drives the CPU core defaults to 3.6923MHz after reset. The MPU clock is scalable by configuring the MPU Clock Control register (MPUCKCtl).

**Master Clock Control Register (MCLKCtl): 0x8F ← 0x0A**

**Table 18: The MCLKCtl Register**

| MSB | | | | | | | LSB |
|---|---|---|---|---|---|---|---|
| HSOEN | KBEN | SCEN | USBEN | 32KEN | MCT.2 | MCT.1 | MCT.0 |

| Bit | Symbol | Function |
|---|---|---|
| MCLKCtl.7 | HSOEN* | High-speed oscillator enable. When set = 1, disables the high-speed crystal oscillator and VCO/PLL system. This bit is not changed when the PWRDN bit is set but the oscillator/VCO/PLL is disabled. |
| MCLKCtl.6 | KBEN | 1 = Disable the keypad logic clock. This bit is not changed in PWRDN mode but the function is disabled. |
| MCLKCtl.5 | SCEN | 1 = Disable the smart card logic clock. This bit is not changed in PWRDN mode but the function is disabled. Interrupt logic for card insertion/removal remains operable even with smart card clock disabled. |
| MCLKCtl.4 | USBEN | 1 = Disable the USB logic clock. This bit is not changed in PWRDN mode but the function is disabled. |
| MCLKCtl.3 | 32KEN | 1 = Disable the 32Khz oscillator. This function is not affected by PWRDN mode. Note: This bit must be set if there is no 32KHz crystal or the 44 pin package is used. Some internal clocks and circuits will not run if the oscillator is enabled and no crystal is connected. |
| MCLKCtl.2 | MCT.2 | This value determines the ratio of the VCO frequency (MCLK) to the high-speed crystal oscillator frequency such that:<br>MCLK = (MCount*2 + 4)*Fxtal. The default value is MCount = 2h such that MCLK = (2*2 + 4)*12.00MHz = 96MHz. |
| MCLKCtl.1 | MCT.1 | |
| MCLKCtl.0 | MCT.0 | |

*Note: The HSOEN bit should never be set under normal circumstances. Power down control should only be initiated via use of the PWRDN bit in MISCtl0.

**Miscellaneous Control Register 0 (MISCtl0): 0xFFF1 ← 0x00**

Transmit and receive (TX and RX) pin selection and loop back test configuration are set up via this register.

**Table 38: The MISCtl0 Register**

| MSB | | | | | | | LSB |
|---|---|---|---|---|---|---|---|
| PWRDN | – | – | – | – | – | SLPBK | SSEL |

| Bit | Symbol | Function |
|---|---|---|
| MISCtl0.7 | PWRDN | This bit places the 73S1215F into a power down state. |
| MISCtl0.6 | – | |
| MISCtl0.5 | – | |
| MISCtl0.4 | – | |
| MISCtl0.3 | – | |
| MISCtl0.2 | – | |
| MISCtl0.1 | SLPBK | 1 = UART loop back testing mode. The pins TXD and RXD are to be connected together externally (with SLPBK =1) and therefore:<br>SLPBK SSEL Mode<br>0 0 normal using Serial_0<br>0 1 normal using Serial_1<br>1 0 Serial_0 TX feeds Serial_1 RX<br>1 1 Serial_1 TX feeds Serial_0 RX |
| MISCtl0.0 | SSEL | Selects either Serial_1 if set =1 or Serial_0 if set = 0 to be connected to RXD and TXD pins. |

#### 1.7.4.1 Serial Interface 0

The Serial Interface 0 can operate in four modes:

- **Mode 0**

  Pin RX serves as input and output. TX outputs the shift clock. 8 bits are transmitted with LSB first. The baud rate is fixed at 1/12 of the crystal frequency. Reception is initialized in Mode 0 by setting the flags in S0CON as follows: RI0 = 0 and REN0 = 1. In other modes, a start bit when REN0 = 1 starts receiving serial data.

- **Mode 1**

  Pin RX serves as input, and TX serves as serial output. No external shift clock is used, 10 bits are transmitted: a start bit (always 0), 8 data bits (LSB first), and a stop bit (always 1). On receive, a start bit synchronizes the transmission, 8 data bits are available by reading S0BUF, and stop bit sets the flag RB80 in the Special Function Register S0CON. In mode 1 either internal baud rate generator or timer 1 can be use to specify baud rate.

- **Mode 2**

  This mode is similar to Mode 1, with two differences. The baud rate is fixed at 1/32 or 1/64 of oscillator frequency and 11 bits are transmitted or received: a start bit (0), 8 data bits (LSB first), a programmable 9th bit, and a stop bit (1). The 9th bit can be used to control the parity of the serial interface: at transmission, bit TB80 in S0CON is output as the 9th bit, and at receive, the 9th bit affects RB80 in Special Function Register S0CON.

- **Mode 3**

  The only difference between Mode 2 and Mode 3 is that in Mode 3 either internal baud rate generator or timer 1 can be use to specify baud rate.

The S0BUF register is used to read/write data to/from the serial 0 interface.

**Table 42: Timers/Counters Mode Description**

| M1 | M0 | Mode | Function |
|---|---|---|---|
| 0 | 0 | Mode 0 | 13-bit Counter/Timer. |
| 0 | 1 | Mode 1 | 16-bit Counter/Timer. |
| 1 | 0 | Mode 2 | 8-bit auto-reload Counter/Timer. |
| 1 | 1 | Mode 3 | If Timer 1 M1 and M0 bits are set to '1', Timer 1 stops. If Timer 0 M1 and M0 bits are set to '1', Timer 0 acts as two independent 8-bit Timer/Counters. |

**Mode 0**

Putting either timer/counter into mode 0 configures it as an 8-bit timer/counter with a divide-by-32 prescaler. In this mode, the timer register is configured as a 13-bit register. As the count rolls over from all 1's to all 0's, it sets the timer overflow flag TF0. The overflow flag TF0 then can be used to request an interrupt. The counted input is enabled to the timer when TRx = 1 and either GATE = 0 or TX = 1 (setting GATE = 1 allows the timer to be controlled by external input TX, to facilitate pulse width measurements). TRx are control bits in the special function register TCON; GATE is in TMOD. The 13-bit register consists of all 8 bits of TH1 and the lower 5 bits of TL0. The upper 3 bits of TL0 are indeterminate and should be ignored. Setting the run flag (TRx) does not clear the registers. Mode 0 operation is the same for timer 0 as for timer 1.

**Mode 1**

Mode 1 is the same as mode 0, except that the timer register is run with all 16 bits.

**Mode 2**

Mode 2 configures the timer register as an 8-bit counter (TLx) with automatic reload. The overflow from TLx not only sets TFx, but also reloads TLx with the contents of THx, which is preset by software. The reload leaves THx unchanged.

**Mode 3**

Mode 3 has different effects on timer 0 and timer 1. Timer 1 in mode 3 simply holds its count. The effect is the same as setting TR1 = 0. Timer 0 in mode 3 establishes TL0 and TH0 as two separate counters. TL0 uses the timer 0 control bits: C/T, GATE, TR0, INT0, and TF0. TH0 is locked into a timer function (counting machine cycles) and takes over the use of TR1 and TF1 from timer 1. Thus, TH0 now controls the "timer 1" interrupt. Mode 3 is provided for applications requiring an extra 8-bit timer or counter. When timer 0 is in mode 3, timer 1 can be turned on and off by switching it out of and into its own mode 3, or can still be used by the serial channel as a baud rate generator, or in fact, in any application not requiring an interrupt from timer 1 itself.

### 1.7.9 Analog Voltage Comparator

The 73S1215F includes a programmable comparator that is connected to the ANA_IN pin. The comparator can be configured to trigger an interrupt if the input voltage rises above or falls below a selectable threshold voltage. The comparator control register should not be modified when the analog interrupt (ANAIEN bit in the INT6Ctl register) is enabled to guard against any false interrupt that might be generated when modifying the threshold. The comparator has a built-in hysteresis to prevent the comparator from repeatedly responding to low-amplitude noise. This hysteresis is approximately 20mV. The maximum voltage on the ANA_IN pad should be less than 3 volts. An external resistor divider is required for detecting voltages greater than 3.0 volts. Interrupt control is handled in the INT6Ctl register.

**Analog Compare Control Register (ACOMP): 0xFFD0 ← 0x00**

**Table 60: The ACOMP Register**

MSB LSB

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| ANALVL | – | ONCHG | CPOL | CMPEN | 0 | TSEL.1 | TSEL.0 |

| Bit | Symbol | Function |
|---|---|---|
| ACOMP.7 | ANALVL | When read, indicates whether the input level is above or below the threshold. This is a real time value and is not latched, so it may change from the time of the interrupt trigger until read. |
| ACOMP.6 | – | |
| ACOMP.5 | ONCHG | If set, the Ana_interrupt is invoked on any change above or below the threshold, bit 4 is ignored. |
| ACOMP.4 | CPOL | If set = 1, Ana_interrupt is invoked when signal rises above selected threshold. If set = 0, Ana_interrupt is invoked when signal goes below selected threshold (default). |
| ACOMP.3 | CMPEN | Enables power to the analog comparator. 1= Enabled. 0 = Disabled (default). |
| ACOMP.2 | 0 | This value must be fixed at 0. |
| ACOMP.1 | TSEL.1 | Sets the voltage threshold for comparison to the voltage on pin ANA_IN. Thresholds are as follows:<br>00 = 1.00V<br>01 = 1.24V<br>10 = 1.40V<br>11 = 1.50V |
| ACOMP.0 | TSEL.0 | |

### I2C Secondary Read Data Register (SRDR): 0XFF84 ← 0x00

**Table 67: The SRDR Register**

| MSB | | | | | | | LSB |
|---|---|---|---|---|---|---|---|
| SRDR.7 | SRDR.6 | SRDR.5 | SRDR.4 | SRDR.3 | SRDR.2 | SRDR.1 | SRDR.0 |

| Bit | Function |
|---|---|
| SRDR.7 | Second Data byte to be read from the $I^2C$ slave device if bit 0 (I2CLEN) of the Control and Status register (CSR) is set = 1. |
| SRDR.6 | |
| SRDR.5 | |
| SRDR.4 | |
| SRDR.3 | |
| SRDR.2 | |
| SRDR.1 | |
| SRDR.0 | |

### I2C Control and Status Register (CSR): 0xFF85 ← 0x00

**Table 68: The CSR Register**

| MSB | | | | | | | LSB |
|---|---|---|---|---|---|---|---|
| – | – | – | – | – | AKERR | I2CST | I2CLEN |

| Bit | Symbol | Function |
|---|---|---|
| CSR.7 | – | |
| CSR.6 | – | |
| CSR.5 | – | |
| CSR.4 | – | |
| CSR.3 | – | |
| CSR.2 | AKERR | Set to 1 if acknowledge bit from Slave Device is not 0. Automatically reset when the new bus transaction is started. |
| CSR.1 | I2CST | Write a 1 to start $I^2C$ transaction. Automatically reset to 0 when the bus transaction is done. This bit should be treated as a “busy” indicator on reading. If it is high, the serial read/write operations are not completed and no new address or data should be written. |
| CSR.0 | I2CLEN | Set to 1 for 2-byte read or write operations. Set to 0 for 1-byte operations. |

**Keypad Scan Time Register (KSCAN): 0xD3 ← 0x00**

This register contains the values of scanning time and debouncing time.

**Table 72: The KSCAN Register**

| MSB | | | | | | | LSB |
|---|---|---|---|---|---|---|---|
| DBTIME.5 | DBTIME.4 | DBTIME.3 | DBTIME.2 | DBTIME.1 | DBTIME.0 | SCTIME.1 | SCTIME.0 |

| Bit | Symbol | Function |
|---|---|---|
| KSCAN.7 | DBTIME.5 | De-bounce time in 4ms increments. 1 = 4ms de-bounce time, 0x3F = 252ms, 0x00 = 256ms. Key presses and key releases are de-bounced by this amount of time. |
| KSCAN.6 | DBTIME.4 | |
| KSCAN.5 | DBTIME.3 | |
| KSCAN.4 | DBTIME.2 | |
| KSCAN.3 | DBTIME.1 | |
| KSCAN.2 | DBTIME.0 | |
| KSCAN.1 | SCTIME.1 | Scan time in ms. 01 = 1ms, 02 = 2ms, 00 = 3ms, 00 = 4ms. Time between checking each key during keypad scanning. |
| KSCAN.0 | SCTIME.0 | |

**Keypad Control/Status Register (KSTAT): 0xD4 ← 0x00**

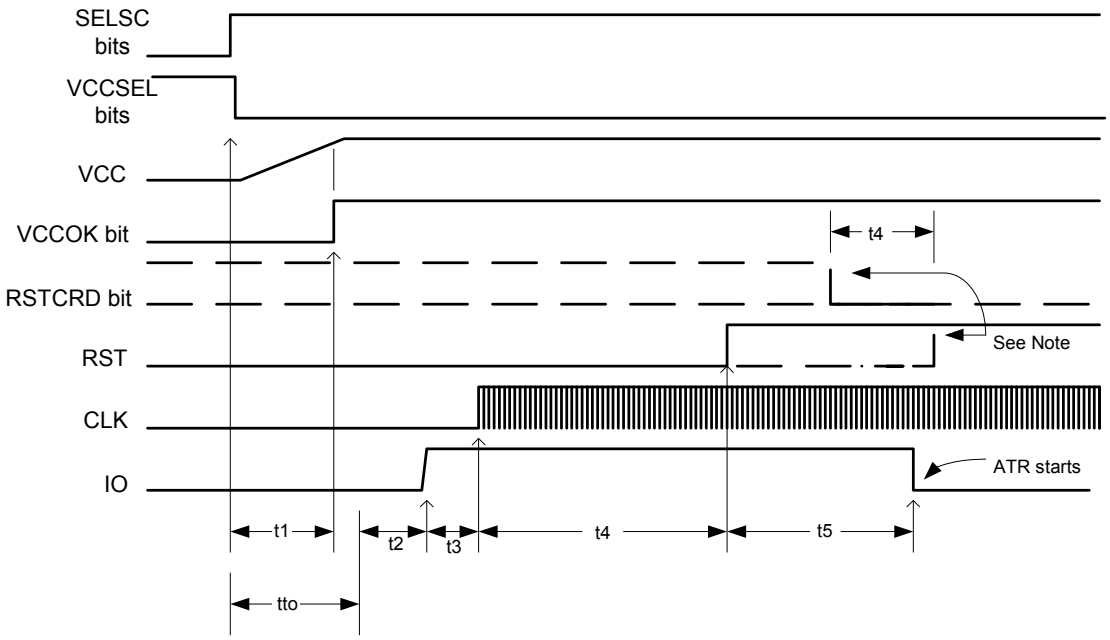
This register is used to control the hardware keypad scanning and detection capabilities, as well as the keypad interrupt control and status.

**Table 73: The KSTAT Register**

| MSB | | | | | | | LSB |
|---|---|---|---|---|---|---|---|
| – | – | – | – | KEYCLK | HWSCEN | KEYDET | KYDTEN |

| Bit | Symbol | Function |
|---|---|---|
| KSTAT.7 | – | |
| KSTAT.6 | – | |
| KSTAT.5 | – | |
| KSTAT.4 | – | |
| KSTAT.3 | KEYCLK | The current state of the keyboard clock can be read from this bit. |
| KSTAT.2 | HWSCEN | Hardware Scan Enable – When set, the hardware will perform automatic key scanning. When cleared, the firmware must perform the key scanning manually (bypass mode). |
| KSTAT.1 | KEYDET | Key Detect – When HWSCEN = 1 this bit is set causing an interrupt that indicates a valid key press was detected and the key location can be read from the Keypad Column and Row registers. When HWSCEN = 0, this bit is an interrupt which indicates a falling edge on any Row input if all Row inputs had been high previously (note: multiple Key Detect interrupts may occur in this case due to the keypad switch bouncing). In all cases, this bit is cleared when read. When HWSCEN = 0 and the keypad interface 1kHz clock is disabled, a key press will still set this bit and cause an interrupt. |
| KSTAT.0 | KYDTEN | Key Detect Enable – When set, the KEYDET bit can cause an interrupt and when cleared the KEYDET cannot cause an interrupt. KEYDET can still get set even if the interrupt is not enabled. |

Smart card RST, I/O and CLK, C4, C8 shall be low before the end of the deactivation sequence. Figure 18 shows the timing for a deactivation sequence.




t1: SELSC.1 bit set (selects internal ICC interface) and a non-zero value in VCCSEL bits (calling for a value of Vcc of 1.8, 3.0, or 5.0 volts) will begin the activation sequence. t1 is the time for Vcc to rise to acceptable level, declared as Vcc OK (bit VCCOK gets set). This time depends on filter capacitor value and card Icc load.

tto: The time allowed for Vcc to rise to Vcc OK status after setting of the VCCSEL bits. This time is generated by the VCCTMR counter. If Vcc OK is not set, (bit VCCOK) at this time, a deactivation will be initiated. VCCSEL bits are not automatically cleared. The firmware must clear the VCCSEL bits before starting a new activation.

t2: Time from VCCTMR timeout and VCC OK to IO reception (high), typically 2-3 CLK cycles if RDYST = 0. If RDYST = 1, t2 starts when VCCOK = 1.

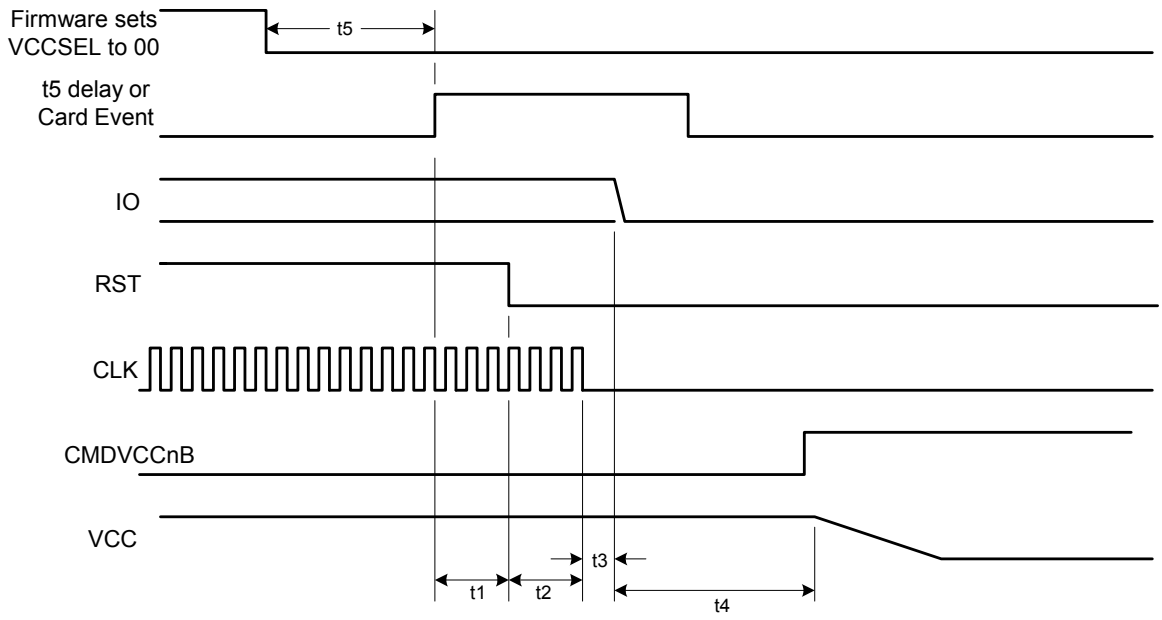
t3: Time from IO = high to CLK start, typically 2-3 CLK cycles.

t4: Time allowed for start of CLK to de-assertion of RST. Programmable by RLength register.

t5: Time allowed for ATR timeout, set by the STSTO register.

Note: If the RSTCRD bit is set, RST is asserted (low). Upon clearing RSTCRD bit, RST will be de-asserted after t4.

**Figure 17: Asynchronous Activation Sequence Timing**




t1: Time after either a "card event" occurs or firmware sets the VCCSela and VCCSelb bits to 0 (see t5, VCCOff_tmr) occurs until RST is asserted low.

t2: Time after RST goes low until CLK stops.

t3: Time after CLK stops until IO goes low.

t4: Time after IO goes low until VCC is powered down.

t5: Delayed VCC off time (in ETUs per VCCOff_tmr bits). Only in effect due to firmware deactivation.

**Figure 18: Deactivation Sequence**

#### 1.7.15.3 Data Reception/Transmission

When a 12Mhz crystal is used, the smart card UART will generate a 3.69Mhz (default) clock to both smart card interfaces. This will allow approximately 9600bps (1/ETU) communication during ATR (ISO 7816 default). As part of the PPS negotiation between the smart card and the reader, the firmware may determine that the smart card parameters F & D may be changed. After this negotiation, the firmware may change the ETU by writing to the SFR FDReg to adjust the ETU and CLK. The firmware may also change the smart card clock frequency by writing to the SFR SCCLK (SCECLK for external interface). Independent clock frequency control is provided to each smart card interface. Clock stop high or Clock stop low is supported in asynchronous mode. Figure 19 shows the ETU and CLK control circuits. The firmware determines when clock stop is supported by the smart card and when it is appropriate to go into that mode (and when to come out of it). The smart card UART is clocked by the same clock that is provided to the selected smart card. The transition between smart card clocks is handled in hardware to eliminate any glitches for the UART during switchover. The external smart card clock is not affected when switching the UART to communicate with the internal smart card.

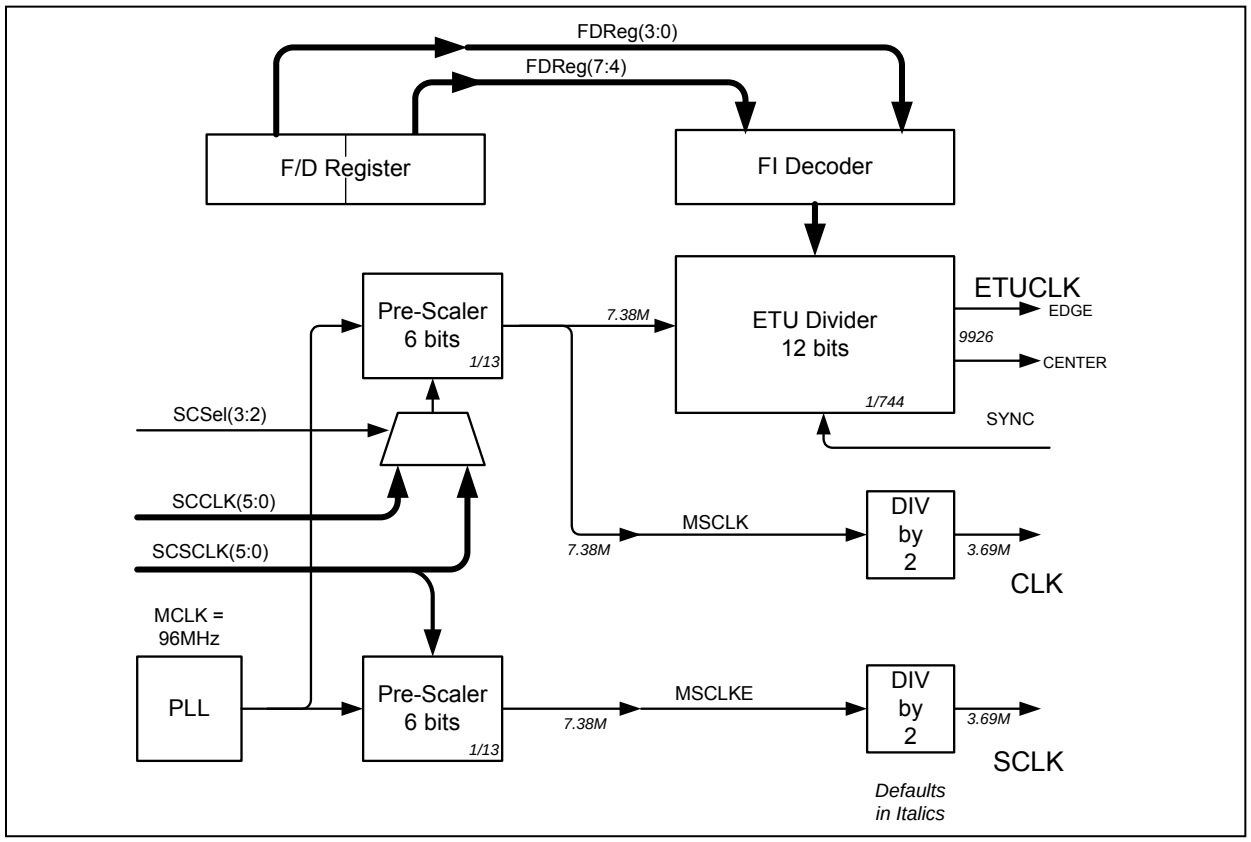



**Figure 19: Smart Card CLK and ETU Generation**

There are two, two-byte FIFOs that are used to buffer transmit and receive data. During a T=0 processing, if a parity error is detected by the 73S1215F during message reception, an error signal (BREAK) will be generated to the smart card. The byte received will be discarded and the firmware notified of the error. Break generation and receive byte dropping can be disabled under firmware control. During the transmission of a byte, if an error signal (BREAK) is detected, the last byte is retransmitted again and the firmware notified. Retransmission can be disabled by firmware. When a correct byte is received, an interrupt is generated to the firmware, which then reads the byte from the receive FIFO. Receive overruns are detected by the hardware and reported via an interrupt. During transmission of a message, the firmware will write bytes into the transmit FIFO. The hardware will send them to the smart card. When the last byte of a message has been written, the firmware will need to set the LASTTX bit in the STXCtl SFR. This will cause the hardware to insert the CRC/LRC if in a T=1 protocol mode. CRC/LRC generation/checking is only provided during T=1 processing. Firmware will need to instruct the smart function to go into receive mode after this last transmit data byte if it expects a response from the smart card. At the end of the smart card response, the firmware will put the interface back into transmit mode if appropriate.

The hardware can check for the following card-related timeouts:

- Character Waiting Time (CWT)
- Block Waiting Time (BWT)
- Initial Waiting Time (IWT)

The firmware will load the Wait Time registers with the appropriate value for the operating mode at the appropriate time. Figure 20 shows the guard, block, wait and ATR time definitions. If a timeout occurs, an interrupt will be generated and the firmware can take appropriate recovery steps. Support is provided for adding additional guard times between characters (Extra Guard Time register) and between the last byte received by the 73S1215F and the first byte transmitted by the 73S1215F Block Guard Time register (BGT). Other than the protocol checks described above, the firmware is responsible for all protocol checking and error recovery.

### C4/C8 Data Direction Register (SCDIR): 0xFE0C ← 0x00

This register determines the direction of the internal interface C4/C8 lines. After reset, all signals are tri-stated.

**Table 92: The SCDIR Register**

MSB LSB

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| – | – | – | – | C8D | C4D | – | – |

| Bit | Symbol | Function |
|---|---|---|
| SCDIR.7 | – | |
| SCDIR.6 | – | |
| SCDIR.5 | – | |
| SCDIR.4 | – | |
| SCDIR.3 | C8D | 1 = input, 0 = output. Smart Card C8 direction. |
| SCDIR.2 | C4D | 1 = input, 0 = output. Smart Card C4 direction. |
| SCDIR.1 | – | |
| SCDIR.0 | – | |

### 1.7.16 VDD Fault Detect Function

The 73S1215F contains a circuit to detect a low-voltage condition on the supply voltage $V_{DD}$. If enabled, it will deactivate the active internal smart card interface when $V_{DD}$ falls below the $V_{DD}$ Fault threshold. The register configures the $V_{DD}$ Fault threshold for the nominal default of 2.3V* or a user selectable threshold. The user's code may load a different value using the FOVRVDDF bit =1 after the power-up cycle has completed

**VDDFault Control Register (VDDFCtl): 0xFFD4 ← 0x00**

**Table 118: The VDDFCtl Register**

MSB LSB

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| – | FOVRVDDF | VDDFLTEN | – | STXDAT.3 | VDDFTH.2 | VDDFTH.1 | VDDFTH.0 |

| Bit | Symbol | Function |
|---|---|---|
| VDDFCtl.7 | – | |
| VDDFCtl.6 | FOVRVDDF | Setting this bit high will allow the VDDFLT(2:0) bits set in this register to control the VDDFault threshold. When this bit is set low, the VDDFault threshold will be set to the factory default setting of 2.3V*. |
| VDDFCtl.5 | VDDFLTEN | Set = 1 will disable VDD Fault operation. |
| VDDFCtl.4 | – | |
| VDDFCtl.3 | – | |
| VDDFCtl.2 | VDDFTH.2 | VDD Fault Threshold.<br>Bit value(2:0) VDDFault voltage<br>000 2.3 (nominal default)<br>001 2.4<br>010 2.5<br>011 2.6<br>100 2.7<br>101 2.8<br>110 2.9<br>111 3.0 |
| VDDFCtl.1 | VDDFTH.1 | |
| VDDFCtl.0 | VDDFTH.0 | |

* Note: The $V_{DD}$ Fault factory default can be set to any threshold as defined by bits VDDFTH(2:0). The 73S1215F has the capability to burn fuses at the factory to set the factory default to any of these voltages. Contact Teridian for further details.

### 3.7.1 DC Characteristics

| Symbol | Parameter | Condition | Min | Typ. | Max | Unit |
|---|---|---|---|---|---|---|
| $I_{DD}$ | Supply Current | CPU clock @ 24MHz | | 30 | 35 | mA |
| | | CPU clock @ 12MHz | | 22 | 25.5 | mA |
| | | CPU clock @ 6MHz | | 16 | 19.5 | mA |
| | | CPU clock @ 3.69MHz | | 14 | 17 | mA |
| | | Power down (-40□ to 85□C) | | 8 | 50 | μA |
| | | Power down (25□C) | | 6 | 13 | μA |
| $I_{PC}$ | Supply Current | $V_{CC}$ on, ICC=0 I/O, AUX1, AUX2=high, CLK not toggling | | 450 | 650 | μA |
| | | Power down | | 1 | 10 | |
| $I_{PCOFF}$ | $V_{PC}$ supply current when $V_{CC}$ = 0 | Smart card deactivated | | 345 | | μA |

## 3.8 Voltage / Temperature Fault Detection Circuits

| Symbol | Parameter | Condition | Min | Typ. | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{PCF}$ | $V_{PC}$ fault ($V_{PC}$ Voltage supervisor threshold) | $V_{PC}$<$V_{CC}$, a transient event | | $V_{CC}$ > $V_{PC}$ + 0.3 | | V |
| $V_{CCF}$ | VCCOK = 0 ($V_{CC}$ Voltage supervisor threshold) | $V_{CC}$ = 5V | | | 4.6 | V |
| | | $V_{CC}$= 3V | | | 2.7 | V |
| | | $V_{CC}$= 1.8V | | | 1.65 | |
| $T_F$ | Die over temperature fault | | 115 | | 145 | °C |
| ICCF | Vcc over current fault | | 110 | | | mA |

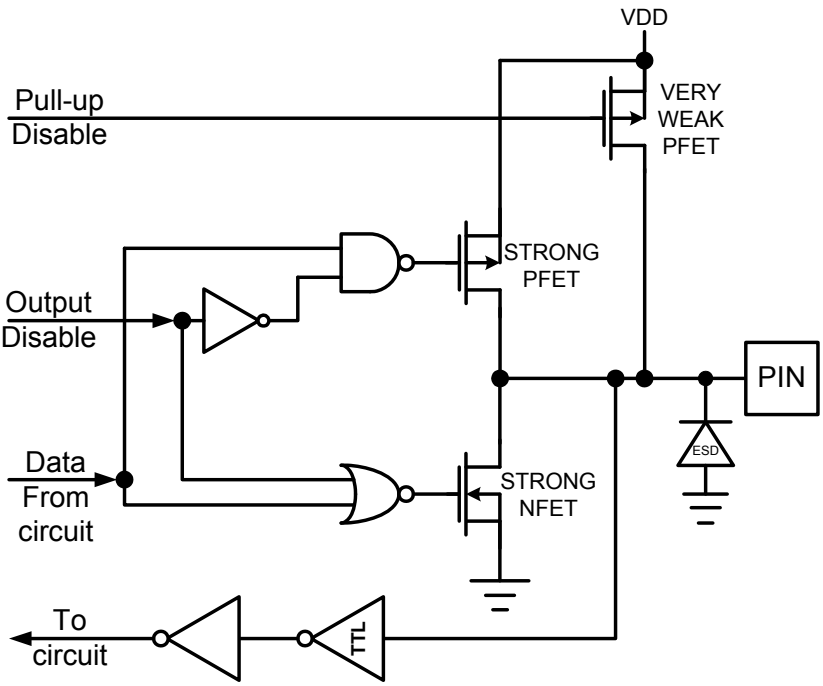



**Figure 31: Digital I/O with Pull Up Circuit**

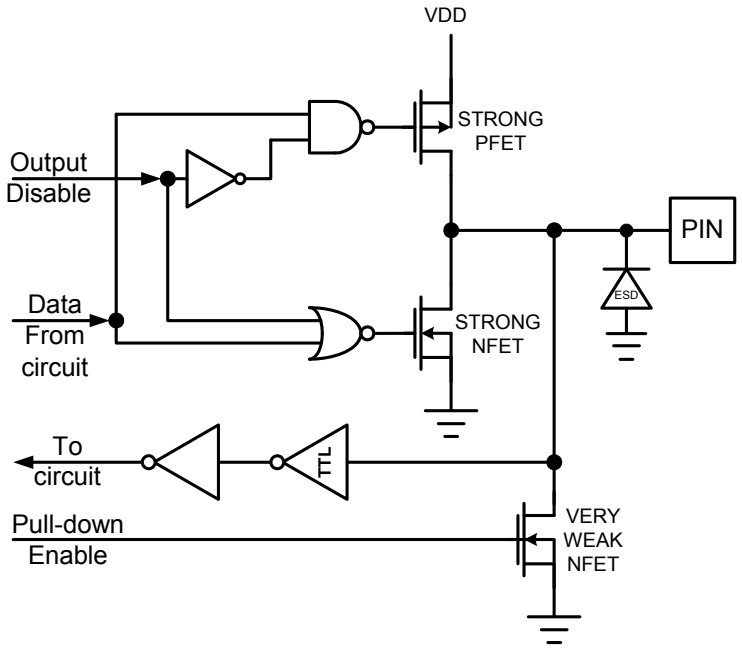



**Figure 32: Digital I/O with Pull-Down Circuit**

# 5 Package Pin Designation

## 5.1 68-pin QFN Pinout

CAUTION: Use handling procedures necessary for a static sensitive component.

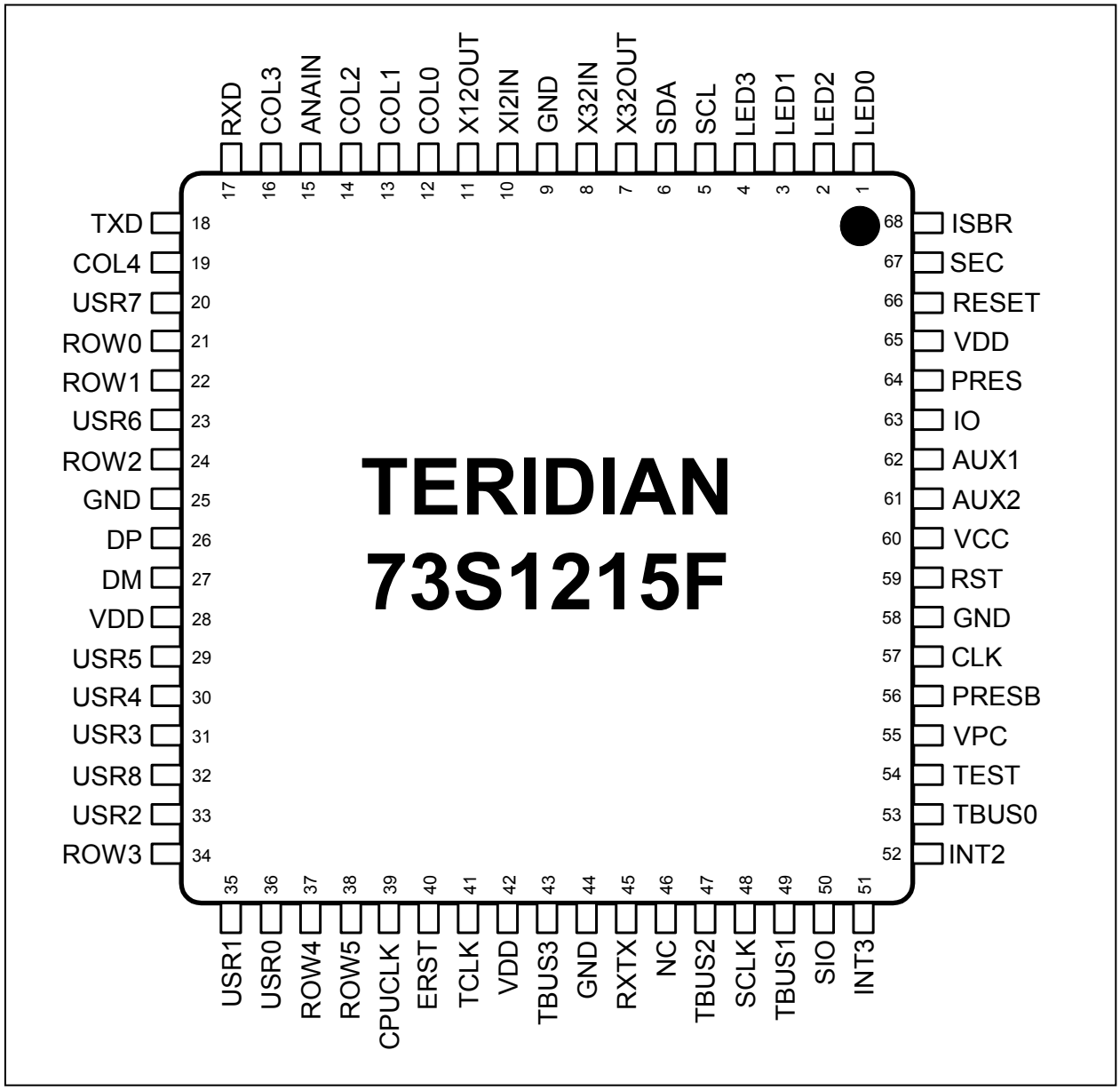



**Figure 44: 73S1215F 68 QFN Pinout**

# 6 Packaging Information

## 6.1 68-Pin QFN Package Outline

Notes: 6.3mm x 6.3mm exposed pad area must remain UNCONNECTED (clear of PCB traces or vias). Controlling dimensions are in mm.

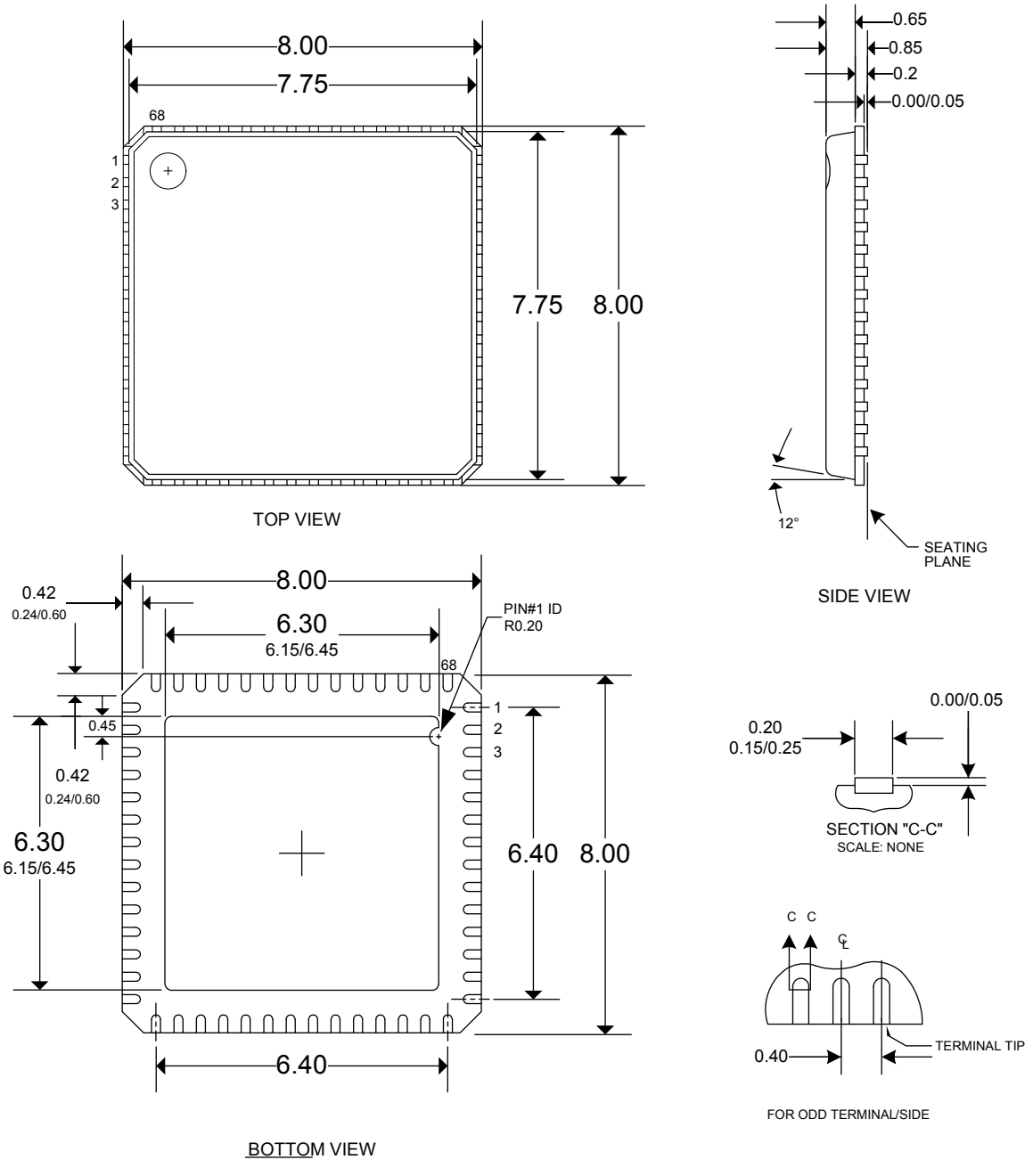



**Figure 46: 73S1215F 68 QFN Package Drawing**

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