Analog Devices Inc./Maxim Integrated - 73S1215F-44IM/F Datasheet

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	80515
Core Size	8-Bit
Speed	24MHz
Connectivity	I²C, SmartCard, UART/USART, USB
Peripherals	LED, POR, WDT
Number of I/O	9
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	44-VFQFN Exposed Pad
Supplier Device Package	44-QFN (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/analog-devices/73s1215f-44im-f

Figures

Program Status Word (PSW):

Table 9: PSW Register Flags

MSB							LSB
CV	AC	F0	RS1	RS	OV	–	P

Table 10: PSW Bit Functions

Bit	Symbol	Function
PSW.7	CV	Carry flag.
PSW.6	AC	Auxiliary Carry flag for BCD operations.
PSW.5	F0	General purpose Flag 0 available for user.
PSW.4	RS1	Register bank select control bits. The contents of RS1 and RS0 select the working register bank:
PSW.3	RS0	
PSW.2	OV	Overflow flag.
PSW.1	F1	General purpose Flag 1 available for user.
PSW.0	P	Parity flag, affected by hardware to indicate odd / even number of "one" bits in the Accumulator, i.e. even parity.

RS1/RS0	Bank Selected	Location
00	Bank 0	(0x00 – 0x07)
01	Bank 1	(0x08 – 0x0F)
10	Bank 2	(0x10 – 0x17)
11	Bank 3	(0x18 – 0x1F)

Stack Pointer (SP): The stack pointer is a 1-byte register initialized to 0x07 after reset. This register is incremented before PUSH and CALL instructions, causing the stack to begin at location 0x08.

Data Pointer: The data pointer (DPTR) is 2 bytes wide. The lower part is DPL, and the highest is DPH. It can be loaded as a 2-byte register (MOV DPTR,#data16) or as two registers (e.g. MOV DPL,#data8). It is generally used to access external code or data space (e.g. MOVC A,@A+DPTR or MOVX A,@DPTR respectively).

Program Counter: The program counter (PC) is 2 bytes wide initialized to 0x0000 after reset. This register is incremented during the fetching operation code or when operating on data from program memory. Note: The program counter is not mapped to the SFR area.

Port Registers: The I/O ports are controlled by Special Function Registers USR70, and USR8. The contents of the SFR can be observed on corresponding pins on the chip. Writing a 1 to any of the ports (see Table 11) causes the corresponding pin to be at high level (3.3V), and writing a 0 causes the corresponding pin to be held at low level (GND). The data direction registers UDIR70, and UDIR8 define individual pins as input or output pins (see the User (USR) Ports section for details).

External Interrupt Control Register (INT5Ctl): 0xFF94 ← 0x00

Table 15: The INT5Ctl Register

MSB							LSB
PDMUX	–	RTCIEN	RTCINT	USBIEN	USBINT	KPIEN	KPINT

Bit	Symbol	Function
INT5Ctl.7	PDMUX	When set = 1, enables interrupts from USB, RTC, Keypad (normally going to int5), Smart Card interrupts (normally going to int4), or USR(7:0) pins (int0) to cause interrupt on int0. The assertion of the interrupt to int0 is delayed by 512 MPU clocks to allow the analog circuits, including the clock system, to stabilize. This bit must be set prior to asserting the PWRDN bit in order to properly configure the interrupts that will wake up the circuit. This bit is reset = 0 when this register is read.
INT5Ctl.6	–	
INT5Ctl.5	RTCIEN	RTC interrupt enable.
INT5Ctl.4	RTCINT	RTC interrupt flag.
INT5Ctl.3	USBIEN	USB interrupt enable.
INT5Ctl.2	USBINT	USB interrupt flag.
INT5Ctl.1	KPIEN	Keypad interrupt enable.
INT5Ctl.0	KPINT	Keypad interrupt flag.

Miscellaneous Control Register 0 (MISCtl0): 0xFFF1 ← 0x00

Table 16: The MISCtl0 Register

MSB							LSB
PWRDN	–	–	–	–	–	SLPBK	SSEL

Bit	Symbol	Function
MISCtl0.7	PWRDN	This bit sets the circuit into a low-power condition. All analog (high speed oscillator and VCO/PLL) functions are disabled 32 MPU clock cycles after this bit is set = 1. This allows time for the next instruction to set the STOP bit in the PCON register to stop the CPU core. The RTC will stay active if it is set to operate from the 32kHz oscillator. The MPU is not operative in this mode. When set, this bit overrides the individual control bits that otherwise control power consumption.
MISCtl0.6	–	
MISCtl0.5	–	
MISCtl0.4	–	
MISCtl0.3	–	
MISCtl0.2	–	
MISCtl0.1	SLPBK	UART loop back testing mode.
MISCtl0.0	SSEL	Serial port pins select.

1.7.3 Interrupts

The 80515 core provides 10 interrupt sources with four priority levels. Each source has its own request flag(s) located in a special function register (TCON, IRCON, and SCON). Each interrupt requested by the corresponding flag can be individually enabled or disabled by the enable bits in SFRs IEN0, IEN1 and IEN2. Some of the 10 sources are multiplexed in order to expand the number of interrupt sources. These will be described in more detail in the respective sections.

External interrupts are the interrupts external to the 80515 core, i.e. signals that originate in other parts of the 73S1215F, for example the USB interface, USR I/O, RTC, smart card interface, analog comparators, etc. The external interrupt configuration is shown in Figure 8.

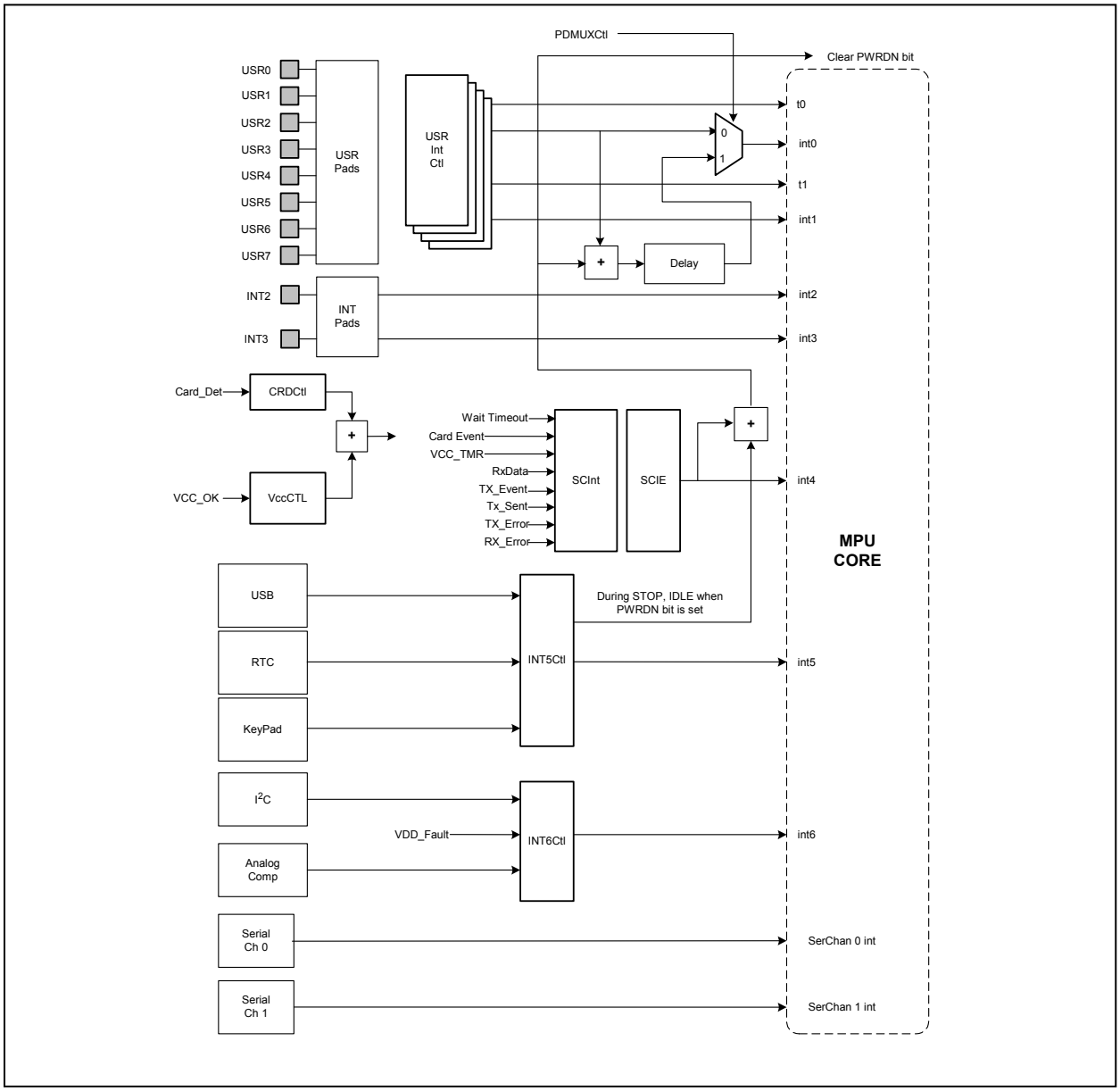

Figure 8: External Interrupt Configuration

1.7.3.1 Interrupt Overview

When an interrupt occurs, the MPU will vector to the predetermined address as shown in Table 33. Once the interrupt service has begun, it can only be interrupted by a higher priority interrupt. The interrupt service is terminated by a return from the REIT instruction. When a RETI is performed, the processor will return to the instruction that would have been next when the interrupt occurred.

When the interrupt condition occurs, the processor will also indicate this by setting a flag bit. This bit is set regardless of whether the interrupt is enabled or disabled. Each interrupt flag is sampled once per machine cycle, then samples are polled by the hardware. If the sample indicates a pending interrupt when the interrupt is enabled, then the interrupt request flag is set. On the next instruction cycle, the interrupt will be acknowledged by hardware forcing an LCALL to the appropriate vector address.

Interrupt response will require a varying amount of time depending on the state of the MPU when the interrupt occurs. If the MPU is performing an interrupt service with equal or greater priority, the new interrupt will not be invoked. In other cases, the response time depends on the current instruction. The fastest possible response to an interrupt is 7 machine cycles. This includes one machine cycle for detecting the interrupt and six cycles to perform the LCALL.

1.7.3.2 Special Function Registers for Interrupts

Interrupt Enable 0 Register (IEN0): 0xA8 ← 0x00

Table 20: The IEN0 Register

MSB LSB

EAL	WDT	–	ES0	ET1	EX1	ET0	EX0

Bit	Symbol	Function
IEN0.7	EAL	EAL = 0 – disable all interrupts.
IEN0.6	WDT	Not used for interrupt control.
IEN0.5	–	
IEN0.4	ES0	ES0 = 0 – disable serial channel 0 interrupt.
IEN0.3	ET1	ET1 = 0 – disable timer 1 overflow interrupt.
IEN0.2	EX1	EX1 = 0 – disable external interrupt 1.
IEN0.1	ET0	ET0 = 0 – disable timer 0 overflow interrupt.
IEN0.0	EX0	EX0 = 0 – disable external interrupt 0.

Power Control Register 0 (PCON): 0x87 ← 0x00

The SMOD bit used for the baud rate generator is set up via this register.

Table 36: The PCON Register

MSB LSB

SMOD	–	–	–	GF1	GF0	STOP	IDLE

Bit	Symbol	Function
PCON.7	SMOD	If SM0D = 1, the baud rate is doubled.
PCON.6	–	
PCON.5	–	
PCON.4	–	
PCON.3	GF1	General purpose flag 1.
PCON.2	GF0	General purpose flag 1.
PCON.1	STOP	Sets CPU to Stop mode.
PCON.0	IDLE	Sets CPU to Idle mode.

Baud Rate Control Register 0 (BRCON): 0xD8 ← 0x00

The BSEL bit used to enable the baud rate generator is set up via this register.

Table 37: The BRCON Register

MSB LSB

BSEL	–	–	–	–	–	–	–

Bit	Symbol	Function
BRCON.7	BSEL	If BSEL = 0, the baud rate is derived using timer 1. If BSEL = 1 the baud rate generator circuit is used.
BRCON.6	–	
BRCON.5	–	.
BRCON.4	–	
BRCON.3	–	
BRCON.2	–	
BRCON.1	–	
BRCON.0	–	

Serial Interface 0 Control Register (S0CON): 0x9B ← 0x00

Transmit and receive data are transferred via this register.

Table 39: The S0CON Register

MSB							LSB
SM0	SM1	SM20	REN0	TB80	RB80	TI0	RI0

Bit	Symbol	Function
S0CON.7	SM0	These two bits set the UART0 mode:
S0CON.6	SM1	
S0CON.5	SM20	Enables the inter-processor communication feature.
S0CON.4	REN0	If set, enables serial reception. Cleared by software to disable reception.
S0CON.3	TB80	The 9th transmitted data bit in Modes 2 and 3. Set or cleared by the MPU, depending on the function it performs (parity check, multiprocessor communication etc.).
S0CON.2	RB80	In Modes 2 and 3 it is the 9th data bit received. In Mode 1, if SM20 is 0, RB80 is the stop bit. In Mode 0 this bit is not used. Must be cleared by software.
S0CON.1	TI0	Transmit interrupt flag, set by hardware after completion of a serial transfer. Must be cleared by software.
S0CON.0	RI0	Receive interrupt flag, set by hardware after completion of a serial reception. Must be cleared by software.

Mode	Description	SM0	SM1
0	N/A	0	0
1	8-bit UART	0	1
2	9-bit UART	1	0
3	9-bit UART	1	1

1.7.4.2 Serial Interface 1

The Serial Interface 1 can operate in 2 modes:

- **Mode A**

  This mode is similar to Mode 2 and 3 of Serial interface 0, 11 bits are transmitted or received: a start bit (0), 8 data bits (LSB first), a programmable 9th bit, and a stop bit (1). The 9th bit can be used to control the parity of the serial interface: at transmission, bit TB81 in S1CON is outputted as the 9th bit, and at receive, the 9th bit affects RB81 in Special Function Register S1CON. The only difference between Mode 3 and A is that in Mode A only the internal baud rate generator can be use to specify baud rate.

- **Mode B**

  This mode is similar to Mode 1 of Serial interface 0. Pin RX serves as input, and TX serves as serial output. No external shift clock is used, 10 bits are transmitted: a start bit (always 0), 8 data bits (LSB first), and a stop bit (always 1). On receive, a start bit synchronizes the transmission, 8 data bits are available by reading S1BUF, and stop bit sets the flag RB81 in the Special Function Register S1CON. In mode 1, the internal baud rate generator is use to specify the baud rate.

The S1BUF register is used to read/write data to/from the serial 1 interface.

A 32-bit RTC counter is clocked by a selectable clock (1/2, 1, 2 second) to measure time. A trimming function is provided such that a trim value is accumulated in a 24-bit accumulator at the same rate as the RTC counter. The trim value is sign magnitude number. When the accumulator reaches overflow, it will advance the counter one additional count if the trim value is positive, or prevent the counter from advancing one count if the trim value is negative. This mechanism allows the RTC counter to be adjusted to keep accurate time with a minimum 0.5 second resolution. When using the high speed oscillator, the RTC counter wants to have an extra count added every 9375 seconds to keep the RTC counter at the proper time. If the one second RTC counter rate is used, the RTC Trim value should be set to 0x6FD (1789 decimal). This value is derived by taking the resolution of the 24 bit accumulator (2 ^ 24 = 16777216) and dividing this by 9375. This means the RTC accumulator will overflow every 9375 seconds and will cause the RTC counter to advance by 2 when the accumulator overflow occurs, thus bringing the RTC count to the proper time.

In addition to the basic software watchdog timer included in the 80515 MPU, an independent, robust, fixed-duration, hardware watchdog timer (WDT) is included with the 73S1215F RTC. The Watch Dog timer will give the MPU ½ second to respond to the RTC Interrupt. If the processor does not perform an RTC Interrupt service, a full RESET will be performed. The RTC interrupt is connected to the core interrupt "external interrupt 5" signal. The RTC interrupt must be enabled to obtain the watchdog timer function. Note: if the power down mode doesn't want the watchdog to wake up the MPU, the RTC interrupt should be masked before entering the power down mode.

Real Time Clock Control Register (RTCCtl) : 0x FFB0 ← 0x00

Table 55: The RTCCtl Register

MSB LSB

–	–	RTCLD	CTSEL.1	CTSEL.0	RINT.2	RINT.1	RINT.0

Bit	Symbol	Function
RTCCtl.7	–	
RTCCtl.6	–	
RTCCtl.5	RTCLD	When set, RTC parameters (RTC Count, RTC Accumulator, and RTC Trim) are loaded at the next 32kHz clock positive edge.
RTCCtl.4	CTSEL.1	Selects the time value that is counted by the real time clock: 0x – 1 second (default) 10 – ½ second 11 – 2 seconds
RTCCtl.3	CTSEL.0	
RTCCtl.2	RINT.2	RTC interrupt internal selection bits: (listed as bits 2,1,0) 100 – 0.5 second 0xx – 1 second (default) 101 – 2 seconds 110 – 4 seconds 111 – 8 seconds
RTCCtl.1	RINT.1	
RTCCtl.0	RINT.0	

I2C Secondary Read Data Register (SRDR): 0XFF84 ← 0x00

Table 67: The SRDR Register

MSB							LSB
SRDR.7	SRDR.6	SRDR.5	SRDR.4	SRDR.3	SRDR.2	SRDR.1	SRDR.0

Bit	Function
SRDR.7	Second Data byte to be read from the I^2C slave device if bit 0 (I2CLEN) of the Control and Status register (CSR) is set = 1.
SRDR.6	
SRDR.5	
SRDR.4	
SRDR.3	
SRDR.2	
SRDR.1	
SRDR.0	

I2C Control and Status Register (CSR): 0xFF85 ← 0x00

Table 68: The CSR Register

MSB							LSB
–	–	–	–	–	AKERR	I2CST	I2CLEN

Bit	Symbol	Function
CSR.7	–	
CSR.6	–	
CSR.5	–	
CSR.4	–	
CSR.3	–	
CSR.2	AKERR	Set to 1 if acknowledge bit from Slave Device is not 0. Automatically reset when the new bus transaction is started.
CSR.1	I2CST	Write a 1 to start I^2C transaction. Automatically reset to 0 when the bus transaction is done. This bit should be treated as a “busy” indicator on reading. If it is high, the serial read/write operations are not completed and no new address or data should be written.
CSR.0	I2CLEN	Set to 1 for 2-byte read or write operations. Set to 0 for 1-byte operations.

1.7.12 Keypad Interface

The 73S1215F supports a 30-button (6 row x 5 column) keypad (SPST Mechanical Contact Switches) interface using 11 dedicated I/O pins.

Figure 12 shows a simplified block diagram of the keypad interface.

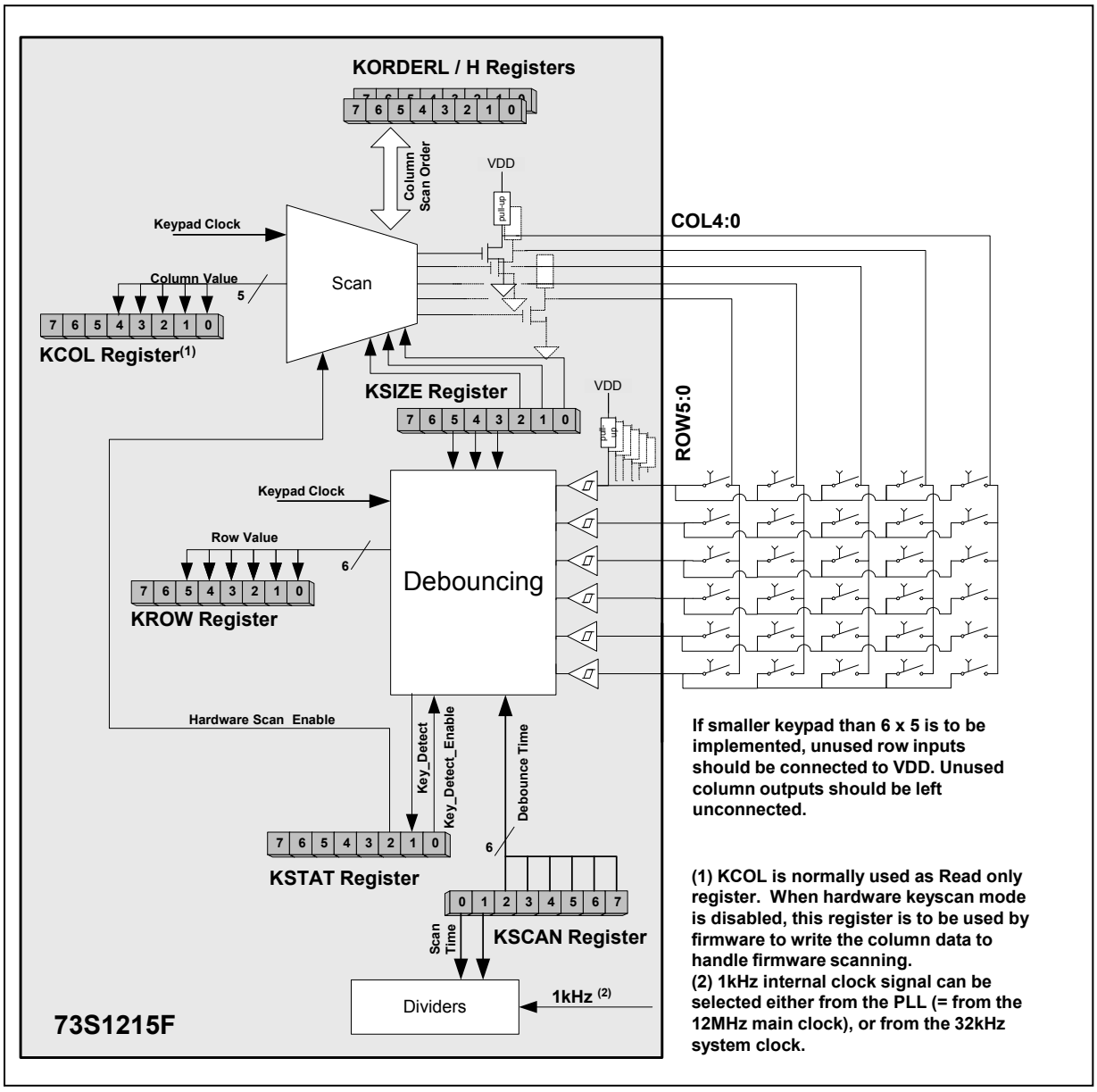

Figure 12: Simplified Keypad Block Diagram

There are 5 drive lines (outputs) corresponding to columns and 6 sense lines (inputs) corresponding to rows. Hysteresis and pull-ups are provided on all inputs (rows), which eliminate the need for external resistors in the keypad. Key scanning happens by asserting one of the 5 column lines low and looking for a low on a sense line indicating that a key is pressed (switch closed) at the intersection of the drive/sense (col/row) line in the keypad. Key detection is performed by hardware with an incorporated debounce timer. Debouncing time is adjustable through the KSCAN register. Internal hardware circuitry performs column scanning at an adjustable scanning rate and column scanning order through registers KSCAN and KORDERL / KORDERH. Key scanning is disabled at reset and must be enabled by firmware. When a valid key is detected, an interrupt is generated and the valid value of the pressed key is automatically written into KCOL and KROW registers. The keypad interface uses a 1kHz clock derived from either the

Keypad Column Register (KCOL): 0xD1 ← 0x1F

This register contains the value of the column of a key detected as valid by the hardware. In bypass mode, this register firmware writes directly this register to carry out manual scanning.

Table 70: The KCOL Register

MSB							LSB
–	–	–	COL.4	COL.3	COL.2	COL.1	COL.0

Bit	Symbol	Function
KCOL.7	–	
KCOL.6	–	
KCOL.5	–	
KCOL.4	COL.4	Drive lines bit mapped to corresponding with pins COL(4:0). When a key is detected, firmware reads this register to determine column. In bypass (S/W keyscan) mode, Firmware writes this register directly. 0x1E = COL(0) low, all others high. 0x0F = COL(4) low, all others high. 0x1F = COL(4:0) all high.
KCOL.3	COL.3	
KCOL.2	COL.2	
KCOL.1	COL.1	
KCOL.0	COL.0	

Keypad Row Register (KROW): 0xD2 ← 0x3F

This register contains the value of the row of a key detected as valid by the hardware. In bypass mode, this register firmware reads directly this register to carry out manual detection.

Table 71: The KROW Register

MSB							LSB
–	–	ROW.5	ROW.4	ROW.3	ROW.2	ROW.1	ROW.0

Bit	Symbol	Function
KROW.7	–	
KROW.6	–	
KROW.5	ROW.6	Sense lines bit mapped to correspond with pins ROW(5:0). When key detected, firmware reads this register to determine row. In bypass mode, firmware reads rows and has to determine if there was a key press or not. 0x3E = ROW(0) low, all others high. 0x1F = ROW(5) low, all others high. 0x3F = ROW(5:0) all high.
KROW.4	ROW.4	
KROW.3	ROW.3	
KROW.2	ROW.2	
KROW.1	ROW.1	
KROW.0	ROW.0	

Keypad Scan Time Register (KSIZE): 0xD5 ← 0x00

This register is not applicable when HWSCEN is not set. Unused row inputs should be connected to VDD.

Table 74: The KSIZE Register

MSB							LSB
–	–	ROWSIZ.2	ROWSIZ.1	ROWSIZ.0	COLSIZ.2	COLSIZ.1	COLSIZ.0

Bit	Symbol	Function
KSIZE.7	–	
KSIZE.6	–	
KSIZE.5	ROWSIZ.2	Defines the number of rows in the keypad. Maximum number is 6 given the number of row pins on the package. Allows for a reduced keypad size for scanning.
KSIZE.4	ROWSIZ.1	
KSIZE.3	ROWSIZ.0	
KSIZE.2	COLSIZ.2	Defines the number of columns in the keypad. Maximum number is 5 given the number of column pins on the package. Allows for a reduced keypad size for scanning.
KSIZE.1	COLSIZ.1	
KSIZE.0	COLSIZ.0	

Keypad Column LS Scan Order Register (KORDERL): 0xD6 ← 0x00

In registers KORDERL and KORDERH, Column Scan Order(14:0) is grouped into 5 sets of 3 bits each. Each set determines which column (COL(4:0) pin) to activate by loading the column number into the 3 bits. When in HW_Scan_Enable mode, the hardware will step through the sets from 1Col to 5Col (up to the number of columns in Colsize) and scan the column defined in the 3 bits. To scan in sequential order, set a counting pattern with 0 in set 0, and 1 in set 1,and 2 in set 2, and 3 in set 3, and 4 in set 4. The firmware should update this as part of the interrupt service routine so that the new scan order is loaded prior to the next key being pressed. For example, to scan COL(0) first, 1Col(2:0) should be loaded with 000'b. To scan COL(4) fifth, 5Col(2:0) should be loaded with 100'b.

Table 75: The KORDERL Register

MSB							LSB
3COL.1	3COL.0	2COL.2	2COL.1	2COL.0	1COL.2	1COL.1	1COL.0

Bit	Symbol	Function
KORDERL.7	3COL.1	Column to scan 3rd (lsb's).
KORDERL.6	3COL.0	
KORDERL.5	2COL.2	Column to scan 2nd.
KORDERL.4	2COL.1	
KORDERL.3	2COL.0	
KORDERL.2	1COL.2	Column to scan 1st.
KORDERL.1	1COL.1	
KORDERL.0	1COL.0	

Smart Card SFRs

Smart Card Select Register (SCSel): 0xFE00 ← 0x00

Table 80: The SCSel Register

MSB							LSB
–	–	–	–	SELSC.1	SELSC.0	BYPASS	–

The smart card select register is used to determine which smart card interface is using the ISO UART. The internal Smart Card has integrated 7816-3 compliant sequencer circuitry to drive an external smart card interface. The external smart card interface relies on 73S8010x parts to generate the ISO 7816-3 compatible signals and sequences. Multiple 73S8010x devices can be connected to the external smart card interface.

Table 81: The SCSel Bit Functions

Bit	Symbol	Function
SCSel.7	–	
SCSel.6	–	
SCSel.5	–	
SCSel.4	–	
SCSel.3	SELSC.1	Select Smart Card Interface – These bits select the interface that is using the IS0 UART. These bits do not activate the interface. Activation is performed by the VccCtl register. 00 = No smart card interface selected. 01 = External Smart Card Interface selected (using SCLK, SIO). 1X = Internal Smart Card Interface selected.
SCSel.2	SELSC.0	
SCSel.1	BYPASS	1 = Enabled, 0 = Disabled. When enabled, ISO UART is bypassed and the I/O line is controlled via the SCCtl and SCECtl registers.
SCSel.0	–	

Parity Control Register (SParCtl): 0xFE11 ← 0x00

This register provides the ability to configure the parity circuitry on the smart card interface. The settings apply to both integrated smart card interfaces.

Table 96: The SParCtl Register

MSB LSB

–	DISPAR	BRKGEN	BRKDET	RETRAN	DISCRX	INSPE	FORCPE

Bit	Symbol	Function
SParCtl.7	–	
SParCtl.6	DISPAR	Disable Parity Check – 1 = disabled, 0 = enabled. If enabled, the UART will check for even parity (the number of 1's including the parity bit is even) on every character. This also applies to the TS during ATR.
SParCtl.5	BRKGEN	Break Generation Disable – 1 = disabled, 0 = enabled. If enabled, and T=0 protocol, the UART will generate a Break to the smart card if a parity error is detected on a receive character. No Break will be generated if parity checking is disabled. This also applies to TS during ATR.
SParCtl.4	BRKDET	Break Detection Disable – 1 = disabled, 0 = enabled. If enabled, and T=0 protocol, the UART will detect the generation of a Break by the smart card.
SParCtl.3	RETRAN	Retransmit Byte – 1 = enabled, 0 = disabled. If enabled and a Break is detected from the smart card (Break Detection must be enabled), the last character will be transmitted again. This bit applies to T=0 protocol.
SParCtl.2	DISCRX	Discard Received Byte – 1 = enabled, 0 = disabled. If enabled and a parity error is detected (Parity checking must be enabled), the last character received will be discarded. This bit applies to T=0 protocol.
SParCtl.1	INSPE	Insert Parity Error – 1 = enabled, 0 = disabled. Used for test purposes. If enabled, the UART will insert a parity error in every character transmitted by generating odd parity instead of even parity for the character.
SParCtl.0	FORCPE	Force Parity Error – 1 = enabled, 0 = disabled. Used for test purposes. If enabled, the UART will generate a parity error on a character received from the smart card.

Parameter		Condition	Min	Typ.	Max	Unit
C_L = 50pf, series 24Ω, 1% source termination resistor included						
Rise Time	USBTR	10% to 90%	4		20	ns
Fall Time	USBTF	90% to 10%	4		20	ns
Rise/fall time matching	TRFM	(USBTR/USBTF)	90		111.11	%
Output signal crossover voltage	VCRS	Includes VDI range	1.3		2.0	V
Source Jitter to Next Transition	TDJ1	Measured as in Figure 7-49 of USB 2.0 Spec	-3.5		3.5	ns
Source Jitter For Paired Transitions	TDJ2	Measured as in Figure 7-49 of USB 2.0 Spec (1) (2)	-4		4	ns
Receiver Jitter to Next Transition	TJR1	Measure as in Figure 7-51 of USB 2.0 Spec. Characterized but not production tested.	-18.5		18.5	ns
Receiver Jitter for Paired Transitions	TJR2	Measure as in Figure 7-51 of USB 2.0 Spec. Characterized but not production tested.	-9		9	ns
Source SE0 interval of EOP	TEOPT	Figure 7-50 of USB 2.0 Spec	160		175	ns
Receiver SEO interval of EOP	TEOPR	Figure 7-50 of USB 2.0 Spec. (3)	82			ns

(1) For both transitions of differential signaling.
(2) Excluding first transition from the Idle state.
(3) Must accept as valid EOP.

Symbol	Parameter	Condition	Min	Typ.	Max	Unit
Interface Requirements – Data Signals: I/O, AUX1 and AUX2						
V_{OH}	Output level, high (I/O, AUX1, AUX2)	I_{OH} =0	0.9 * V_{CC}		V_{CC}+0.1	V
		I_{OH} = -40μA	0.75 V_{CC}		V_{CC}+0.1	V
V_{OL}	Output level, low (I/O, AUX1, AUX2)	I_{OL}=1mA			0.15 *V_{CC}	V
V_{IH}	Input level, high (I/O, AUX1, AUX2)		0.6 * V_{CC}		V_{CC}+0.30	V
V_{IL}	Input level, low (I/O, AUX1, AUX2)		-0.15		0.2 * V_{CC}	V
V_{INACT}	Output voltage when outside of session	I_{OL} = 0			0.1	V
		I_{OL} = 1mA			0.3	V
I_{LEAK}	Input leakage	V_{IH} = V_{CC}			10	μA
I_{IL}	Input current, low (I/O, AUX1, AUX2)	V_{IL} = 0			0.65	mA
I_{SHORTL}	Short circuit output current	For output low, shorted to V_{CC} through 33Ω			15	mA
I_{SHORTH}	Short circuit output current	For output high, shorted to ground through 33Ω			15	mA
t_R, t_F	Output rise time, fall times	For I/O, AUX1, AUX2, C_L = 80pF, 10% to 90%.			100	ns
t_{IR}, t_{IF}	Input rise, fall times				1	μs
R_{PU}	Internal pull-up resistor	Output stable for >200ns	8	11	14	kΩ
FD_{MAX}	Maximum data rate				1	MHz
Reset and Clock for Card Interface, RST, CLK						
V_{OH}	Output level, high	I_{OH} =-200μA	0.9 * V_{CC}		V_{CC}	V
V_{OL}	Output level, low	I_{OL}=200μA	0		0.15 *V_{CC}	V
V_{INACT}	Output voltage when outside of session	I_{OL} = 0			0.1	V
		I_{OL} = 1mA			0.3	V
I_{RST_LIM}	Output current limit, RST				30	
I_{CLK_LIM}	Output current limit, CLK				70	mA
CLK_{SR3V}	CLK slew rate	V_{CC} = 3V	0.3			V/ns
CLK_{SR5V}	CLK slew rate	V_{CC} = 5V	0.5			V/ns
t_R, t_F	Output rise time, fall time	C_L = 35pF for CLK, 10% to 90%			8	ns
		C_L = 200pF for RST, 10% to 90%			100	ns
δ	Duty cycle for CLK	C_L =35pF, F_{CLK} ≤ 20MHz	45		55	%

3.7.1 DC Characteristics

Symbol	Parameter	Condition	Min	Typ.	Max	Unit
I_{DD}	Supply Current	CPU clock @ 24MHz		30	35	mA
		CPU clock @ 12MHz		22	25.5	mA
		CPU clock @ 6MHz		16	19.5	mA
		CPU clock @ 3.69MHz		14	17	mA
		Power down (-40□ to 85□C)		8	50	μA
		Power down (25□C)		6	13	μA
I_{PC}	Supply Current	V_{CC} on, ICC=0 I/O, AUX1, AUX2=high, CLK not toggling		450	650	μA
		Power down		1	10	
I_{PCOFF}	V_{PC} supply current when V_{CC} = 0	Smart card deactivated		345		μA

3.8 Voltage / Temperature Fault Detection Circuits

Symbol	Parameter	Condition	Min	Typ.	Max	Unit
V_{PCF}	V_{PC} fault (V_{PC} Voltage supervisor threshold)	V_{PC}<V_{CC}, a transient event		V_{CC} > V_{PC} + 0.3		V
V_{CCF}	VCCOK = 0 (V_{CC} Voltage supervisor threshold)	V_{CC} = 5V			4.6	V
		V_{CC}= 3V			2.7	V
		V_{CC}= 1.8V			1.65	
T_F	Die over temperature fault		115		145	°C
ICCF	Vcc over current fault		110			mA

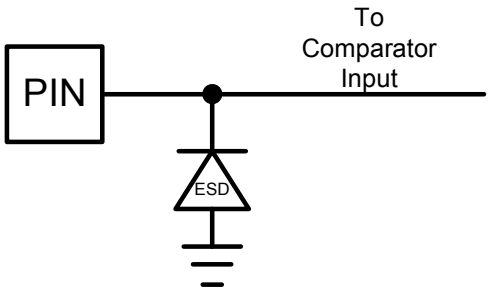

Figure 38: Analog Input Circuit

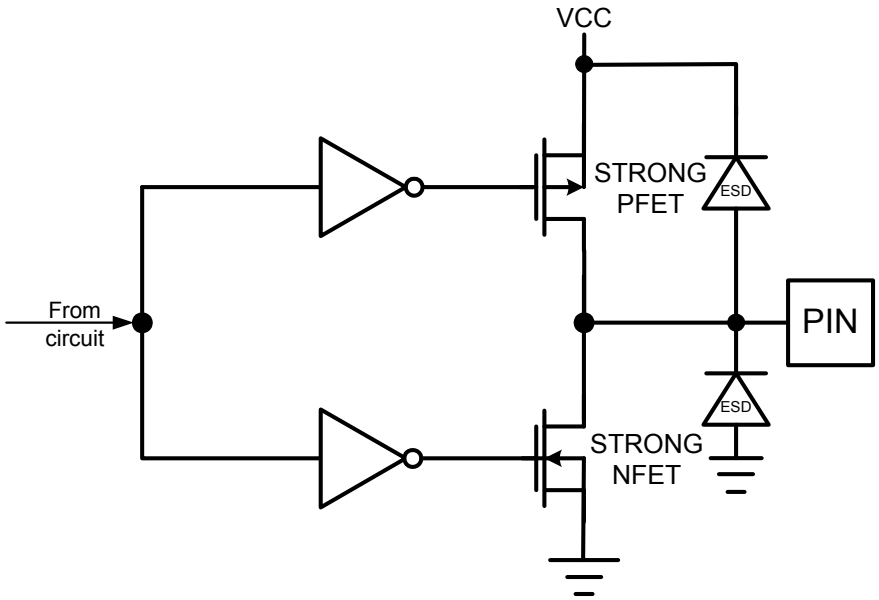

Figure 39: Smart Card Output Circuit

6 Packaging Information

6.1 68-Pin QFN Package Outline

Notes: 6.3mm x 6.3mm exposed pad area must remain UNCONNECTED (clear of PCB traces or vias). Controlling dimensions are in mm.

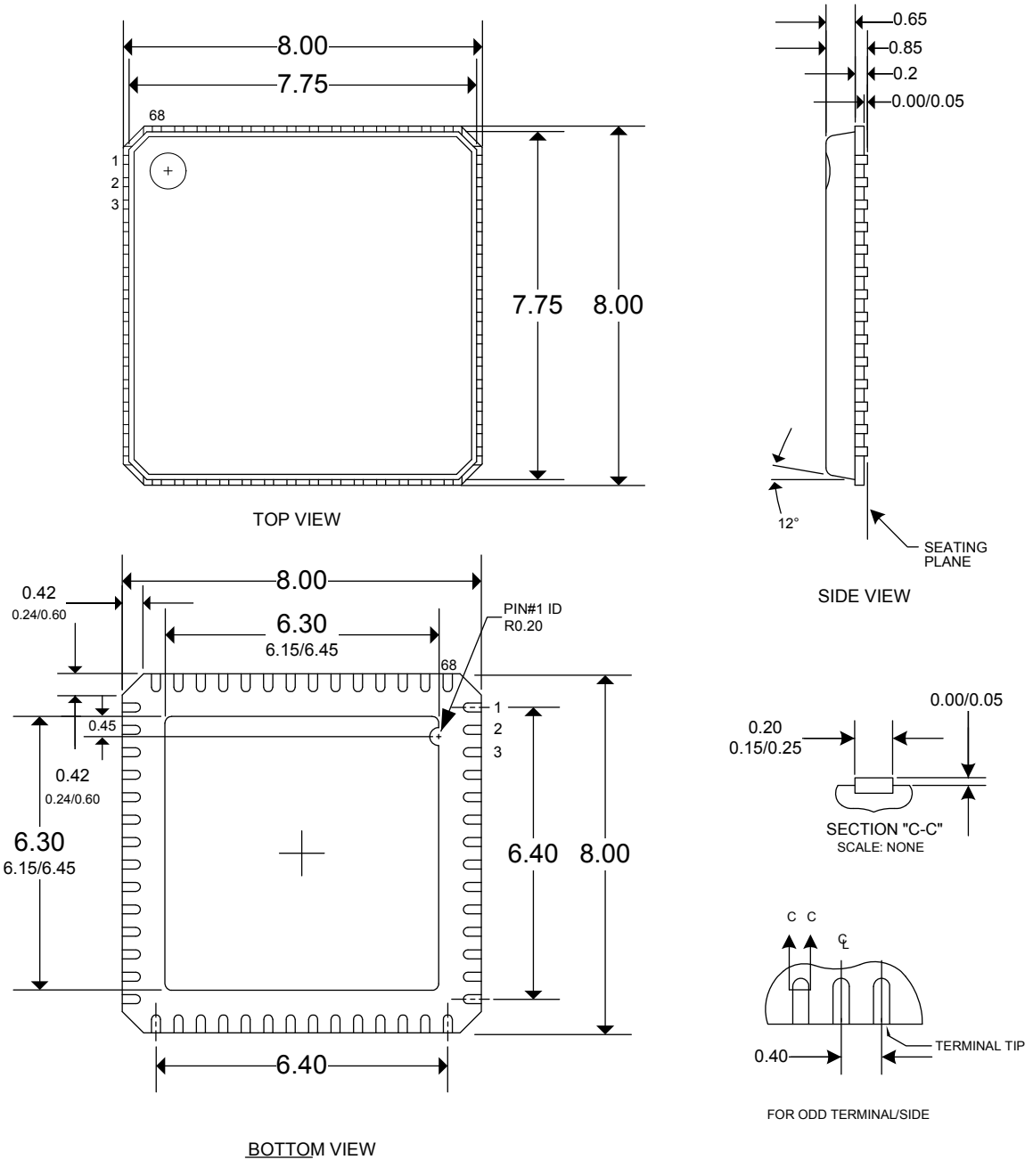

Figure 46: 73S1215F 68 QFN Package Drawing

1.4	12/16/2008	In Table 1, added more description to the VCC, VPC, VDD, SCL, SDA, PRES, SEC and TEST pins. In Section 1.3.2, changed "FLSH_ERASE" to "ERASE" and "FLSH_PGADR" to "PGADDR". Added "The PGADDR register denotes the page address for page erase. The page size is 512 (200h) bytes and there are 128 pages within the flash memory. The PGADDR denotes the upper seven bits of the flash memory address such that bit 7:1 of the PGADDR corresponds to bit 15:9 of the flash memory address. Bit 0 of the PGADDR is not used and is ignored." In the description of the PGADDR register, added "Note: the page address is shifted left by one bit (see detailed description above)." Changed the register address for ATRMsB from FE21 to FE1F. In Table 5, changed "FLSHCRL" to "FLSHCTL". In Table 5, moved the TRIMPCtl bit description to FUSECtl and moved the FUSECtl bit description to TRIMPCtl. In Table 6, changed "PGADR" to "PGADDR". In Table 7, added PGADDR. In Table 8, changed the reset value for RTCCtl from "0x81" to "0x00". Added the RTCTrim0 and ACOMP registers. Deleted the OMP, VRCtl, LEDCal and LOCKCtl registers. In Table 23, corrected the descriptions for TCON.2 and TCON.0. In Table 62, added "Write data controls output level of pin LEDn. Read will report level of pin LEDn." to the description of LEDD3, LEDD2 and LEDD1. In Section 1.7.15.5 (number 3), deleted "If CLKOFF/SCLKOFF is high and SYCKST is set=1(STXCtl, b7=1), Rlen=max will stop the clock at the selected (CLKLVL or SCLKLVL) level." In Section 1.7.15.5, added "Synchronous card operation is broken down into three primary types. These are commonly referred to as 2-wire, 3-wire and I2C synchronous cards. Each card type requires different control and timing and therefore requires different algorithms to access. Teridian has created an application note to provide detailed algorithms for each card type. Refer to the application note titled *73S12xxF Synchronous Card Design Application Note*." In the VccVtl.0 bit description, deleted "When in power down mode, V_{DD} = 0V. V_{DD} can only be turned on by pressing the ON/OFF switch or by application of 5V to V_{BUS}. If V_{BUS} power is available and SCPWRDN bit is set, it has no effect until V_{BUS} is removed and V_{DD} will shut off." In Table 86 and Table 117, changed the SYCKST bit to I2CMODE. In Figure 26, replaced the schematic with a new schematic. Added Section 6, Ordering Information. Added Section 7, Related Documentation. Added Section 8, Contact Information. Formatted the document per new standard. Added section numbering.