Analog Devices Inc./Maxim Integrated - 73S1215F-44IMR/F/P Datasheet

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Details	
Product Status	Discontinued at Digi-Key
Core Processor	80515
Core Size	8-Bit
Speed	24MHz
Connectivity	I²C, SmartCard, UART/USART, USB
Peripherals	LED, POR, WDT
Number of I/O	9
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	44-VFQFN Exposed Pad
Supplier Device Package	44-QFN (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/analog-devices/73s1215f-44imr-f-p

1 Hardware Description

1.1 Pin Description

Table 1: 73S1215F Pinout Description

Pin Name	Pin (68 Qfn)	Pin (44 Qfn)	Type	Equivalent Circuit*	Description
X12IN	10	8	I	Figure 27	MPU/USB clock crystal oscillator input pin. A 12MHz crystal is required for USB operation. A 1MΩ resistor is required between pins X12IN and X12OUT.
X12OUT	11	9	O	Figure 27	MPU/USB clock crystal oscillator output pin.
X32IN	8		I	Figure 28	RTC clock crystal oscillator input pin. A 32768Hz crystal is required for low-power RTC operation.
X32OUT	7		O	Figure 28	RTC clock crystal oscillator output pin.
CPUCLK	39		O	Figure 30	Output signal, square wave at the frequency of the MPU clock.
DP	26	16	IO	Figure 43	USB D+ IO pin, requires series 24Ω resistor.
DM	27	17	IO	Figure 43	USB D- IO pin, requires series 24Ω resistor.
ROW(5:0) 0 1 2 3 4 5	 21 22 24 34 37 38		I	Figure 34	Keypad row input sense.
COL(4:0) 0 1 2 3 4	 12 13 14 16 19		O	Figure 35	Keypad column output scan pins.
USR(8:0) 0 1 2 3 4 5 6 7 8	 36 35 33 31 30 29 23 20 32	 24 23 22 21 20 19 14 13	IO	Figure 31	General-purpose user pins, individually configurable as inputs or outputs or as external input interrupt ports.
SCL	5	5	O	Figure 30	I^2C (master mode) compatible Clock signal. Note: the pin is configured as an open drain output. When the I2C interface is being used, an external pull up resistor is required. A value of 3K is recommended.
SDA	6	6	IO	Figure 29	I^2C (master mode) compatible data I/O. Note: this pin is bi-directional. When the pin is configured as output, it is an open drain output. When the I2C interface is being used, an external pull up resistor is required. A value of 3K is recommended.

1.2 Hardware Overview

The Teridian 73S1215F single smart card controller integrates all primary functional blocks required to implement a smart card reader. Included on chip are an 8051-compatible microprocessor (MPU) which executes up to one instruction per clock cycle (80515), a fully integrated IS0-7816 compliant smart card interface, expansion smart card interface, full speed USB 2.0 compatible interface, serial interface, I2C interface, 6 x 5 keypad interface, 4 LED drivers, RAM, FLASH memory, a real time clock (RTC), and a variety of I/O pins. Figure 1 shows a functional block diagram of the 73S1215F.

1.3 80515 MPU Core

1.3.1 80515 Overview

The 73S1215F includes an 80515 MPU (8-bit, 8051-compatible) that performs most instructions in one clock cycle. The 80515 architecture eliminates redundant bus states and implements parallel execution of fetch and execution phases. Normally a machine cycle is aligned with a memory fetch, therefore, most of the 1-byte instructions are performed in a single cycle. This leads to an 8x performance (average) improvement (in terms of MIPS) over the Intel 8051 device running at the same clock frequency.

Actual processor clocking speed can be adjusted to the total processing demand of the application (cryptographic calculations, key management, memory management, and I/O management) using the XRAM special function register MPUCKCtl.

Typical smart card, USB, serial, keyboard, I2C, and RTC management functions are available for the MPU as part of the Teridian standard library. A standard ANSI “C” 80515-application programming interface library is available to help reduce design cycle. Refer to the *73S12xxF Software User’s Guide*.

1.3.2 Memory Organization

The 80515 MPU core incorporates the Harvard architecture with separate code and data spaces. Memory organization in the 80515 is similar to that of the industry standard 8051. There are three memory areas: Program memory (Flash), external data memory (XRAM), and internal data memory (IRAM). Data bus address space is allocated to on-chip memory as shown Table 2.

Table 2: MPU Data Memory Map

Address (hex)	Memory Technology	Memory Type	Typical Usage	Memory Size (bytes)
0000-FFFF	Flash Memory	Non-volatile	Program and non-volatile data	64KB
0000-07FF	Static RAM	Volatile	MPU data XRAM	2KB
FC00-FFFF	External SFR	Volatile	Peripheral control	1KB

Note: The IRAM is part of the core and is addressed differently.

Program Memory: The 80515 can address up to 64KB of program memory space from 0x0000 to 0xFFFF. Program memory is read when the MPU fetches instructions or performs a MOVC operation. After reset, the MPU starts program execution from location 0x0000. The lower part of the program memory includes reset and interrupt vectors. The interrupt vectors are spaced at 8-byte intervals, starting from 0x0003 (Reset is located at 0x0000).

Flash Memory: The program memory consists of flash memory. The flash memory is intended to primarily contain MPU program code. Flash erasure is initiated by writing a specific data pattern to specific SFR registers in the proper sequence. These special pattern/sequence requirements prevent inadvertent erasure of the flash memory.

Table 3: Flash Special Function Registers

Register	SFR Address	R/W	Description
ERASE	0x94	W	This register is used to initiate either the Flash Mass Erase cycle or the Flash Page Erase cycle. Specific patterns are expected for ERASE in order to initiate the appropriate Erase cycle (default = 0x00). 0x55 – Initiate Flash Page Erase cycle. Must be proceeded by a write to PGADDR @ SFR 0xB7. 0xAA – Initiate Flash Mass Erase cycle. Must be proceeded by a write to FLSH_MEEN @ SFR 0xB2 and the debug port must be enabled. Any other pattern written to ERASE will have no effect.
PGADDR	0xB7	R/W	Flash Page Erase Address register containing the flash memory page address (page 0 through 127) that will be erased during the Page Erase cycle (default = 0x00). Note: the page address is shifted left by one bit (see detailed description above). Must be re-written for each new Page Erase cycle.
FLSHCTL	0xB2	R/W	Bit 0 (FLSH_PWE): Program Write Enable: 0 – MOVX commands refer to XRAM Space, normal operation (default). 1 – MOVX @DPTR,A moves A to Program Space (Flash) @ DPTR. This bit is automatically reset after each byte written to flash. Writes to this bit are inhibited when interrupts are enabled.
		W	Bit 1 (FLSH_MEEN): Mass Erase Enable: 0 – Mass Erase disabled (default). 1 – Mass Erase enabled. Must be re-written for each new Mass Erase cycle.
		R/W	Bit 6 (SECURE): Enables security provisions that prevent external reading of flash memory and CE program RAM. This bit is reset on chip reset and may only be set. Attempts to write zero are ignored.

Internal Data Memory: The Internal data memory provides 256 bytes (0x00 to 0xFF) of data memory. The internal data memory address is always one byte wide and can be accessed by either direct or indirect addressing. The Special Function Registers occupy the upper 128 bytes**. This SFR area is available only by direct addressing. Indirect addressing accesses the upper 128 bytes of Internal RAM.**

The lower 128 bytes contain working registers and bit-addressable memory. The lower 32 bytes form four banks of eight registers (R0-R7). Two bits on the program memory status word (PSW) select which bank is in use. The next 16 bytes form a block of bit-addressable memory space at bit addresses 0x00-0x7F. All of the bytes in the lower 128 bytes are accessible through direct or indirect addressing. Table 4 shows the internal data memory map.

Table 4: Internal Data Memory Map

<table>
<tr><th>Address</th><th>Direct Addressing</th><th>Indirect Addressing</th></tr>
<tr><td>0xFF</td><td rowspan="2">Special Function Registers (SFRs)</td><td rowspan="2">RAM</td></tr>
<tr><td>0x80</td></tr>
<tr><td>0x7F</td><td colspan="2" rowspan="2">Byte-addressable area</td></tr>
<tr><td>0x30</td></tr>
<tr><td>0x2F</td><td colspan="2" rowspan="2">Byte or bit-addressable area</td></tr>
<tr><td>0x20</td></tr>
<tr><td>0x1F</td><td colspan="2" rowspan="2">Register banks R0…R7 (x4)</td></tr>
<tr><td>0x00</td></tr>
</table>

External Data Memory: While the 80515 can address up to 64KB of external data memory in the space from 0x0000 to 0xFFFF, only the memory ranges shown in Figure 2 contain physical memory. The 80515 writes into external data memory when the MPU executes a MOVX @Ri,A or MOVX @DPTR,A instruction. The MPU reads external data memory by executing a MOVX A,@Ri or MOVX A,@DPTR instruction.

There are two types of instructions, differing in whether they provide an eight-bit or sixteen-bit indirect address to the external data RAM.

In the first type (MOVX A,@Ri), the contents of R0 or R1, in the current register bank, provide the eight lower-ordered bits of address. This method allows the user access to the first 256 bytes of the 2KB of external data RAM. In the second type of MOVX instruction (MOVX A,@DPTR), the data pointer generates a sixteen-bit address.

Name	Location	Reset Value	Description
TRIMPCtl	0x FFD1	0x00	TRIM Pulse Control
FUSECtl	0x FFD2	0x00	FUSE Control
VDDFCtl	0x FFD4	0x00	VDDFault Control
SECReg	0x FFD7	0x00	Security Register
MISCtl0	0x FFF1	0x00	Miscellaneous Control Register 0
MISCtl1	0x FFF2	0x10	Miscellaneous Control Register 1
LEDCtl	0x FFF3	0xFF	LED Control Register

Accumulator (ACC, A): ACC is the accumulator register. Most instructions use the accumulator to hold the operand. The mnemonics for accumulator-specific instructions refer to accumulator as “A”, not ACC.

B Register: The B register is used during multiply and divide instructions. It can also be used as a scratch-pad register to hold temporary data.

External Interrupt Control Register (INT5Ctl): 0xFF94 ← 0x00

Table 15: The INT5Ctl Register

MSB							LSB
PDMUX	–	RTCIEN	RTCINT	USBIEN	USBINT	KPIEN	KPINT

Bit	Symbol	Function
INT5Ctl.7	PDMUX	When set = 1, enables interrupts from USB, RTC, Keypad (normally going to int5), Smart Card interrupts (normally going to int4), or USR(7:0) pins (int0) to cause interrupt on int0. The assertion of the interrupt to int0 is delayed by 512 MPU clocks to allow the analog circuits, including the clock system, to stabilize. This bit must be set prior to asserting the PWRDN bit in order to properly configure the interrupts that will wake up the circuit. This bit is reset = 0 when this register is read.
INT5Ctl.6	–	
INT5Ctl.5	RTCIEN	RTC interrupt enable.
INT5Ctl.4	RTCINT	RTC interrupt flag.
INT5Ctl.3	USBIEN	USB interrupt enable.
INT5Ctl.2	USBINT	USB interrupt flag.
INT5Ctl.1	KPIEN	Keypad interrupt enable.
INT5Ctl.0	KPINT	Keypad interrupt flag.

Miscellaneous Control Register 0 (MISCtl0): 0xFFF1 ← 0x00

Table 16: The MISCtl0 Register

MSB							LSB
PWRDN	–	–	–	–	–	SLPBK	SSEL

Bit	Symbol	Function
MISCtl0.7	PWRDN	This bit sets the circuit into a low-power condition. All analog (high speed oscillator and VCO/PLL) functions are disabled 32 MPU clock cycles after this bit is set = 1. This allows time for the next instruction to set the STOP bit in the PCON register to stop the CPU core. The RTC will stay active if it is set to operate from the 32kHz oscillator. The MPU is not operative in this mode. When set, this bit overrides the individual control bits that otherwise control power consumption.
MISCtl0.6	–	
MISCtl0.5	–	
MISCtl0.4	–	
MISCtl0.3	–	
MISCtl0.2	–	
MISCtl0.1	SLPBK	UART loop back testing mode.
MISCtl0.0	SSEL	Serial port pins select.

1.7.3 Interrupts

The 80515 core provides 10 interrupt sources with four priority levels. Each source has its own request flag(s) located in a special function register (TCON, IRCON, and SCON). Each interrupt requested by the corresponding flag can be individually enabled or disabled by the enable bits in SFRs IEN0, IEN1 and IEN2. Some of the 10 sources are multiplexed in order to expand the number of interrupt sources. These will be described in more detail in the respective sections.

External interrupts are the interrupts external to the 80515 core, i.e. signals that originate in other parts of the 73S1215F, for example the USB interface, USR I/O, RTC, smart card interface, analog comparators, etc. The external interrupt configuration is shown in Figure 8.

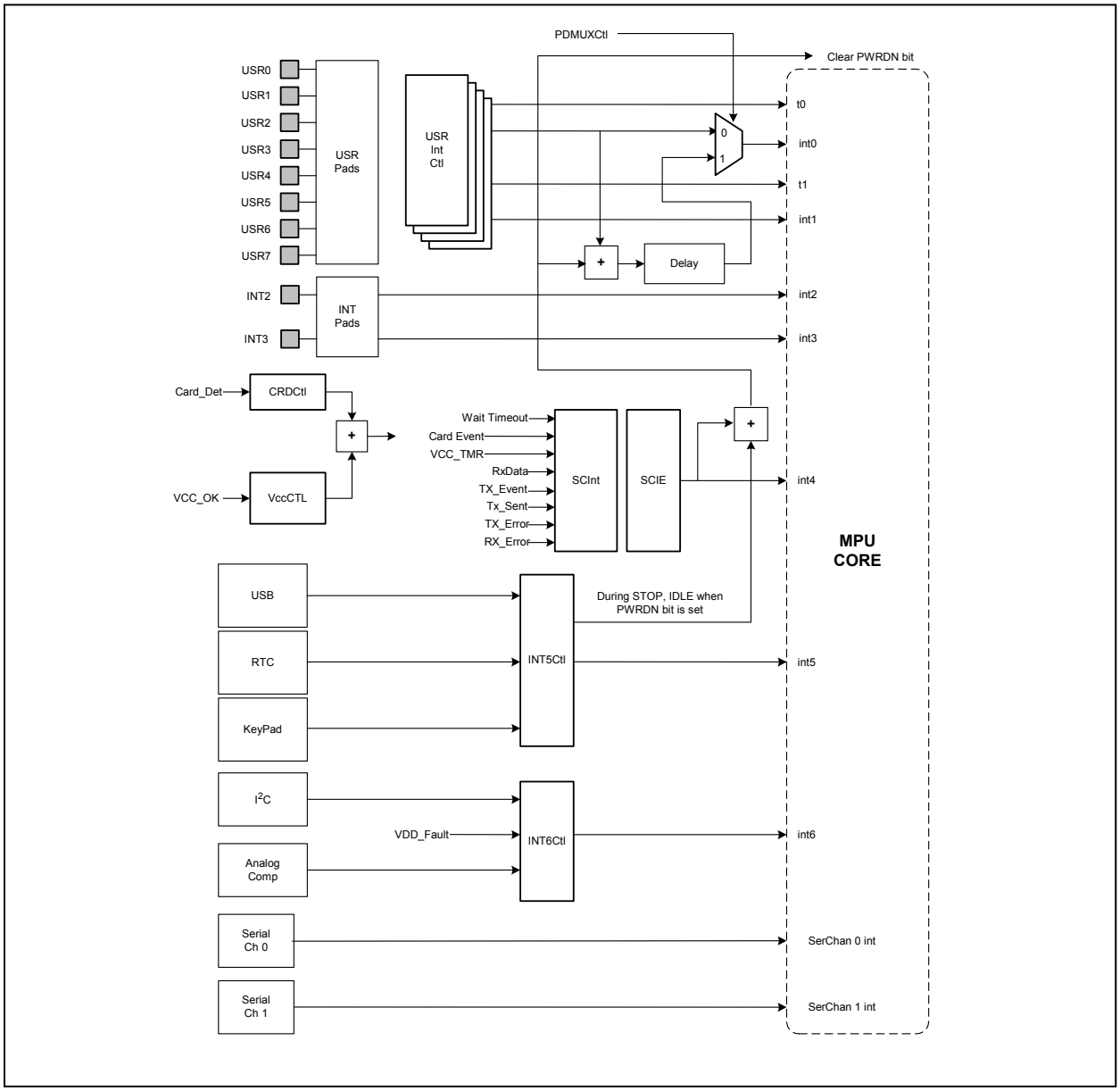


Figure 8: External Interrupt Configuration

Interrupt Priority 0 Register (IP0): 0xA9 ← 0x00

Table 46: The IP0 Register

MSB							LSB
–	WDTS	IP0.5	IP0.4	IP0.3	IP0.2	IP0.1	IP0.0

Bit	Symbol	Function
IP0.6	WDTS	Watchdog timer status flag. Set when the watchdog timer has expired. The internal reset will be generated, but this bit will not be cleared by the reset. This allows the user program to determine if the watchdog timer caused the reset to occur and respond accordingly. Can be read and cleared by software.

Note: The remaining bits in the IP0 register are not used for watchdog control.

Watchdog Timer Reload Register (WDTREL): 0x86 ← 0x00

Table 47: The WDTREL Register

MSB							LSB
WDPSEL	WDREL6	WDREL5	WDREL4	WDREL3	WDREL2	WDREL1	WDREL0

Bit	Symbol	Function
WDTREL.7	WDPSEL	Prescaler select bit. When set, the watchdog is clocked through an additional divide-by-16 prescaler.
WDTREL.6 to WDTREL.0	WDREL6-0	Seven bit reload value for the high-byte of the watchdog timer. This value is loaded to the WDT when a refresh is triggered by a consecutive setting of bits WDT and SWDT.

There are 3 sets of registers to load the RTC 24-bit accumulator, 32-bit counter and 23-bit trim registers. The registers are loaded when the RTCLD bit is set in RTCCtl.

Table 56: The 32-bit RTC Counter

Register	RTCCnt3	RTCCnt2	RTCCnt1	RTCCnt0
	RTCCnt[31:24]	RTCCnt[23:16]	RTCCnt[15:8]	RTCCnt[7:0]

Table 57: The 24-bit RTC Accumulator

Register		RTCACC2	RTCACC1	RTCACC0
		RTCACC [23:16]	RTCACC [15:8]	RTCACC [7:0]

Table 58: The 24-bit RTC Trim (sign magnitude value)

Register		RTCTrim2	RTCTrim1	RTCTrim0
		RTCTrim [23:16]	RTCTrim [15:8]	RTCTrim [7:0]

External Interrupt Control Register (INT5Ctl): 0xFF94 ← 0x00

Table 59: The INT5Ctl Register

MSB LSB

PDMUX	–	RTCIEN	RTCINT	USBIEN	USBINT	KPIEN	KPINT

Bit	Symbol	Function
INT5Ctl.7	PDMUX	Power down multiplexer control.
INT5Ctl.6	–	
INT5Ctl.5	RTCIEN	When set =1, enables RTC interrupt. Note: The RTC based watchdog will be enabled when set.
INT5Ctl.4	RTCINT	When set =1, indicates interrupt from Real Time Clock function. Cleared on read of register.
INT5Ctl.3	USBIEN	USB interrupt enable.
INT5Ctl.2	USBINT	USB interrupt flag.
INT5Ctl.1	KPIEN	Keypad interrupt enable.
INT5Ctl.0	KPINT	Keypad interrupt flag.

1.7.10 LED Drivers

The 73S1215F F provides four dedicated output pins for driving LEDs. The LED driver pins can be configured as current sources that will pull to ground to drive LEDs that are connected to VDD without the need for external current limiting resistors. These pins may be used as general purpose outputs with the programmed pull-down current and a strong (CMOS) pull-up, if enabled. The analog block must be enabled when these outputs are being used to drive the selected output current.

The pins can be used as inputs with consideration of the programmed output current and level. The register bit when read, indicates the state of the pin.

LED Control Register (LEDCtl): 0xFFF3 ← 0xFF

Table 62: The LEDCtl Register

MSB LSB

–	LPUEN	ISET.1	ISET.0	LEDD3	LEDD2	LEDD 1	LEDD0

Bit	Symbol	Function
LEDCtl.7	–	
LEDCtl.6	LPUEN	0 = Pull-up is enabled for the LED pin.
LEDCtl.5	ISET.1	These two bits control the drive current (to ground) for all of the LED driver pins. Current levels are: 00 = 0ma(off) 01 = 2ma 10 = 4ma 11 = 10ma
LEDCtl.4	ISET.0	
LEDCtl.3	LEDD3	Write data controls output level of pin LED3. Read will report level of pin LED3.
LEDCtl.2	LEDD2	Write data controls output level of pin LED2. Read will report level of pin LED2.
LEDCtl.1	LEDD1	Write data controls output level of pin LED1. Read will report level of pin LED1.
LEDCtl.0	LEDD0	Write data controls output level of pin LED0. Read will report level of pin LED0.

Keypad Scan Time Register (KSIZE): 0xD5 ← 0x00

This register is not applicable when HWSCEN is not set. Unused row inputs should be connected to VDD.

Table 74: The KSIZE Register

MSB							LSB
–	–	ROWSIZ.2	ROWSIZ.1	ROWSIZ.0	COLSIZ.2	COLSIZ.1	COLSIZ.0

Bit	Symbol	Function
KSIZE.7	–	
KSIZE.6	–	
KSIZE.5	ROWSIZ.2	Defines the number of rows in the keypad. Maximum number is 6 given the number of row pins on the package. Allows for a reduced keypad size for scanning.
KSIZE.4	ROWSIZ.1	
KSIZE.3	ROWSIZ.0	
KSIZE.2	COLSIZ.2	Defines the number of columns in the keypad. Maximum number is 5 given the number of column pins on the package. Allows for a reduced keypad size for scanning.
KSIZE.1	COLSIZ.1	
KSIZE.0	COLSIZ.0	

Keypad Column LS Scan Order Register (KORDERL): 0xD6 ← 0x00

In registers KORDERL and KORDERH, Column Scan Order(14:0) is grouped into 5 sets of 3 bits each. Each set determines which column (COL(4:0) pin) to activate by loading the column number into the 3 bits. When in HW_Scan_Enable mode, the hardware will step through the sets from 1Col to 5Col (up to the number of columns in Colsize) and scan the column defined in the 3 bits. To scan in sequential order, set a counting pattern with 0 in set 0, and 1 in set 1,and 2 in set 2, and 3 in set 3, and 4 in set 4. The firmware should update this as part of the interrupt service routine so that the new scan order is loaded prior to the next key being pressed. For example, to scan COL(0) first, 1Col(2:0) should be loaded with 000'b. To scan COL(4) fifth, 5Col(2:0) should be loaded with 100'b.

Table 75: The KORDERL Register

MSB							LSB
3COL.1	3COL.0	2COL.2	2COL.1	2COL.0	1COL.2	1COL.1	1COL.0

Bit	Symbol	Function
KORDERL.7	3COL.1	Column to scan 3rd (lsb's).
KORDERL.6	3COL.0	
KORDERL.5	2COL.2	Column to scan 2nd.
KORDERL.4	2COL.1	
KORDERL.3	2COL.0	
KORDERL.2	1COL.2	Column to scan 1st.
KORDERL.1	1COL.1	
KORDERL.0	1COL.0	

1.7.14.1 USB Interface Implementation

The 73S1215F Application Programming Interface includes some dedicated software commands to configure the USB interface, to get a status of each USB Endpoint, to stall / unstall portions of the USB, and to send / receive data to / from each endpoint.

USB API entirely manages the USB circuitry, the USB registers and the FIFOs. Use of those commands facilitates USB implementation, without dealing with low-level programming.

Miscellaneous Control Register 1 (MISCtl1): 0xFFF2 ← 0x10

Table 78: The MISCtl1 Register

MSB LSB

–	–	FRPEN	FLSH66	–	ANAPEN	USBPEN	USBCON

Bit	Symbol	Function
MISCtl1.7	–	
MISCtl1.6	–	
MISCtl1.5	FRPEN	Flash Read Pulse enable.
MISCtl1.4	FLSH66	Flash Read Pulse.
MISCtl1.3	–	
MISCtl1.2	ANAPEN	Analog power enable.
MISCtl1.1	USBPEN	0 = Enable the USB differential transceiver.
MISCtl1.0	USBCON	1 = Connect pull-up resistor from VDD to D+. If connected, the USB host will recognize the attachment of a USB device and begin enumeration.

Note: When using the USB on the 73S1215F, external 24Ω series resistors must be added to the D+ and D- signals to provide the proper impedance matching on these pins.

The USB peripheral block is not able to support read or write operations to the USB SFR registers when the MPU clock is running at MPU clock rates of 12MHz or greater. In order to properly communicate with the USB SFR registers when running at these speeds, wait states must be inserted when addressing the USB SFRs. The CKCON register allows wait states to be inserted when accessing these registers. The proper settings for the number of wait states are shown in **Error! Reference source not found.**.

When changing the MPU clock rate or the number of wait states, the USB connection must be inactive. If the USB is active, then it must be inactivated before changing the MPU clock or number of wait states. It can then be reconnected and re-enumerated. Changing these parameters while the USB interface is active may cause communication errors on the USB interface.

Clock Control Register (CKCON): 0x8E ← 0x01

Table 79: The CKCON Register

MSB LSB

–	–	–	–	–	CKWT.2	CKWT.1	CKWT.0

Bit	Symbol	Function
CKCON.7	–	
CKCON.6	–	
CKCON.5	–	
CKCON.4	–	
CKCON.3	–	
CKCON.2	CKWT.2	These three bits determine the number of wait states (machine cycles) to insert when accessing the USB SFRs: 000 = 0 (not to be used). 001 = 1 wait state. Use when MPU clock is <12MHz. 010 = 2 wait states. Use when MPU clock is between 12 and 16MHz. 011 = 3 wait states. Use when MPU clock is 24MHz. 100 = 4 wait states. 101 = 5 wait states. 110 = 6 wait states. 111 = 7 wait states.
CKCON.1	CKWT.1	
CKCON.0	CKWT.0	

1.7.15.1 ISO 7816 UART

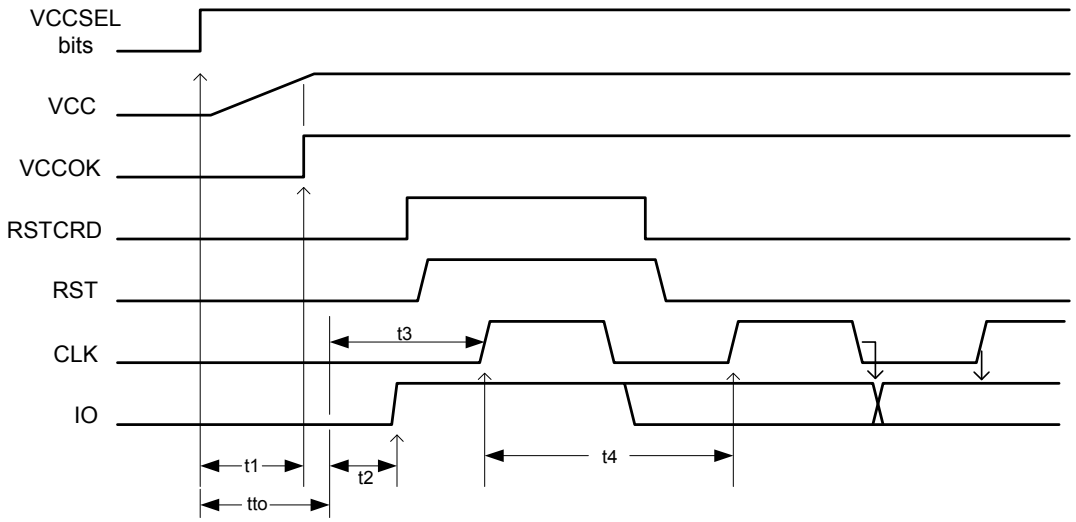
An embedded ISO 7816 (hardware) UART is provided to control communications between a smart card and the 73S1215F MPU. The UART can be shared between the one built-in ICC interface and the external ICC interface. Selection of the desired interface is made by register SCSel. Control of the external interface is handled by the I^2C interface for any external 8010 devices. The following is a list of features for the ISO 7816 UART:

- Two-byte FIFO for temporary data storage on both TX and Rx data.
- Parity checking in T=0. This feature can be enabled/disabled by firmware. Parity error reporting to firmware and Break generation to ICC can be controlled independently.
- Parity error generation for test purposes.
- Retransmission of last byte if ICC indicates T=0 parity error. This feature can be enabled/disabled by firmware.
- Deletion of last byte received if ICC indicates T=0 parity error. This feature can be enabled/disabled by firmware.
- CRC/LRC generation and checking. CRC/LRC is automatically inserted into T=1 data stream by the hardware. This feature can be enabled/disabled by firmware.
- Support baud rates: 230000, 115200, 57600, 38400, 28800, 19200, 14400, 9600 under firmware control (assuming 12MHz crystal) with various F/D settings
- Firmware manages F/D. All F/D combinations are supported in which F/D is directly divisible by 31 or 32 (i.e. F/D is a multiple of either 31 or 32).
- Flexible ETU clock generation and control.
- Detection of convention (direct or indirect) character TS. This affects both polarity and order of bits in byte. Convention can be overridden by firmware.
- Supports WTX Timeout with an expanded Wait Time Counter (28 bits).
- A Bypass Mode is provided to bypass the hardware UART in order for the software to emulate the UART (for non-standard operating modes). In such a case, the I/O line value is reflected in SFR SCCtl or SCECtl respectively for the built-in or external interfaces. This mode is appropriate for some synchronous and non T=0 / T=1 cards.

The single integrated smart card UART is capable of supporting T=0 and T=1 cards in hardware therefore offloading the bit manipulation tasks from the firmware. The embedded firmware instructs the hardware which smart card it should communicate with at any point in time. Firmware reconfigures the UART as required when switching between smart cards. When the 73S1215F has transmitted a message with an expected response, the firmware should not switch the UART to another smart card until the first smart card has responded. If the smart card responds while another smart card is selected, that first smart card's response will be ignored.

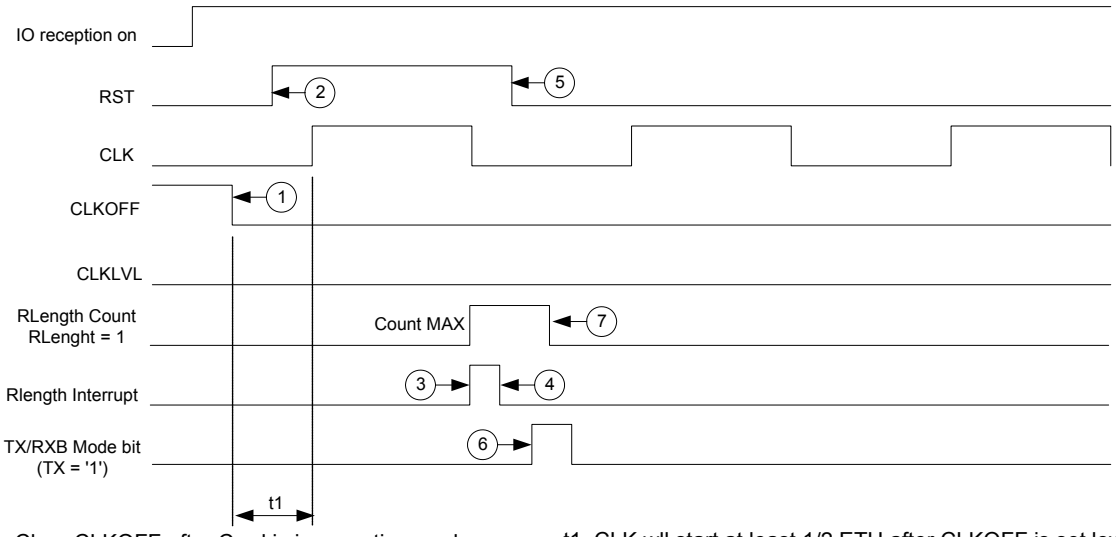
1.7.15.2 Answer to Reset Processing

A card insertion event generates an interrupt to the firmware, which is then responsible for the configuration of the electrical interface, the UART and activation of the card. The activation sequencer goes through the power up sequence as defined in the ISO 7816-3 specification. An asynchronous activation timing diagram is shown in Figure 17. After the card RST is de-asserted, the firmware instructs the hardware to look for a TS byte that begins the ATR response. If a response is not provided within the pre-programmed timeout period, an interrupt is generated and the firmware can then take appropriate action, including instructing the 73S1215F to begin a deactivation sequence. Once commanded, the deactivation sequencer goes through the power down sequence as defined in the ISO 7816-3 specification. If an ATR response is received, the hardware looks for a TS byte that determines direct/inverse convention. The hardware handles the indirect convention conversion such that the embedded firmware only receives direct convention. This feature can be disabled by firmware within SByteCtl register. Parity checking and break generation is performed on the TS byte unless disabled by firmware. If during the card session, a card removal, over-current or other error event is detected, the hardware will automatically perform the deactivation sequence and then generate an interrupt to the firmware. The firmware can then perform any other error handling required for proper system operation.



t1: The time from setting VCCSEL bits until VCCOK = 1.
tto: The time from setting VCCSEL bits until VCCTMR times out. At t1 (if RDYST = 1) or tto (if RDYST = 0), activation starts. It is suggested to have RDYST = 0 and use the VCCTMR interrupt to let MPU know when sequence is starting.
t2: time from start of activation (no external indication) until IO goes into reception mode (= 1). This is approximately 4 SCCLK (or SCECLK) clock cycles.
t3: minimum one half of ETU period.
t4: ETU period.
Note that in Sync mode, IO as input is sampled on the rising edge of CLK. IO changes on the falling edge of CLK, either from the card or from the 73S1215F. The RST signal to the card is directly controlled by the RSTCRD bit (non-inverted) via the MPU and is shown as an example of a possible RST pattern.

Figure 21: Synchronous Activation



1. Clear CLKOFF after Card is in reception mode.
2. Set RST bit.
3. Interrupt is generated when RIength counter is MAX.
4. Read and clear Interrupt.
5. Clear RST bit.
6. Toggle TX/RXB to reset bit counter.
7. Reload RLength Counter.

t1. CLK wll start at least 1/2 ETU after CLKOFF is set low when CLKLVL = 0

Figure 22: Example of Sync Mode Operation: Generating/Reading ATR Signals

STX Data Register (STXData): 0xFE07 ← 0x00

Table 87: The STXData Register

MSB							LSB
STXDAT.7	STXDAT.6	STXDAT.5	STXDAT.4	STXDAT.3	STXDAT.2	STXDAT.1	STXDAT.0

Bit	Function
STXData.7	Data to be transmitted to smart card. Gets stored in the TX FIFO and then extracted by the hardware and sent to the selected smart card. When the MPU reads this register, the byte pointer is changed to effectively "read out" the data. Thus, two reads will always result in an "empty" FIFO condition. The contents of the FIFO registers are not cleared, but will be overwritten by writes.
STXData.6	
STXData.5	
STXData.4	
STXData.3	
STXData.2	
STXData.1	
STXData.0	

SRX Control/Status Register (SRXCtl): 0xFE08 ← 0x00

This register is used to monitor reception of data from the smart card.

Table 88: The SRXCtl Register

MSB							LSB
BIT9DAT	–	LASTRX	CRCERR	RXFULL	RXEMTY	RXOVRR	PARITYE

Bit	Symbol	Function
SRXCtl.7	BIT9DAT	Bit 9 Data – When in sync mode and with MODE9/8B set, this bit will contain the data on IO (or SIO) pin that was sampled on the ninth CLK (or SCLK) rising edge. This is used to read data in synchronous 9-bit formats.
SRXCtl.6	–	
SRXCtl.5	LASTRX	Last RX Byte – User sets this bit during the reception of the last byte. When byte is received and this bit is set, logic checks CRC to match 0x1D0F (T=1 mode) or LRC to match 00h (T=1 mode), otherwise a CRC or LRC error is asserted.
SRXCtl.4	CRCERR	(Read only) 1 = CRC (or LRC) error has been detected.
SRXCtl.3	RXFULL	(Read only) RX FIFO is full. Status bit to indicate RX FIFO is full.
SRXCtl.2	RXEMTY	(Read only) RX FIFO is empty. This is only a status bit and does not generate a RX interrupt.
SRXCtl.1	RXOVRR	RX Overrun – (Read Only) Asserted when a receive-over-run condition has occurred. An over-run is defined as a byte was received from the smart card when the RX FIFO was full. Invalid data may be in the receive FIFO. Firmware should take appropriate action. Cleared when read. Additional writes to the RX FIFO are discarded when a RXOVRR occurs until the overrun condition is cleared. Will generate RXERR interrupt.
SRXCtl.0	PARITYE	Parity Error – (Read only) 1 = The logic detected a parity error on incoming data from the smart card. Cleared when read. Will generate RXERR interrupt.

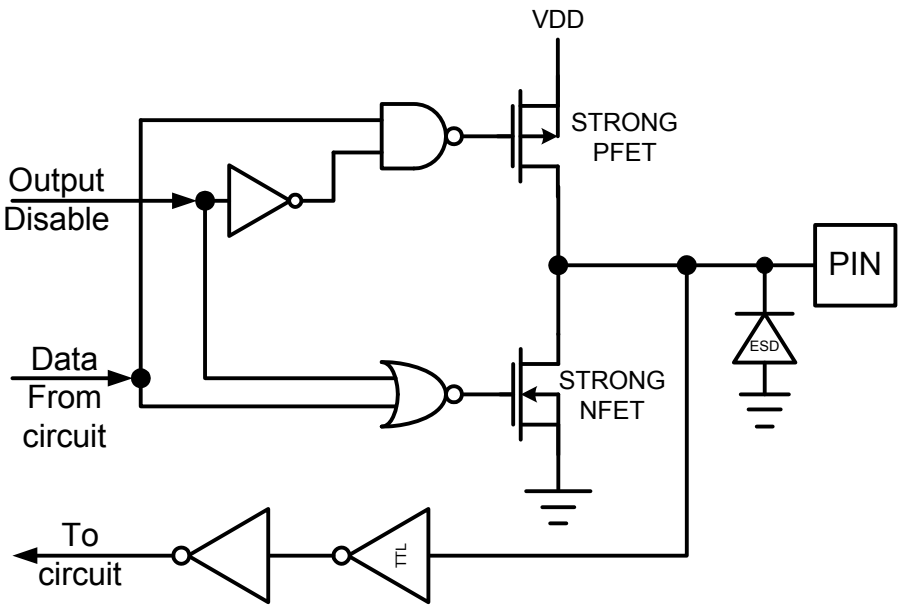


Figure 29: Digital I/O Circuit

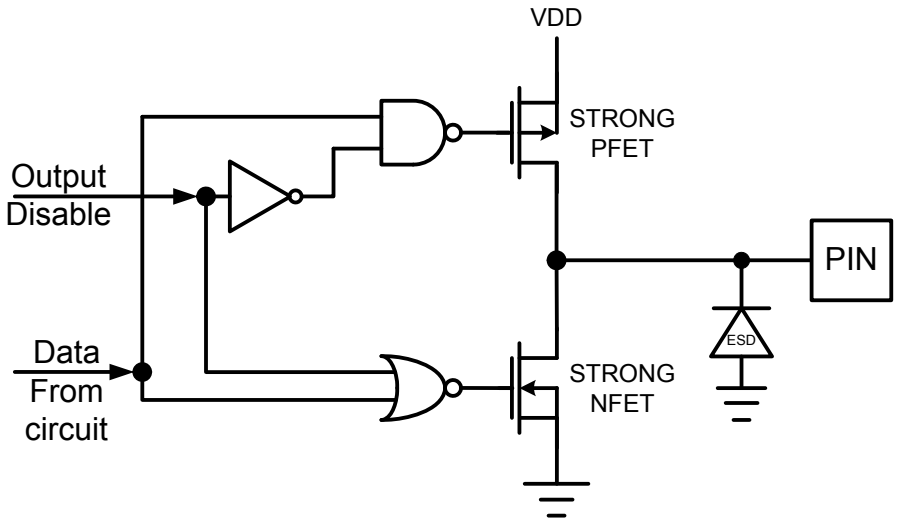


Figure 30: Digital Output Circuit

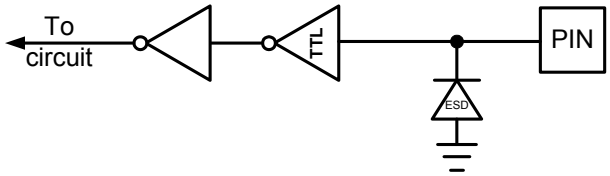


Figure 33: Digital Input Circuit

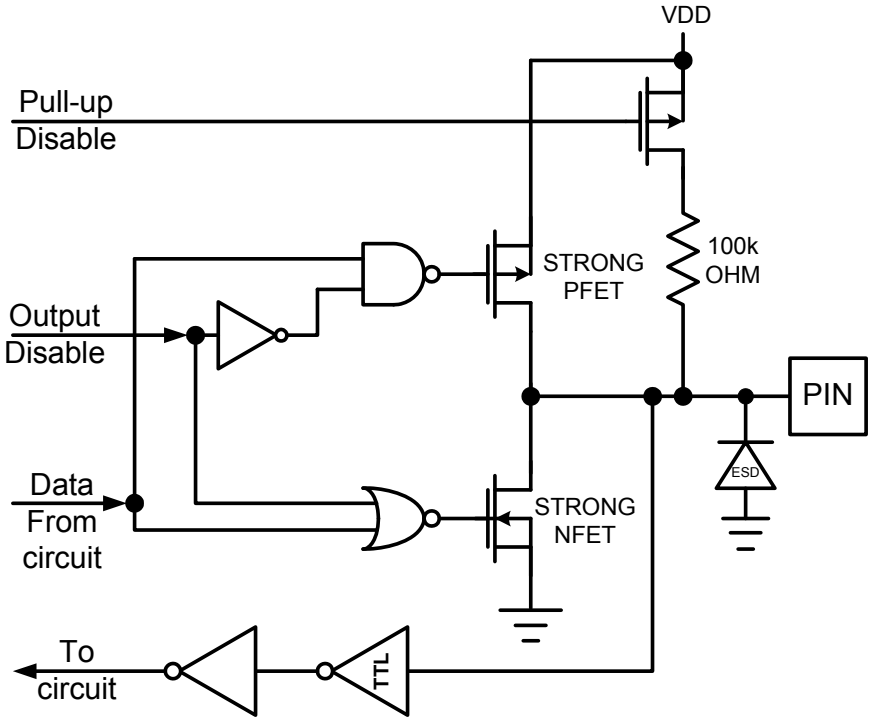


Figure 34: Keypad Row Circuit

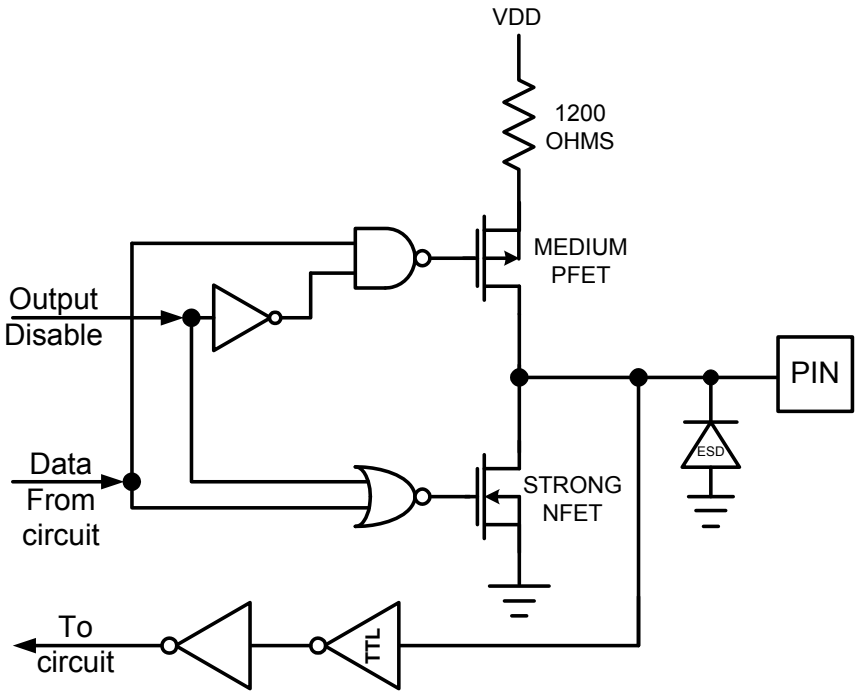


Figure 35: Keypad Column Circuit

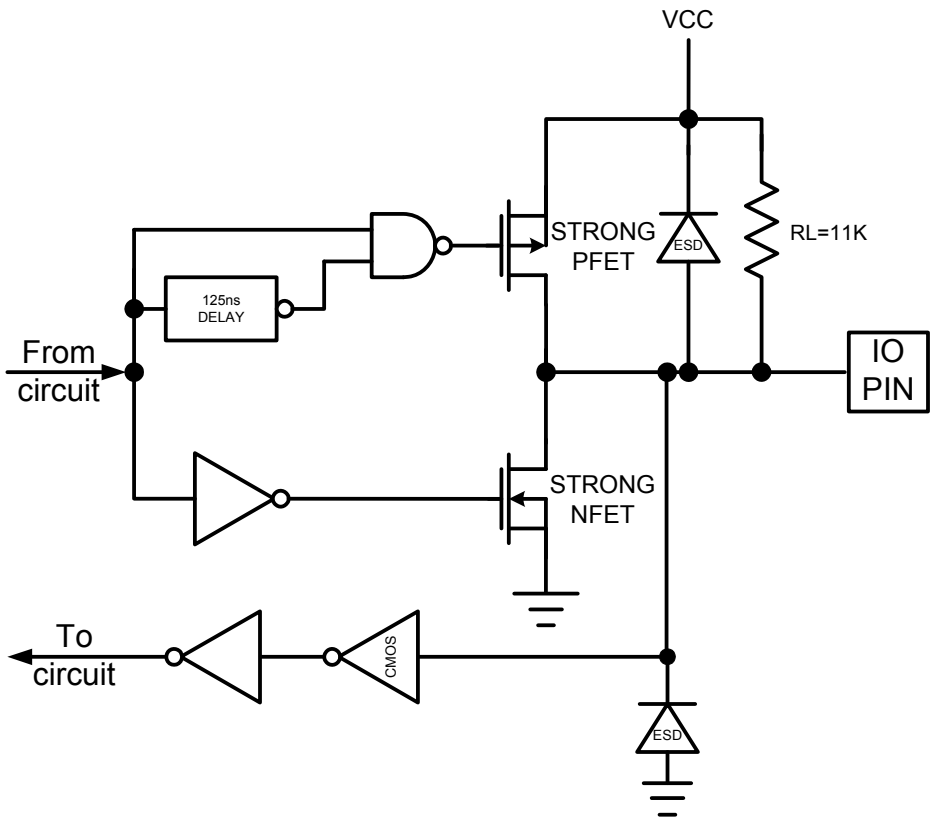


Figure 40: Smart Card I/O Circuit

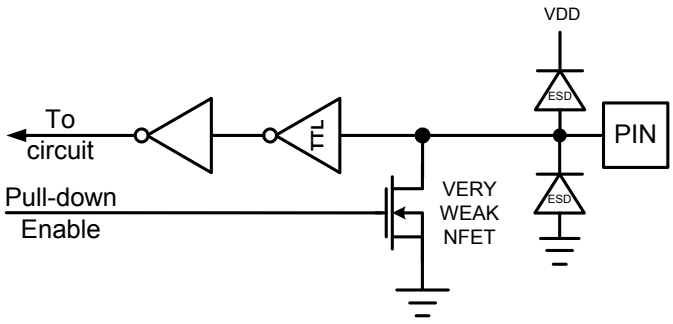


Figure 41: PRES Input Circuit