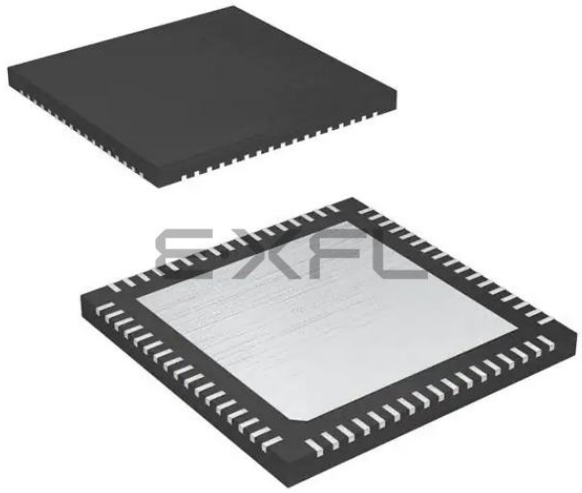
Analog Devices Inc./Maxim Integrated - 73S1215F-68IM/F/P Datasheet



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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Discontinued at Digi-Key
Core Processor	80515
Core Size	8-Bit
Speed	24MHz
Connectivity	I²C, SmartCard, UART/USART, USB
Peripherals	LED, POR, WDT
Number of I/O	9
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	68-VFQFN Exposed Pad
Supplier Device Package	68-QFN (8x8)
Purchase URL	https://www.e-xfl.com/product-detail/analog-devices/73s1215f-68im-f-p

Figures

Tables

1 Hardware Description

1.1 Pin Description

Table 1: 73S1215F Pinout Description

Pin Name	Pin (68 Qfn)	Pin (44 Qfn)	Type	Equivalent Circuit*	Description
X12IN	10	8	I	Figure 27	MPU/USB clock crystal oscillator input pin. A 12MHz crystal is required for USB operation. A 1MΩ resistor is required between pins X12IN and X12OUT.
X12OUT	11	9	O	Figure 27	MPU/USB clock crystal oscillator output pin.
X32IN	8		I	Figure 28	RTC clock crystal oscillator input pin. A 32768Hz crystal is required for low-power RTC operation.
X32OUT	7		O	Figure 28	RTC clock crystal oscillator output pin.
CPUCLK	39		O	Figure 30	Output signal, square wave at the frequency of the MPU clock.
DP	26	16	IO	Figure 43	USB D+ IO pin, requires series 24Ω resistor.
DM	27	17	IO	Figure 43	USB D- IO pin, requires series 24Ω resistor.
ROW(5:0) 0 1 2 3 4 5	 21 22 24 34 37 38		I	Figure 34	Keypad row input sense.
COL(4:0) 0 1 2 3 4	 12 13 14 16 19		O	Figure 35	Keypad column output scan pins.
USR(8:0) 0 1 2 3 4 5 6 7 8	 36 35 33 31 30 29 23 20 32	 24 23 22 21 20 19 14 13	IO	Figure 31	General-purpose user pins, individually configurable as inputs or outputs or as external input interrupt ports.
SCL	5	5	O	Figure 30	I^2C (master mode) compatible Clock signal. Note: the pin is configured as an open drain output. When the I2C interface is being used, an external pull up resistor is required. A value of 3K is recommended.
SDA	6	6	IO	Figure 29	I^2C (master mode) compatible data I/O. Note: this pin is bi-directional. When the pin is configured as output, it is an open drain output. When the I2C interface is being used, an external pull up resistor is required. A value of 3K is recommended.

Internal Data Memory: The Internal data memory provides 256 bytes (0x00 to 0xFF) of data memory. The internal data memory address is always one byte wide and can be accessed by either direct or indirect addressing. The Special Function Registers occupy the upper 128 bytes**. This SFR area is available only by direct addressing. Indirect addressing accesses the upper 128 bytes of Internal RAM.**

The lower 128 bytes contain working registers and bit-addressable memory. The lower 32 bytes form four banks of eight registers (R0-R7). Two bits on the program memory status word (PSW) select which bank is in use. The next 16 bytes form a block of bit-addressable memory space at bit addresses 0x00-0x7F. All of the bytes in the lower 128 bytes are accessible through direct or indirect addressing. Table 4 shows the internal data memory map.

Table 4: Internal Data Memory Map

<table>
<tr><th>Address</th><th>Direct Addressing</th><th>Indirect Addressing</th></tr>
<tr><td>0xFF</td><td rowspan="2">Special Function Registers (SFRs)</td><td rowspan="2">RAM</td></tr>
<tr><td>0x80</td></tr>
<tr><td>0x7F</td><td colspan="2" rowspan="2">Byte-addressable area</td></tr>
<tr><td>0x30</td></tr>
<tr><td>0x2F</td><td colspan="2" rowspan="2">Byte or bit-addressable area</td></tr>
<tr><td>0x20</td></tr>
<tr><td>0x1F</td><td colspan="2" rowspan="2">Register banks R0…R7 (x4)</td></tr>
<tr><td>0x00</td></tr>
</table>

External Data Memory: While the 80515 can address up to 64KB of external data memory in the space from 0x0000 to 0xFFFF, only the memory ranges shown in Figure 2 contain physical memory. The 80515 writes into external data memory when the MPU executes a MOVX @Ri,A or MOVX @DPTR,A instruction. The MPU reads external data memory by executing a MOVX A,@Ri or MOVX A,@DPTR instruction.

There are two types of instructions, differing in whether they provide an eight-bit or sixteen-bit indirect address to the external data RAM.

In the first type (MOVX A,@Ri), the contents of R0 or R1, in the current register bank, provide the eight lower-ordered bits of address. This method allows the user access to the first 256 bytes of the 2KB of external data RAM. In the second type of MOVX instruction (MOVX A,@DPTR), the data pointer generates a sixteen-bit address.

1.4 Program Security

Two levels of program and data security are available. Each level requires a specific fuse to be blown in order to enable or set the specific security mode. Mode 0 security is enabled by setting the SECURE bit (bit 6 of SFR register FLSHCTL 0xB2) Mode 0 limits the ICE interface to only allow bulk erase of the flash program memory. All other ICE operations are blocked. This guarantees the security of the user's MPU program code. Security (Mode 0) is enabled by MPU code that sets the SECURE bit. The MPU code must execute the setting of the SECURE bit immediately after a reset to properly enable Mode 0. This should be the first instruction after the reset vector jump has been executed. If the "startup.a51" assembly file is used in an application, then it must be modified to set the SECURE bit after the reset vector jump. If not using "startup.a51", then this should be the first instruction in main(). Once security Mode 0 is enabled, the only way to disable it is to perform a global erase of the flash followed by a full circuit reset. Once the flash has been erased and the reset has been executed, security Mode 0 is disabled and the ICE has full control of the core. The flash can be reprogrammed after the bulk erase operation is completed. Global erase of the flash will also clear the data XRAM memory.

The security enable bit (SECURE) is reset whenever the MPU is reset. Hardware associated with the bit only allows it to be set. As a result, the code may set the SECURE bit to enable the security Mode 0 feature but may not reset it. Once the SECURE bit is set, the code is protected and no external read of program code in flash or data (in XRAM) is possible. In order to invoke the security Mode 0, the SECSET0 (bit 1 of the XRAM SFR register SECReg 0xFFD7) fuse must be blown beforehand or the security mode 0 will not be enabled. The SECSET0 and SECSET1 fuses once blown, cannot be overridden.

Specifically, when SECURE is set:

- The ICE is limited to bulk flash erase only.
- Page zero of flash memory may not be page-erased by either MPU or ICE. Page zero may only be erased with global flash erase. Note that global flash erase erases XRAM whether the SECURE bit is set or not.
- Writes to page zero, whether by MPU or ICE, are inhibited.

Security mode 1 is in effect when the SECSET1 fuse has been programmed (blown open). In security mode 1, the ICE is completely and permanently disabled. The Flash program memory and the MPU are not available for alteration, observation, nor control. As soon as the fuse has been blown, the ICE is disabled. The testing of the SECSET1 fuse will occur during the reset and before the start of pre-boot and boot cycles. This mode is not reversible, nor recoverable. In order to blow the SECSET1 fuse, the SEC pin must be held high for the fuse burning sequence to be executed properly. The firmware can check to see if this pin is held high by reading the SECPIN bit (bit 5 of XRAM SFR register SECReg 0xFFD7). If this bit is set and the firmware desires, it can blow the SECSET1 fuse. The burning of the SECSET0 does not require the SEC pin to be held high.

In order to blow the fuse for SECSET1 and SECSET0, a particular set of register writes in a specific order need to be followed. There are two additional registers that need to have a specific value written to them in order for the desired fuse to be blown. These registers are FUSECtl (0xFFD2) and TRIMPCtl (0xFFD1). The sequence for blowing the fuse is as follows:

1. Write 0x54H to FUSECtl.
2. Write 0x81H for security mode 0. Note: only program one security mode at a time.
3. Write 0x82H for security mode 1. Note: SEC pin must be high for security mode 1.
4. Write 0xA6 to TRIMPCtl.
5. Delay about 500 us.
6. Write 0x00 to TRIMPCtl.

PSW	0xD0	0x00	Program Status Word
KCOL	0XD1	0x1F	Keypad Column
KROW	0XD2	0x3F	Keypad Row
KSCAN	0XD3	0x00	Keypad Scan Time
KSTAT	0XD4	0x00	Keypad Control/Status
KSIZE	0XD5	0x00	Keypad Size
KORDERL	0XD6	0x00	Keypad Column LS Scan Order
KORDERH	0XD7	0x00	Keypad Colum MS Scan Order
BRCON	0xD8	0x00	Baud Rate Control Register (only BRCON.7 bit used)
A	0xE0	0x00	Accumulator
B	0xF0	0x00	B Register

1.5.3 External Data Special Function Registers (SFRs)

A map of the XRAM Special Function Registers is shown in Table 8. The smart card registers are listed separately in Table 117.

Table 8: XRAM Special Function Registers Reset Values

Name	Location	Reset Value	Description
DAR	0x FF80	0x00	Device Address Register (I^2C)
WDR	0x FF81	0x00	Write Data Register (I^2C)
SWDR	0x FF82	0x00	Secondary Write Data Register (I^2C)
RDR	0x FF83	0x00	Read Data Register (I^2C)
SRDR	0x FF84	0x00	Secondary Read Data Register (I^2C)
CSR	0x FF85	0x00	Control and Status Register (I^2C)
USRIntCtl1	0x FF90	0x00	External Interrupt Control 1
USRIntCtl2	0x FF91	0x00	External Interrupt Control 2
USRIntCtl3	0x FF92	0x00	External Interrupt Control 3
USRIntCtl4	0x FF93	0x00	External Interrupt Control 4
INT5Ctl	0x FF94	0x00	External Interrupt Control 5
INT6Ctl	0x FF95	0x00	External Interrupt Control 6
MPUCKCtl	0x FFA1	0x0C	MPU Clock Control
RTCCtl	0x FFB0	0x00	Real Time Clock Control
RTCCnt3	0x FFB1	0x00	RTC Count 3
RTCCnt2	0x FFB2	0x00	RTC Count 2
RTCCnt1	0x FFB3	0x00	RTC Count 1
RTCCnt0	0x FFB4	0x00	RTC Count 0
RTCACC2	0x FFB5	0x00	RTC Accumulator 2
RTCACC1	0x FFB6	0x00	RTC Accumulator 1
RTCACC0	0x FFB7	0x00	RTC Accumulator 0
RTCTrim2	0x FFB8	0x00	RTC TRIM 2
RTCTrim1	0x FFB9	0x00	RTC TRIM 1
RTCTrim0	0x FFBA	0x00	RTC TRIM 0
ACOMP	0x FFD0	0x00	Analog Compare Register

Program Status Word (PSW):

Table 9: PSW Register Flags

MSB							LSB
CV	AC	F0	RS1	RS	OV	–	P

Table 10: PSW Bit Functions

Bit	Symbol	Function
PSW.7	CV	Carry flag.
PSW.6	AC	Auxiliary Carry flag for BCD operations.
PSW.5	F0	General purpose Flag 0 available for user.
PSW.4	RS1	Register bank select control bits. The contents of RS1 and RS0 select the working register bank:
PSW.3	RS0	
PSW.2	OV	Overflow flag.
PSW.1	F1	General purpose Flag 1 available for user.
PSW.0	P	Parity flag, affected by hardware to indicate odd / even number of "one" bits in the Accumulator, i.e. even parity.

RS1/RS0	Bank Selected	Location
00	Bank 0	(0x00 – 0x07)
01	Bank 1	(0x08 – 0x0F)
10	Bank 2	(0x10 – 0x17)
11	Bank 3	(0x18 – 0x1F)

Stack Pointer (SP): The stack pointer is a 1-byte register initialized to 0x07 after reset. This register is incremented before PUSH and CALL instructions, causing the stack to begin at location 0x08.

Data Pointer: The data pointer (DPTR) is 2 bytes wide. The lower part is DPL, and the highest is DPH. It can be loaded as a 2-byte register (MOV DPTR,#data16) or as two registers (e.g. MOV DPL,#data8). It is generally used to access external code or data space (e.g. MOVC A,@A+DPTR or MOVX A,@DPTR respectively).

Program Counter: The program counter (PC) is 2 bytes wide initialized to 0x0000 after reset. This register is incremented during the fetching operation code or when operating on data from program memory. Note: The program counter is not mapped to the SFR area.

Port Registers: The I/O ports are controlled by Special Function Registers USR70, and USR8. The contents of the SFR can be observed on corresponding pins on the chip. Writing a 1 to any of the ports (see Table 11) causes the corresponding pin to be at high level (3.3V), and writing a 0 causes the corresponding pin to be held at low level (GND). The data direction registers UDIR70, and UDIR8 define individual pins as input or output pins (see the User (USR) Ports section for details).

1.7.2 Power Control Modes

The 73S1215F contains circuitry to disable portions of the device and place it into a lower power standby mode. This is accomplished by either shutting off the power or disabling the clock going to the block. The miscellaneous control registers MISCtl0, MISCtl1 and the master clock control register (MCLKCtl) provide control over the power modes. There is also a device power down mode that will stop the core, clock subsystem and the peripherals connected to it. The PWRDN bit in MISCtl0 will set up the 73S1215F for power down and disable all clocks except the 32kHz oscillator. The power down mode should only be initiated by setting the PWRDN bit in the MISCtl0 register and not by manipulating individual control bits in various registers. Figure 5 shows how the PWRDN bit controls the various functions that comprise power down state.

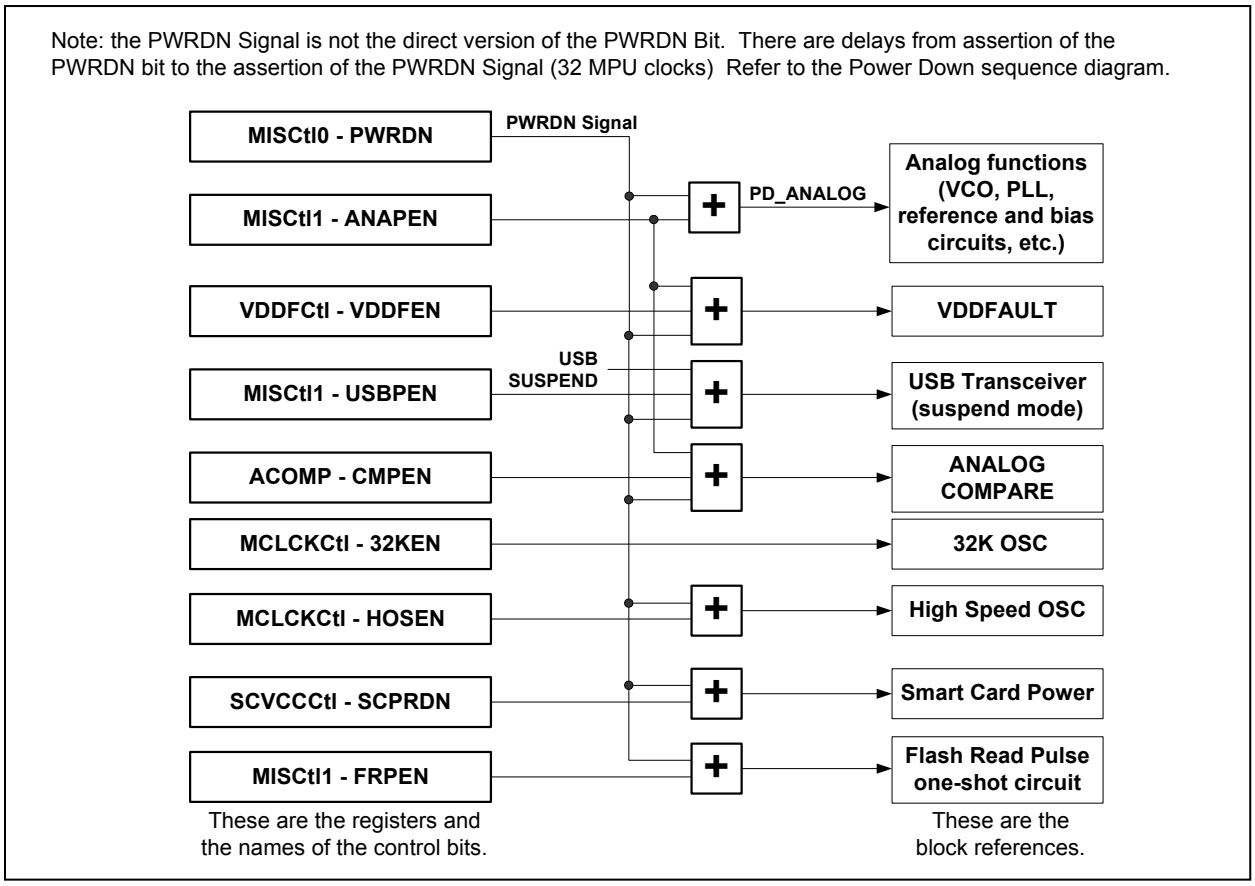


Figure 5: Power Down Control

When the PWRDN bit is set, the clock subsystem will provide a delay of 32 MPUCLK cycles to allow the program to set the STOP bit in the PCON register. This delay will enable the program to properly halt the core before the analog circuits shut down (high speed oscillator, VCO/PLL, voltage reference and bias circuitry, etc.). The PDMUX bit in SFR INT5Ctl should be set prior to setting the PWRDN bit in order to configure the wake up interrupt logic. The power down mode is awakened from interrupts connected to external interrupts 0, 4 and 5 (external USR[0:7], smart card, USB, RTC and Keypad). These interrupt sources are OR'ed together and routed through some delay logic into INT0 to provide this functionality. The interrupt will turn on the power to all sections that were shut off and start the clock subsystem. After the clock subsystem clocks start running, the MPUCLK begins to clock a 512 count delay counter. When the counter times out, the interrupt will then be active on INT0 and the program can resume. Figure 6 shows the detailed logic for waking up the 73S1215F from a power down state using these specific interrupt sources. Figure 7 shows the timing associated with the power down mode.

Power Control Register 0 (PCON): 0x87 ← 0x00

The SMOD bit used for the baud rate generator is setup via this register.

Table 19: The PCON Register

MSB LSB

SMOD	–	–	–	GF1	GF0	STOP	IDLE

Bit	Symbol	Function
PCON.7	SMOD	If SM0D = 1, the baud rate is doubled.
PCON.6	–	
PCON.5	–	
PCON.4	–	
PCON.3	GF1	General purpose flag 1.
PCON.2	GF0	General purpose flag 1.
PCON.1	STOP	Sets CPU to Stop mode.
PCON.0	IDLE	Sets CPU to Idle mode.

Interrupt Enable 1 Register (IEN1): 0xB8 ← 0x00

Table 21: The IEN1 Register

MSB							LSB
–	SWDT	EX6	EX5	EX4	EX3	EX2	–

Bit	Symbol	Function
IEN1.7	–	
IEN1.6	SWDT	Not used for interrupt control.
IEN1.5	EX6	EX6 = 0 – disable external interrupt 6.
IEN1.4	EX5	EX5 = 0 – disable external interrupt 5.
IEN1.3	EX4	EX4 = 0 – disable external interrupt 4.
IEN1.2	EX3	EX3 = 0 – disable external interrupt 3.
IEN1.1	EX2	EX2 = 0 – disable external interrupt 2.
IEN1.0	–	

Interrupt Enable 2 Register (IEN2): 0x9A ← 0x00

Table 22: The IEN2 Register

MSB							LSB
–	–	–	–	–	–	–	ES1

Bit	Symbol	Function
IEN2.0	ES1	ES1 = 0 – disable serial channel interrupt.

1.7.5 Timers and Counters

The 80515 has two 16-bit timer/counter registers: Timer 0 and Timer 1. These registers can be configured for counter or timer operations.

In timer mode, the register is incremented every machine cycle, meaning that it counts up after every 12 periods of the MPU clock signal.

In counter mode, the register is incremented when the falling edge is observed at the corresponding input signal T0 or T1 (T0 and T1 are the timer gating inputs derived from USR[0:7] pins, see the User (USR) Ports section). Since it takes 2 machine cycles to recognize a 1-to-0 event, the maximum input count rate is 1/2 of the oscillator frequency. There are no restrictions on the duty cycle, however to ensure proper recognition of 0 or 1 state, an input should be stable for at least 1 machine cycle.

Four operating modes can be selected for Timer 0 and Timer 1. Two Special Function Registers (TMOD and TCON) are used to select the appropriate mode.

The Timer 0 load registers are designated as TL0 and TH0 and the Timer 1 load registers are designated as TL1 and TH1.

Timer/Counter Mode Control Register (TMOD): 0x89 ← 0x00

Bits TR1 and TR0 in the TCON register start their associated timers when set.

Table 41: The TMOD Register

MSB LSB

GATE	C/T	M1	M0	GATE	C/T	M1	M0
Timer 1				**Timer 0**			

Bit	Symbol	Function
TMOD.7 TMOD.3	Gate	If set, enables external gate control (USR pin(s) connected to T0 or T1 for Counter 0 or 1, respectively). When T0 or T1 is high, and TRx bit is set (see the TCON register), a counter is incremented every falling edge on T0 or T1 input pin. If not set, the TRx bit controls the corresponding timer.
TMOD.6 TMOD.2	C/T	Selects Timer or Counter operation. When set to 1, the counter operation is performed based on the falling edge of T0 or T1. When cleared to 0, the corresponding register will function as a timer.
TMOD.5 TMOD.1	M1	Selects the mode for Timer/Counter 0 or Timer/Counter 1, as shown in TMOD description.
TMOD.4 TMOD.0	M0	Selects the mode for Timer/Counter 0 or Timer/Counter 1, as shown in TMOD description.

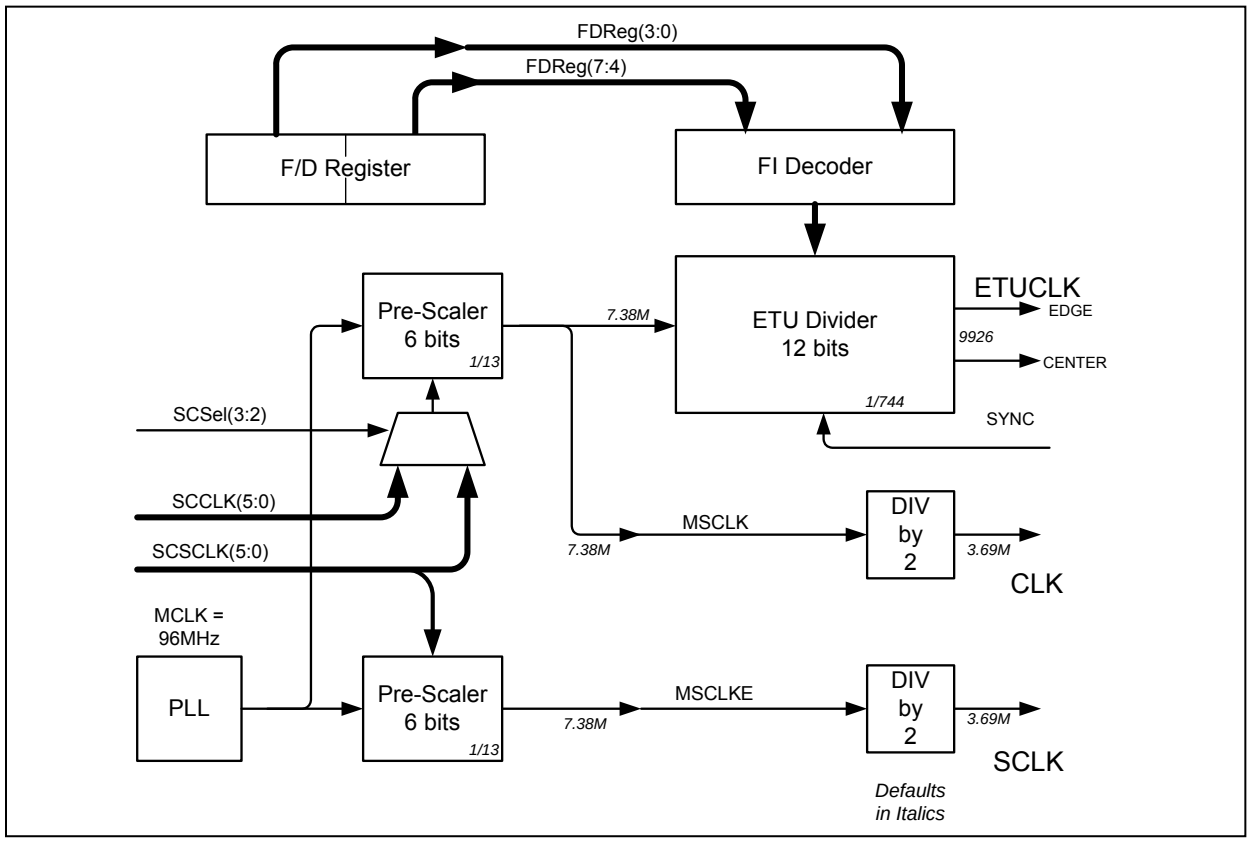


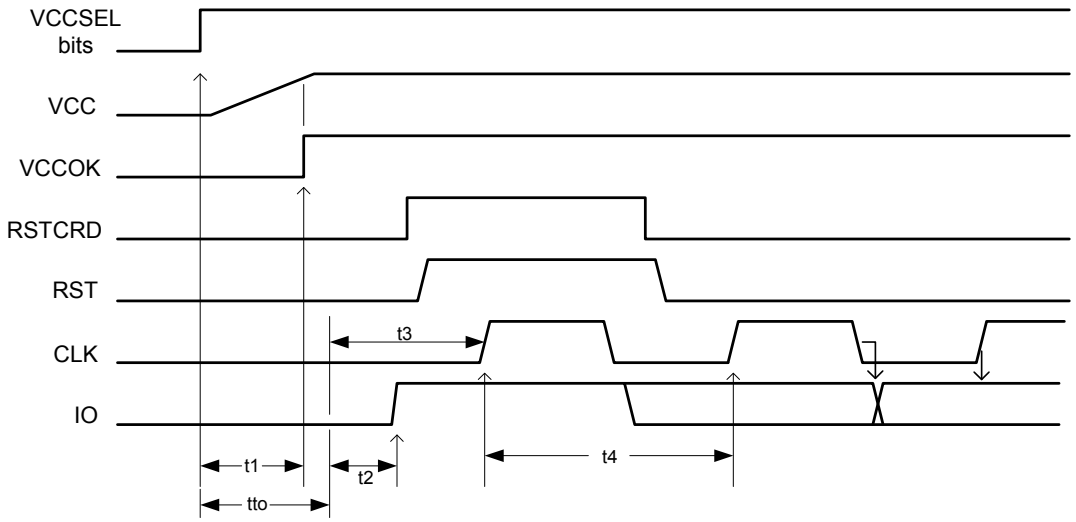
Figure 19: Smart Card CLK and ETU Generation

There are two, two-byte FIFOs that are used to buffer transmit and receive data. During a T=0 processing, if a parity error is detected by the 73S1215F during message reception, an error signal (BREAK) will be generated to the smart card. The byte received will be discarded and the firmware notified of the error. Break generation and receive byte dropping can be disabled under firmware control. During the transmission of a byte, if an error signal (BREAK) is detected, the last byte is retransmitted again and the firmware notified. Retransmission can be disabled by firmware. When a correct byte is received, an interrupt is generated to the firmware, which then reads the byte from the receive FIFO. Receive overruns are detected by the hardware and reported via an interrupt. During transmission of a message, the firmware will write bytes into the transmit FIFO. The hardware will send them to the smart card. When the last byte of a message has been written, the firmware will need to set the LASTTX bit in the STXCtl SFR. This will cause the hardware to insert the CRC/LRC if in a T=1 protocol mode. CRC/LRC generation/checking is only provided during T=1 processing. Firmware will need to instruct the smart function to go into receive mode after this last transmit data byte if it expects a response from the smart card. At the end of the smart card response, the firmware will put the interface back into transmit mode if appropriate.

The hardware can check for the following card-related timeouts:

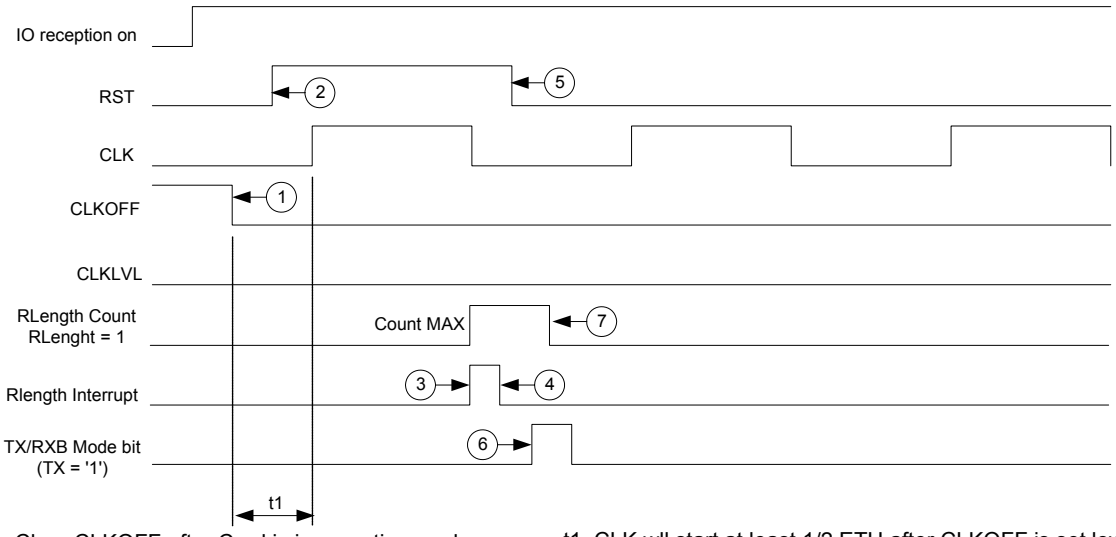
- Character Waiting Time (CWT)
- Block Waiting Time (BWT)
- Initial Waiting Time (IWT)

The firmware will load the Wait Time registers with the appropriate value for the operating mode at the appropriate time. Figure 20 shows the guard, block, wait and ATR time definitions. If a timeout occurs, an interrupt will be generated and the firmware can take appropriate recovery steps. Support is provided for adding additional guard times between characters (Extra Guard Time register) and between the last byte received by the 73S1215F and the first byte transmitted by the 73S1215F Block Guard Time register (BGT). Other than the protocol checks described above, the firmware is responsible for all protocol checking and error recovery.



t1: The time from setting VCCSEL bits until VCCOK = 1.
tto: The time from setting VCCSEL bits until VCCTMR times out. At t1 (if RDYST = 1) or tto (if RDYST = 0), activation starts. It is suggested to have RDYST = 0 and use the VCCTMR interrupt to let MPU know when sequence is starting.
t2: time from start of activation (no external indication) until IO goes into reception mode (= 1). This is approximately 4 SCCLK (or SCECLK) clock cycles.
t3: minimum one half of ETU period.
t4: ETU period.
Note that in Sync mode, IO as input is sampled on the rising edge of CLK. IO changes on the falling edge of CLK, either from the card or from the 73S1215F. The RST signal to the card is directly controlled by the RSTCRD bit (non-inverted) via the MPU and is shown as an example of a possible RST pattern.

Figure 21: Synchronous Activation



1. Clear CLKOFF after Card is in reception mode.
2. Set RST bit.
3. Interrupt is generated when RIength counter is MAX.
4. Read and clear Interrupt.
5. Clear RST bit.
6. Toggle TX/RXB to reset bit counter.
7. Reload RLength Counter.

t1. CLK wll start at least 1/2 ETU after CLKOFF is set low when CLKLVL = 0

Figure 22: Example of Sync Mode Operation: Generating/Reading ATR Signals

Smart Card Interrupt Register (SCInt): 0xFE01 ← 0x00

When the smart card interrupt is asserted, the firmware can read this register to determine the actual cause of the interrupt. The bits are cleared when this register is read. Each interrupt can be disabled by the Smart Card Interrupt Enable register. Error processing must be handled by the firmware. This register relates to the interface that is active – see the SCSel register.

Table 82: The SCInt Register

MSB							LSB
WAITTO	CRDEVT	VCCTMRI	RXDAV	TXEVT	TXSENT	TXERR	RXERR

Bit	Symbol	Function
SCInt.7	WAITTO	Wait Timeout – An ATR or card wait timeout has occurred. In sync mode, this interrupt is asserted when the RLen counter (it advances on falling edges of CLK/ETU) reaches the loaded (max) value. This bit is cleared when the SCInt register is read. When running in Synchronous Clock Stop Mode, this bit becomes RLenINT interrupt (set when the Rlen counter reaches the terminal count).
SCInt.6	CRDEVT	Card Event – A card event is signaled via pin DETCARD either when the Card was inserted or removed (read the CRDCtl register to determine card presence) or there was a fault condition in the interface circuitry. This bit is functional even if the smart card logic clock is disabled and when the PWRDN bit is set. This bit is cleared when the SCInt register is read.
SCInt.5	VCCTMRI	VCC Timer – This bit is set when the VCCTMR times out. This bit is cleared when the SCInt register is read.
SCInt.4	RXDAV	Rx Data Available – Data was received from the smart card because the Rx FIFO is not empty. In bypass mode, this interrupt is generated on a falling edge of the smart card I/O line. After receiving this interrupt in bypass mode, firmware should disable it until the firmware has received the entire byte and is waiting for the next start delimiter. This bit is cleared when there is no RX data available in the RX FIFO.
SCInt.3	TXEVNT	TX Event – Set whenever the TXEMTY or TXFULL bits are set in the SRXCtl SFR. This bit is cleared when the STXCtl register is read.
SCInt.2	TXSENT	TX Sent – Set whenever the ISO UART has successfully transmitted a byte to the smart card. Also set when a CRC/LRC byte is sent in T=1 mode. Will not be set in T=0 when a break is detected at the end of a byte (when break detection is enabled). This bit is cleared when the SCInt register is read.
SCInt.1	TXERR	TX Error – An error was detected during the transmission of data to the smart card as indicated by either BREAKD or TXUNDR bit being set in the STXCtl SFR. Additional information can be found in that register description. This bit is cleared when the STXCtl register is read.
SCInt.0	RXERR	RX Error – An error was detected during the reception of data from the smart card. Additional information can be found in the SRXCtl register. This interrupt will be asserted for RXOVRR, or RX Parity error events. This bit is cleared when the SRXCtl register is read.

Card Status/Control Register (CRDCtl): 0xFE05 ← 0x00

This register is used to configure the card detect pin (DETCARD) and monitor card detect status. This register be written to properly configure Debounce, Detect_Polarity (= 0 or = 1), and the pull-up/down enable before setting CDETEN. The card detect logic is functional even without smart card logic clock. When the PWRDN bit is set = 1, no debounce is provided but card presence is operable.

MSB LSB

DEBOUN	CDETEN	–	–	DETPOL	PUENB	PDEN	CARDIN

Bit	Symbol	Function
CRDCtl.7	DEBOUN	Debounce – When set = 1, this will enable hardware de-bounce of the card detect pin. The de-bounce function shall wait for 64ms of stable card detect assertion before setting the CARDIN bit. This counter/timer uses the keypad clock as a source of 1kHz signal. De-assertion of the CARDIN bit is immediate upon de-assertion of the card detect pin(s).
CRDCtl.6	CDETEN	Card Detect Enable – When set = 1, activates card detection input. Default upon power-on reset is 0.
CRDCtl.5	–	
CRDCtl.4	–	
CRDCtl.3	DETPOL	Detect Polarity – When set = 1, the DETCARD pin shall interpret a logic 1 as card present.
CRDCtl.2	PUENB	Enable pull-up current on DETCARD pin (active low).
CRDCtl.1	PDEN	Enable pull-down current on DETCARD pin.
CRDCtl.0	CARDIN	Card Inserted – (Read only). 1 = card inserted, 0 = card not inserted. A change in the value of this bit is a “card event.” A read of this bit indicates whether smart card is inserted or not inserted in conjunction with the DETPOL setting.

TX Control/Status Register (STXCtl): 0xFE06 ← 0x00

This register is used to control transmission of data to the smart card. Some control and some status bits are in this register.

Table 86: The STXCtl Register

MSB							LSB
I2CMODE	–	TXFULL	TXEMTY	TXUNDR	LASTTX	TX/RXB	BREAKD

Bit	Symbol	Function
STXCtl.7	I2CMODE	I2C Mode – When in sync mode and this bit is set, and when the RLen count value = max or 0, the source of the smart card data for IO pin (or SIO pin) will be connected to the IO bit in SCCtl (or SCECtl) register rather than the TX FIFO. See the description for the Protocol Mode Register for more detail.
STXCtl.6	–	
STXCtl.5	TXFULL	TX FIFO is full. Additional writes may corrupt the contents of the FIFO. This bit it will remain set as long as the TX FIFO is full. Generates TX_Event interrupt upon going full.
STXCtl.4	TXEMTY	1 = TX FIFO is empty, 0 = TX FIFO is not empty. If there is data in the TX FIFO, the circuit will transmit it to the smart card if in transmit mode. In T=1 mode, if the LASTTX bit is set and the hardware is configured to transmit the CRC/LRC, the TXEMTY will not be set until the CRC/LRC is transmitted. In T=0, if the LASTTX bit is set, TXEMTY will be set after the last word has been successfully transmitted to the smart card. Generates TXEVNT interrupt upon going empty.
STXCtl.3	TXUNDR	TX Underrrun – (Read only) Asserted when a transmit under-run condition has occurred. An under-run condition is defined as an empty TX FIFO when the last data word has been successfully transmitted to the smart card and the LASTTX bit was not set. No special processing is performed by the hardware if this condition occurs. Cleared when read by firmware. This bit generates TXERR interrupt.
STXCtl.2	LASTTX	Last TX Byte – Set by firmware (in both T=0 and T=1) when the last byte in the current message has been written into the transmit FIFO. In T=1 mode, the CRC/LRC will be appended to the message. Should be set after the last byte has been written into the transmit FIFO. Should be cleared by firmware before writing first byte of next message into the transmit FIFO. Used in T=0 to determine when to set TXEMTY.
STXCtl.1	TX/RXB	1 = Transmit mode, 0 = Receive mode. Configures the hardware to be receiving from or transmitting to the smart card. Determines which counters should be enabled. This bit should be set to receive mode prior to switching to another interface. Setting and resetting this bit shall initialize the CRC logic. If LASTTX is set, this bit can be reset to RX mode and UART logic will automatically change mode to RX when TX operation is completed (TX_Empty =1).
STXCtl.0	BREAKD	Break Detected – (Read only) 1 = A break has been detected on the I/O line indicating that the smart card detected a parity error. Cleared when read. This bit generates TXERR interrupt.

Protocol Mode Register (SPrtcol): 0xFE0D ← 0x03

This register determines the protocol to be use when communicating with the selected smart card. This register should be updated as required when switching between smart card interfaces.

Table 93: The SPrtcol Register

MSB LSB

SCISYN	MOD9/8B	SCESYN	0	TMODE	CRCEN	CRCMS	RCVATR

Bit	Symbol	Function
SPrtcol.7	SCISYN	Smart Card Internal Synchronous mode – Configures internal smart card interface for synchronous mode. This mode routes the internal interface buffers for RST, IO, C4, C8 to SCCtl register bits for direct firmware control. CLK is generated by the ETU counter.
SPrtcol.6	MOD9/8B	Synchronous 8/9 bit mode select – For sync mode, in protocols with 9-bit words, set this bit. The first eight bits read go into the RX FIFO and the ninth bit read will be stored in the IO (or SIO) data bit of the SRXCtl register.
SPrtcol.5	SCESYN	Smart Card External Synchronous mode – Configures External Smart Card interface for synchronous mode. This mode routes the external smart card interface buffers for SIO to SCECtl register bits for direct firmware control. SCLK is generated by the ETU counter.
SPrtcol.4	0	Reserved bit, must always be set to 0.
SPrtcol.3	TMODE	Protocol mode select – 0: T=0, 1: T=1. Determines which smart card protocol is to be used during message processing.
SPrtcol.2	CRCEN	CRC Enable – 1 = Enabled, 0 = Disabled. Enables the checking/generation of CRC/LRC while in T=1 mode. Has no effect in T=0 mode. If enabled and a message is being transmitted to the smart card, the CRC/LRC will be inserted into the message stream after the last TX byte is transmitted to the smart card. If enabled, CRC/LRC will be checked on incoming messages and the value made available to the firmware via the CRC LS/MS registers.
SPrtcol.1	CRCMS	CRC Mode Select - 1 = CRC, 0 = LRC. Determines type of checking algorithm to be used.
SPrtcol.0	RCVATR	Receive ATR – 1 = Enable ATR timeout, 0 = Disable ATR timeout. Set by firmware after the smart card has been turned on and the hardware is expecting ATR.

FD Control Register (FDReg): 0xFE13 ← 0x11

This register uses the transmission factors F and D to set the ETU (baud) rate. The values in this register are mapped to the ISO 7816 conversion factors as described below. The CLK signal for each interface is created by dividing a high-frequency, intermediate signal (MSCLK) by 2. The ETU baud rate is created by dividing MSCLK by 2 times the Fi/Di ratio specified by the codes below. For example, if FI = 0001 and DI = 0001, the ratio of Fi/Di is 372/1. Thus the ETU divider is configured to divide by 2 * 372 = 744. The maximum supported F/D ratio is 4096.

Table 99: The FDReg Register

MSB LSB

FVAL.3	FVAL.2	FVAL.1	FVAL.0	DVAL.3	DVAL.2	DVAL.1	DVAL.0

Table 100: Divider Ratios Provided by the ETU Counter

FI (code)	0000	0001	0010	0011	0100	0101	0110	0111
Fi (ratio)	372	372	558	744	1116	1488	1860	1860⊕
FCLK max	4	5	6	8	12	16	20	20⊕

FI(code)	1000	1001	1010	1011	1100	1101	1110	1111
Fi(ratio)	512⊕	512	768	1024	1536	2048	2048⊕	2048⊕
FCLK max	5⊕	5	7.5	10	15	20	20⊕	20⊕

DI(code)	0000	0001	0010	0011	0100	0101	0110	0111
Di(ratio)	1⊕	1	2	4	8	16	32	32⊕

DI(code)	1000	1001	1010	1011	1100	1101	1110	1111
Di(ratio)	12	20	16⊕	16⊕	16⊕	16⊕	16⊕	16⊕

Note: values marked with ⊕ are not included in the ISO definition and arbitrary values have been assigned.

The values given below are used by the ETU divider to create the ETU clock. The entries that are not shaded will result in precise CLK/ETU per ISO requirements. Shaded areas are not precise but are within 1% of the target value.

1.7.16 VDD Fault Detect Function

The 73S1215F contains a circuit to detect a low-voltage condition on the supply voltage V_{DD}. If enabled, it will deactivate the active internal smart card interface when V_{DD} falls below the V_{DD} Fault threshold. The register configures the V_{DD} Fault threshold for the nominal default of 2.3V* or a user selectable threshold. The user's code may load a different value using the FOVRVDDF bit =1 after the power-up cycle has completed

VDDFault Control Register (VDDFCtl): 0xFFD4 ← 0x00

Table 118: The VDDFCtl Register

MSB LSB

–	FOVRVDDF	VDDFLTEN	–	STXDAT.3	VDDFTH.2	VDDFTH.1	VDDFTH.0

Bit	Symbol	Function
VDDFCtl.7	–	
VDDFCtl.6	FOVRVDDF	Setting this bit high will allow the VDDFLT(2:0) bits set in this register to control the VDDFault threshold. When this bit is set low, the VDDFault threshold will be set to the factory default setting of 2.3V*.
VDDFCtl.5	VDDFLTEN	Set = 1 will disable VDD Fault operation.
VDDFCtl.4	–	
VDDFCtl.3	–	
VDDFCtl.2	VDDFTH.2	VDD Fault Threshold. Bit value(2:0) VDDFault voltage 000 2.3 (nominal default) 001 2.4 010 2.5 011 2.6 100 2.7 101 2.8 110 2.9 111 3.0
VDDFCtl.1	VDDFTH.1	
VDDFCtl.0	VDDFTH.0	

* Note: The V_{DD} Fault factory default can be set to any threshold as defined by bits VDDFTH(2:0). The 73S1215F has the capability to burn fuses at the factory to set the factory default to any of these voltages. Contact Teridian for further details.

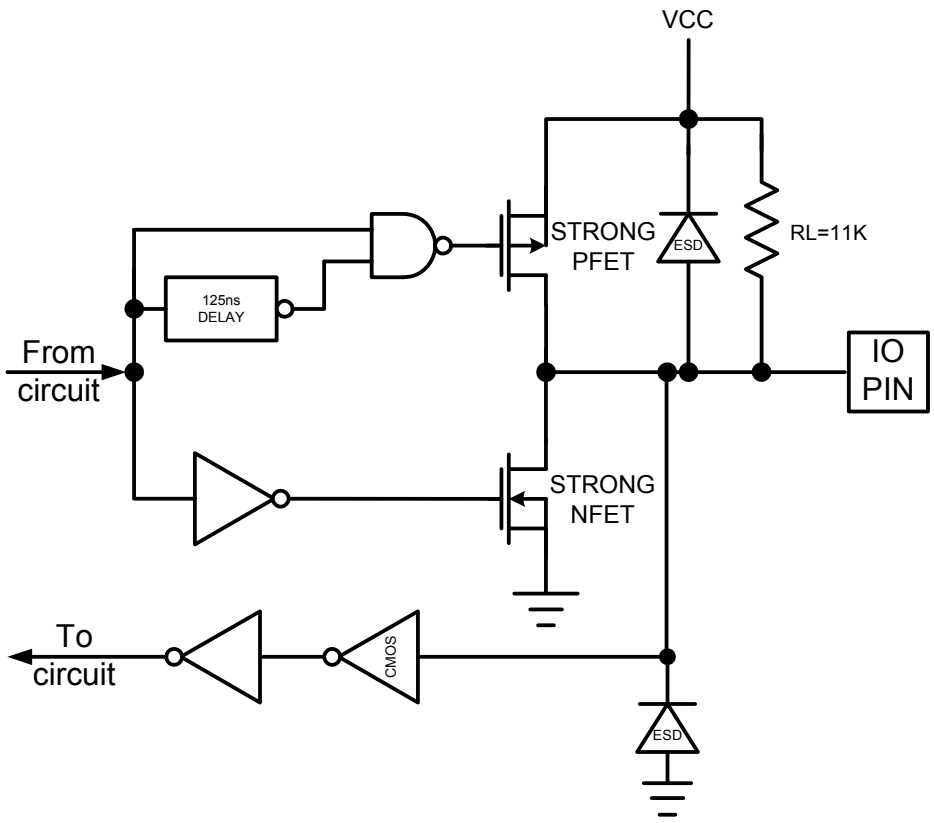


Figure 40: Smart Card I/O Circuit

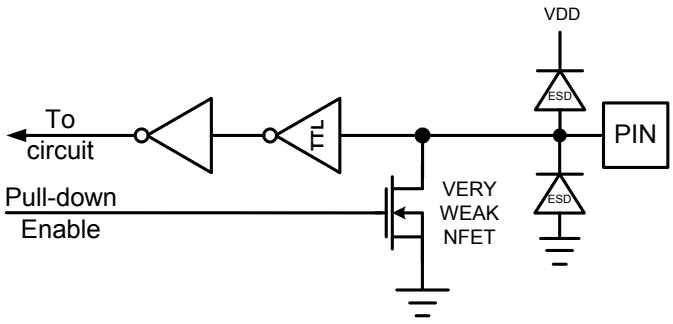


Figure 41: PRES Input Circuit