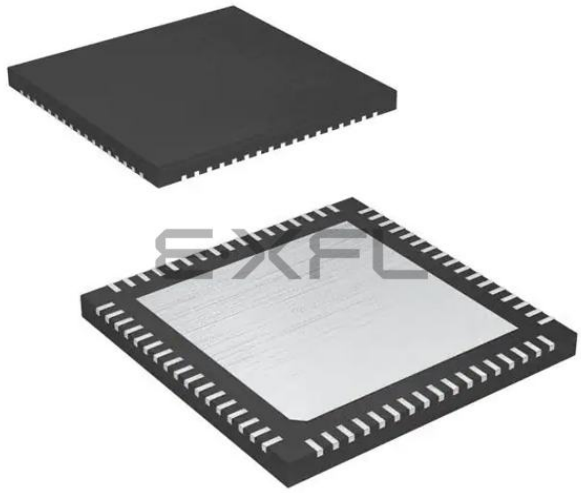
Analog Devices Inc./Maxim Integrated - 73S1215F-68IMR/F/P Datasheet



Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Discontinued at Digi-Key
Core Processor	80515
Core Size	8-Bit
Speed	24MHz
Connectivity	I²C, SmartCard, UART/USART, USB
Peripherals	LED, POR, WDT
Number of I/O	9
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	68-VFQFN Exposed Pad
Supplier Device Package	68-QFN (8x8)
Purchase URL	https://www.e-xfl.com/product-detail/analog-devices/73s1215f-68imr-f-p

Internal Data Memory: The Internal data memory provides 256 bytes (0x00 to 0xFF) of data memory. The internal data memory address is always one byte wide and can be accessed by either direct or indirect addressing. The Special Function Registers occupy the upper 128 bytes**. This SFR area is available only by direct addressing. Indirect addressing accesses the upper 128 bytes of Internal RAM.**

The lower 128 bytes contain working registers and bit-addressable memory. The lower 32 bytes form four banks of eight registers (R0-R7). Two bits on the program memory status word (PSW) select which bank is in use. The next 16 bytes form a block of bit-addressable memory space at bit addresses 0x00-0x7F. All of the bytes in the lower 128 bytes are accessible through direct or indirect addressing. Table 4 shows the internal data memory map.

Table 4: Internal Data Memory Map

<table>
<tr><th>Address</th><th>Direct Addressing</th><th>Indirect Addressing</th></tr>
<tr><td>0xFF</td><td rowspan="2">Special Function Registers (SFRs)</td><td rowspan="2">RAM</td></tr>
<tr><td>0x80</td></tr>
<tr><td>0x7F</td><td colspan="2" rowspan="2">Byte-addressable area</td></tr>
<tr><td>0x30</td></tr>
<tr><td>0x2F</td><td colspan="2" rowspan="2">Byte or bit-addressable area</td></tr>
<tr><td>0x20</td></tr>
<tr><td>0x1F</td><td colspan="2" rowspan="2">Register banks R0…R7 (x4)</td></tr>
<tr><td>0x00</td></tr>
</table>

External Data Memory: While the 80515 can address up to 64KB of external data memory in the space from 0x0000 to 0xFFFF, only the memory ranges shown in Figure 2 contain physical memory. The 80515 writes into external data memory when the MPU executes a MOVX @Ri,A or MOVX @DPTR,A instruction. The MPU reads external data memory by executing a MOVX A,@Ri or MOVX A,@DPTR instruction.

There are two types of instructions, differing in whether they provide an eight-bit or sixteen-bit indirect address to the external data RAM.

In the first type (MOVX A,@Ri), the contents of R0 or R1, in the current register bank, provide the eight lower-ordered bits of address. This method allows the user access to the first 256 bytes of the 2KB of external data RAM. In the second type of MOVX instruction (MOVX A,@DPTR), the data pointer generates a sixteen-bit address.

1.5 Special Function Registers (SFRs)

The 73S1215F utilizes numerous SFRs to communicate with the 73S1215F s many peripherals. This results in the need for more SFR locations outside the direct address IRAM space (0x80 to 0xFF). While some peripherals are mapped to unused IRAM SFR locations, additional SFRs for the USB, smart card and other peripheral functions are mapped to the top of the XRAM data space (0xFC00 to 0xFFFF).

1.5.1 Internal Data Special Function Registers (SFRs)

A map of the Special Function Registers is shown in Table 6.

Table 6: IRAM Special Function Registers Locations

Hex\ Bin	X000	X001	X010	X011	X100	X101	X110	X111	Bin/ Hex
F8									FF
F0	B								F7
E8									EF
E0	A								E7
D8	BRCON								DF
D0	PSW	**KCOL**	**KROW**	**KSCAN**	**KSTAT**	**KSIZE**	**KORDERL**	**KORDERH**	D7
C8	T2CON								CF
C0	IRCON								C7
B8	IEN1	IP1	S0RELH	S1RELH					BF
B0			**FLSHCTL**					**PGADDR**	B7
A8	IEN0	IP0	S0RELL						AF
A0	**USR8**	**UDIR8**							A7
98	S0CON	S0BUF	IEN2	S1CON	S1BUF	S1RELL			9F
90	**USR70**	**UDIR70**	DPS		**ERASE**				97
88	TCON	TMOD	TL0	TL1	TH0	TH1	CKCON	**MCLKCTL**	8F
80		SP	DPL	DPH	DPL1	DPH1	WDTREL	PCON	87

Only a few addresses are used, the others are not implemented. SFRs specific to the 73S1215F are shown in **bold** print (gray background). Any read access to unimplemented addresses will return undefined data, while most write access will have no effect. However, a few locations are reserved and not user configurable in the 73S1215F. **Writes to the unused SFR locations can affect the operation of the core and therefore must not be written to. This applies to all the SFR areas in both the IRAM and XRAM spaces. In addition, all unused bit locations within valid SFR registers must be left in their default (power on default) states.**

Power Control Register 0 (PCON): 0x87 ← 0x00

The SMOD bit used for the baud rate generator is setup via this register.

Table 19: The PCON Register

MSB LSB

SMOD	–	–	–	GF1	GF0	STOP	IDLE

Bit	Symbol	Function
PCON.7	SMOD	If SM0D = 1, the baud rate is doubled.
PCON.6	–	
PCON.5	–	
PCON.4	–	
PCON.3	GF1	General purpose flag 1.
PCON.2	GF0	General purpose flag 1.
PCON.1	STOP	Sets CPU to Stop mode.
PCON.0	IDLE	Sets CPU to Idle mode.

1.7.7 User (USR) Ports

The 73S1215F includes 9 pins of general purpose digital I/O (GPIO). On reset or power-up, all USR pins are inputs until they are configured for the desired direction. The pins are configured and controlled by the USR and UDIR SFRs. Each pin declared as USR can be configured independently as an input or output with the bits of the UDIRn registers. Table 48 lists the direction registers and configurability associated with each group of USR pins. USR pins 0 to 7 are multiple use pins that can be used for general purpose I/O, external interrupts and timer control.

Table 49 shows the configuration for a *USR* pin through its associated bit in its UDIR register. Values read from and written into the GPIO ports use the data registers USR70 and USR8. Note: After reset, all USR pins are defaulted as inputs and pulled up to VDD until any write to the corresponding UDIR register is performed. This insures all USR pins are set to a known value until set by the firmware. Unused USR pins can be set for output if unused and unconnected to prevent them from floating. Alternatively, unused USR pins can be set for input and tied to ground or V_{DD}.

Table 48: Direction Registers and Internal Resources for DIO Pin Groups

USR Pin Group	Type	Direction Register Name	Direction Register (SFR) Location	Data Register Name	Data Register (SFR) Location
USR_0…USR_7	Multi-use	UDIR70	0x91 [7:0]	USR70	0x90 [7:0]
USR_8	GPIO only	UDIR8	0xA1 [0]	USR8	0xA0 [0]

Table 49: UDIR Control Bit

	UDIR Bit	
	0	1
USR Pin Function	output	input

Four XRAM SFR registers (USRIntCtl1, USRIntCtl2, USRIntCtl3, and USRIntCtl4) control the use of the USR [7:0] pins. Each of the USR [7:0] pins can be configured as GPIO or individually be assigned an internal resource such as an interrupt or a timer/counter control. Each of the four registers contains two 3-bit configuration words named UxIS (where x corresponds to the USR pin). The control resources selectable for the USR pins are listed in Table 50through Table 54. If more than one input is connected to the same resource, the resources are combined using a logical OR.

Table 50: Selectable Controls Using the UxIS Bits

UxIS Value	Resource Selected for USRx Pin
0	None
1	None
2	T0 (counter0 gate/clock)
3	T1 (counter1 gate/clock)
4	Interrupt 0 rising edge/high level on USRx
5	Interrupt 1 rising edge/high level on USRx
6	Interrupt 0 falling edge/low level on USRx
7	Interrupt 1 falling edge/low level on USRx

Note: x denotes the corresponding USR pin. Interrupt edge or level control is assigned in the IT0 and IT1 bits in the TCON register.

Figure 11 shows the timing of the I²C read mode.

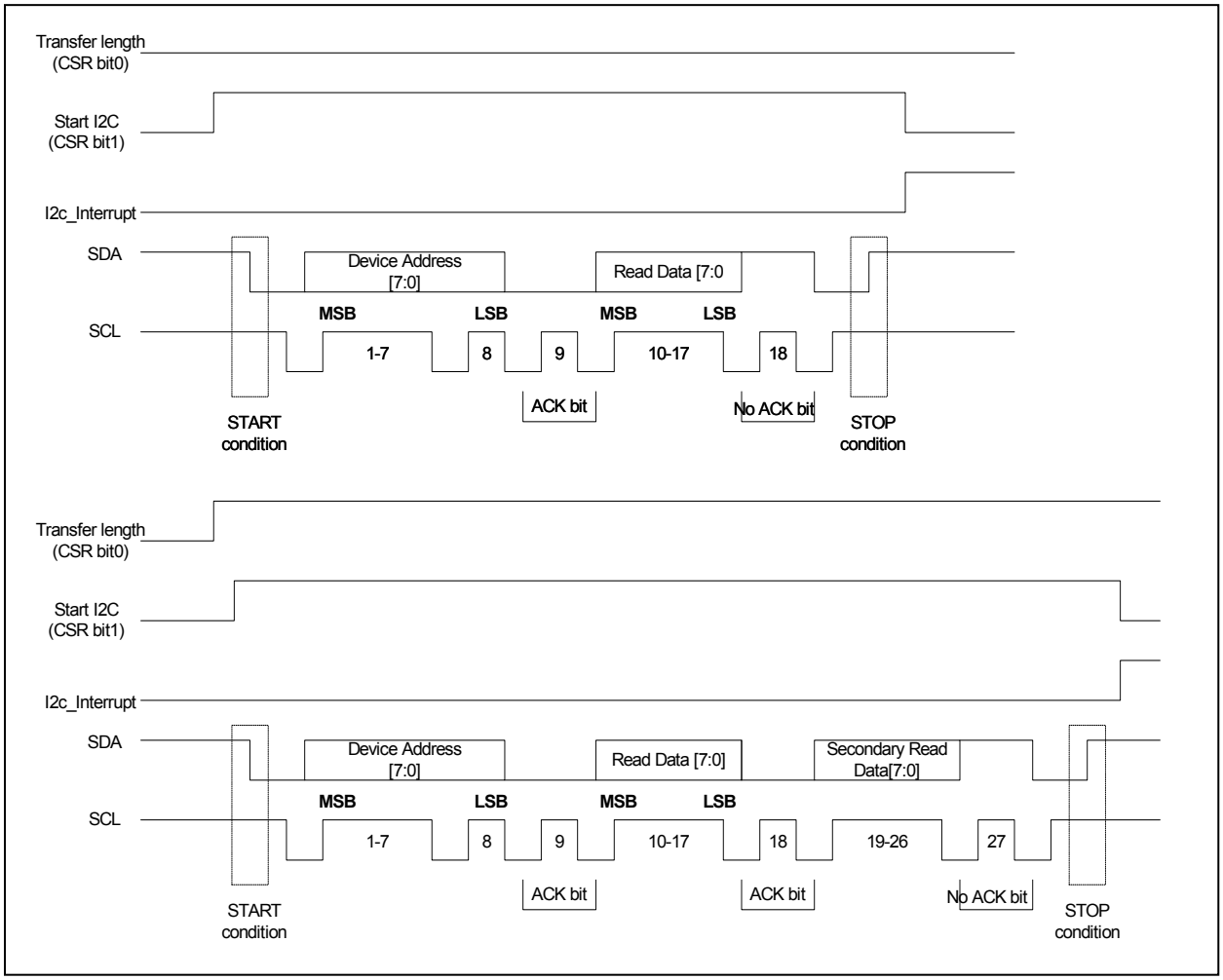


Figure 11: I²C Read Operation

I2C Secondary Write Data Register (SWDR): 0XFF82 ← 0x00

Table 65: The SWDR Register

MSB							LSB
SWDR.7	SWDR.6	SWDR.5	SWDR.4	SWDR.3	SWDR.2	SWDR.1	SWDR.0

Bit	Function
SWDR.7	Second Data byte to be written to the I^2C slave device if bit 0 (I2CLEN) of the Control and Status register (CSR) is set = 1.
SWDR.6	
SWDR.5	
SWDR.4	
SWDR.3	
SWDR.2	
SWDR.1	
SWDR.0	

I2C Read Data Register (RDR): 0XFF83 ← 0x00

Table 66: The RDR Register

MSB							LSB
RDR.7	RDR.6	RDR.5	RDR.4	RDR.3	RDR.2	RDR.1	RDR.0

Bit	Function
RDR.7	Data read from the I^2C slave device.
RDR.6	
RDR.5	
RDR.4	
RDR.3	
RDR.2	
RDR.1	
RDR.0	

Keypad Scan Time Register (KSIZE): 0xD5 ← 0x00

This register is not applicable when HWSCEN is not set. Unused row inputs should be connected to VDD.

Table 74: The KSIZE Register

MSB							LSB
–	–	ROWSIZ.2	ROWSIZ.1	ROWSIZ.0	COLSIZ.2	COLSIZ.1	COLSIZ.0

Bit	Symbol	Function
KSIZE.7	–	
KSIZE.6	–	
KSIZE.5	ROWSIZ.2	Defines the number of rows in the keypad. Maximum number is 6 given the number of row pins on the package. Allows for a reduced keypad size for scanning.
KSIZE.4	ROWSIZ.1	
KSIZE.3	ROWSIZ.0	
KSIZE.2	COLSIZ.2	Defines the number of columns in the keypad. Maximum number is 5 given the number of column pins on the package. Allows for a reduced keypad size for scanning.
KSIZE.1	COLSIZ.1	
KSIZE.0	COLSIZ.0	

Keypad Column LS Scan Order Register (KORDERL): 0xD6 ← 0x00

In registers KORDERL and KORDERH, Column Scan Order(14:0) is grouped into 5 sets of 3 bits each. Each set determines which column (COL(4:0) pin) to activate by loading the column number into the 3 bits. When in HW_Scan_Enable mode, the hardware will step through the sets from 1Col to 5Col (up to the number of columns in Colsize) and scan the column defined in the 3 bits. To scan in sequential order, set a counting pattern with 0 in set 0, and 1 in set 1,and 2 in set 2, and 3 in set 3, and 4 in set 4. The firmware should update this as part of the interrupt service routine so that the new scan order is loaded prior to the next key being pressed. For example, to scan COL(0) first, 1Col(2:0) should be loaded with 000'b. To scan COL(4) fifth, 5Col(2:0) should be loaded with 100'b.

Table 75: The KORDERL Register

MSB							LSB
3COL.1	3COL.0	2COL.2	2COL.1	2COL.0	1COL.2	1COL.1	1COL.0

Bit	Symbol	Function
KORDERL.7	3COL.1	Column to scan 3rd (lsb's).
KORDERL.6	3COL.0	
KORDERL.5	2COL.2	Column to scan 2nd.
KORDERL.4	2COL.1	
KORDERL.3	2COL.0	
KORDERL.2	1COL.2	Column to scan 1st.
KORDERL.1	1COL.1	
KORDERL.0	1COL.0	

1.7.13 Emulator Port

The emulator port, consisting of the pins E_RST, E_TCLK and E_RXTX, provides control of the MPU through an external in-circuit emulator. The E_TBUS[3:0] pins, together with the E_ISYNC/BRKRQ, add trace capability to the emulator. The emulator port is compatible with the ADM51 emulators manufactured by Signum Systems.

If code trace capability is needed on this interface, 20pF capacitors (to ground) need to be added to allow the trace function capability to run properly. These capacitors should be attached to the TBUS0:3 and ISBR signals.

1.7.14 USB Interface

The 73S1215F provides a single interface, full speed -12Mbps - USB device port as per the *Universal Serial Bus Specification, Revision 2.0* (backward compatible with USB 1.1). USB circuitry gathers the transceiver, the Serial Interface Engine (SIE), and the data buffers. An internal pull-up to V_{DD} on D+ indicates that the device is a full speed device attached to the USB bus (allows full speed recognition by the host without adding any external components). When using the USB interface, V_{DD} must be between 3.0V – 3.6V in order to meet the USB VOH requirement. The interface is highly configurable under firmware control. Control (Endpoint 0), Interrupt IN, Bulk IN and Bulk OUT transfers are supported. Four endpoints are supported and are configured by firmware:

- Endpoint 0, the default (Control) endpoint as required by the *Universal Serial Bus Specification*, is used to exchange control and status information between the 73S1215F and the USB host.
- Bulk IN Endpoint #1
- Bulk OUT Endpoint #1
- Interrupt IN Endpoint #2
- The USB block contains several FIFOs used for communication.
- There is a 128 byte RAM FIFO for each BULK endpoint. Maximum Bulk packet size is 64 bytes.
- There is a 32 byte RAM FIFO for the interrupt endpoint. Maximum Interrupt packet size is 16 bytes.
- There is a 16 byte RAM FIFO for the control endpoint. Maximum Control packet size is 16 bytes.

Figure 14 shows the simplified block diagram of the USB interface.

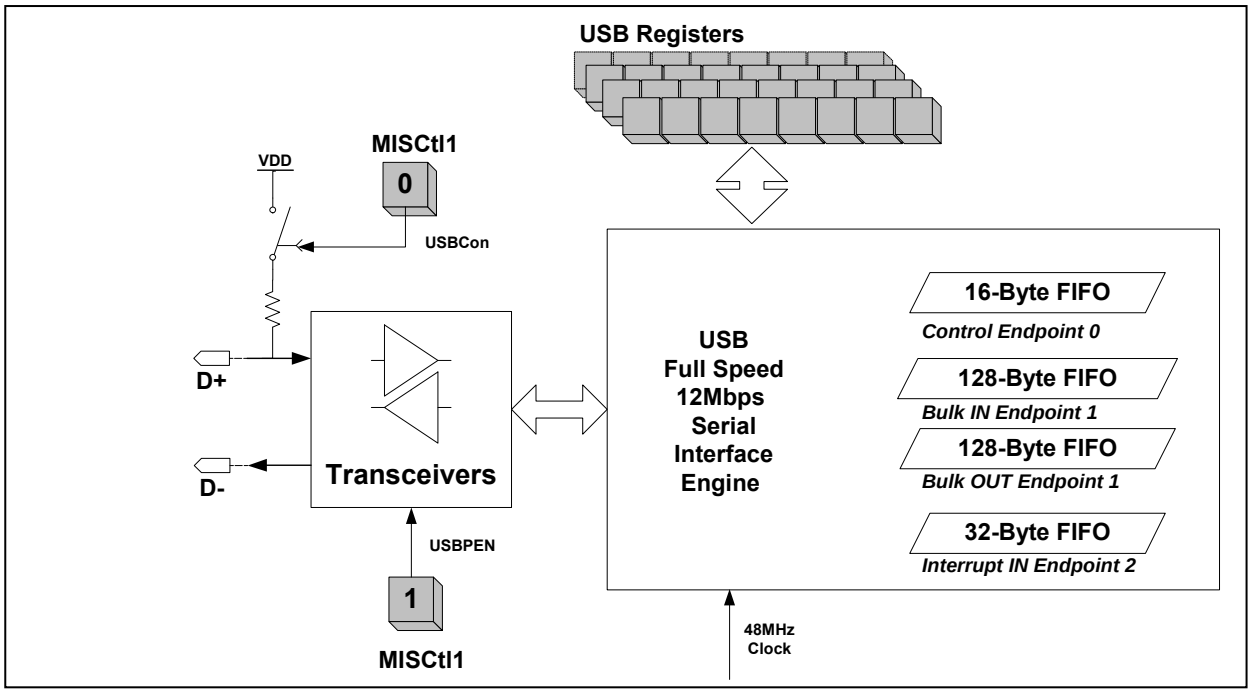


Figure 14: USB Block Diagram

1.7.15 Smart Card Interface Function

The 73S1215F integrates one ISO-7816 (T=0, T=1) UART, one complete ICC electrical interface as well as an external smart card interface to allow multiple smart cards to be connected using the Teridian 8010 family of interface devices. Figure 15 shows the simplified block diagram of the card circuitry (UART + interfaces), with detail of dedicated XRAM registers.

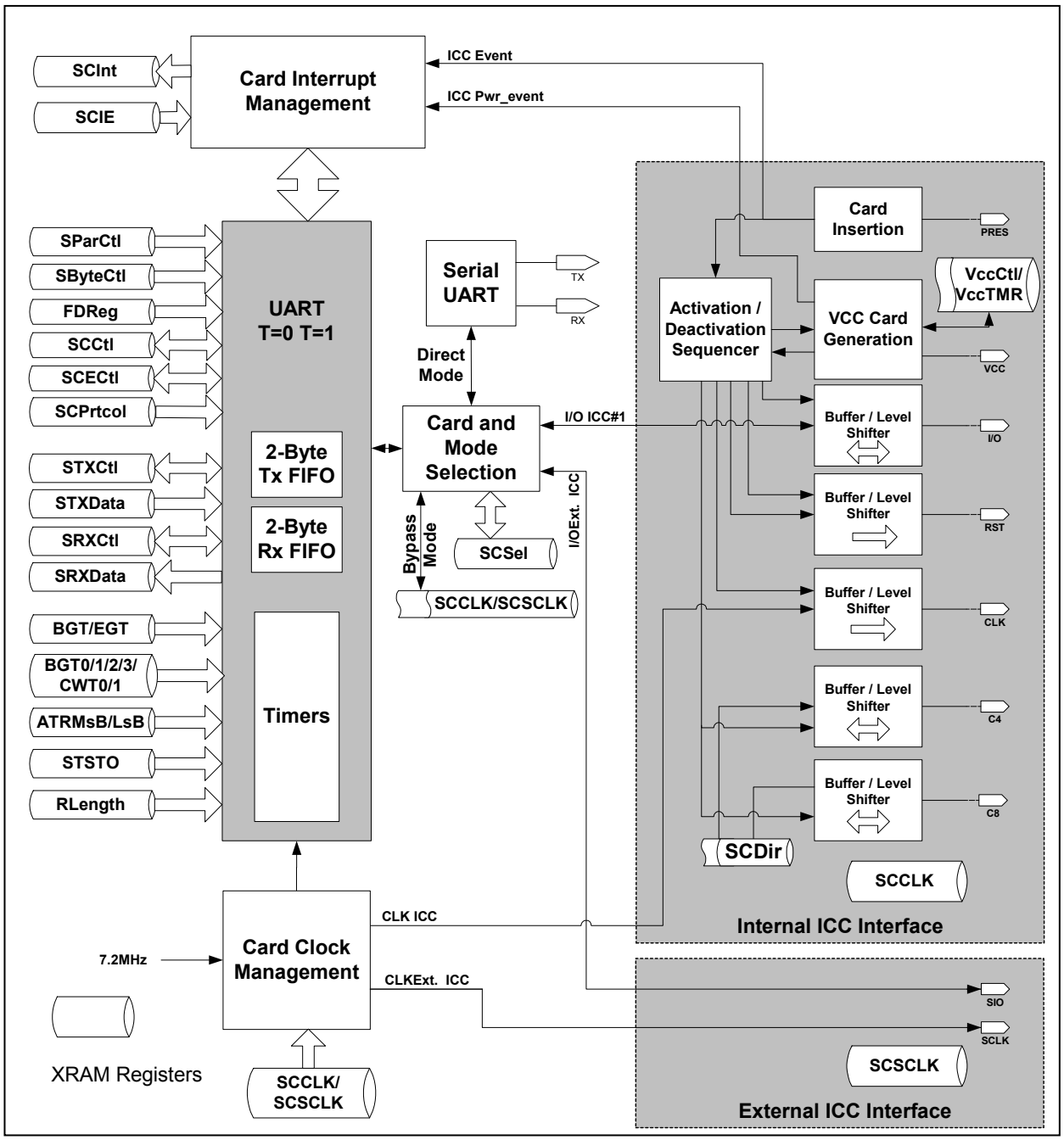


Figure 15: Smart Card Interface Block Diagram

Card interrupts are managed through two dedicated registers SCIE (Interrupt Enable to define which interrupt is enabled) and SCInt (Interrupt status). They allow the firmware to determine the source of an interrupt, that can be a card insertion / removal, card power fault, or a transmission (TX) or reception (RX) event / fault. It should be noted that even when card clock is disabled, an ICC interrupt can be generated

on a card insertion / removal to allow power saving modes. Card insertion / removal is generated from the respective card switch detection inputs (whose polarity is programmable).

The built-in ICC Interface has a low dropout regulator (V_{CC} generator) capable of driving 1.8V, 3.0V and 5.0V smart cards in accordance with the ISO 7816-3 and EMV4.0 standards. This converter requires a separate 5.0V input supply source designated as VPC. Auxiliary I/O lines C4 and C8 are only provided for the built-in interface. If support for the auxiliary lines is necessary for the external interfaces, they need to be handled manually through the USR GPIO pins. The external 8010 devices directly connect the I/O (SIO) and clock (SCLK) signals and control is handled via the I^2C interface.

Figure 16 shows how multiple 8010 devices can be connected to the 73S1215F.

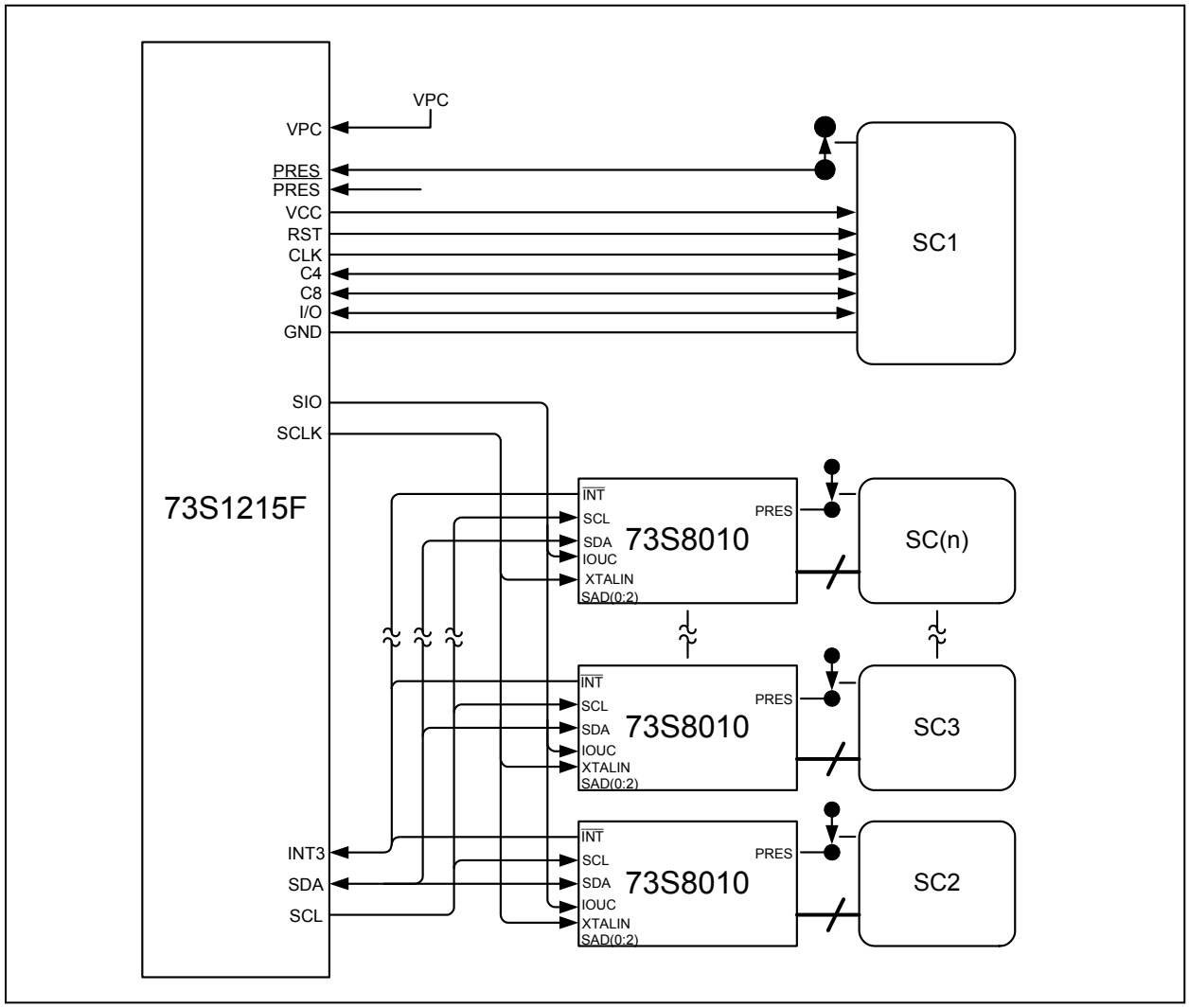
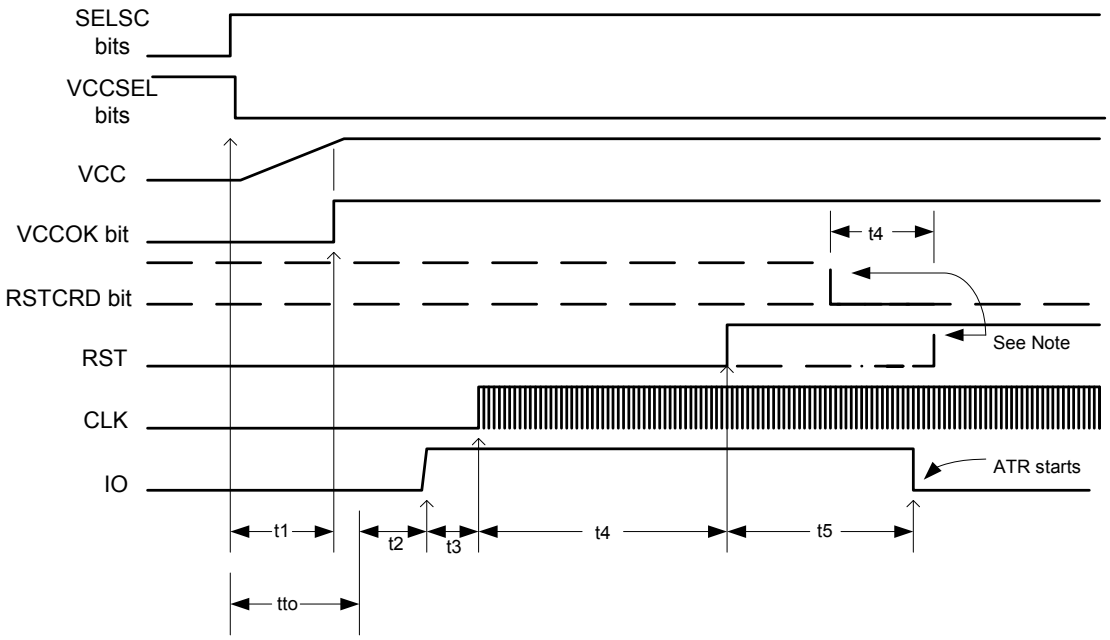


Figure 16: Smart Card Interface Block Diagram

Smart card RST, I/O and CLK, C4, C8 shall be low before the end of the deactivation sequence. Figure 18 shows the timing for a deactivation sequence.



t1: SELSC.1 bit set (selects internal ICC interface) and a non-zero value in VCCSEL bits (calling for a value of Vcc of 1.8, 3.0, or 5.0 volts) will begin the activation sequence. t1 is the time for Vcc to rise to acceptable level, declared as Vcc OK (bit VCCOK gets set). This time depends on filter capacitor value and card Icc load.

tto: The time allowed for Vcc to rise to Vcc OK status after setting of the VCCSEL bits. This time is generated by the VCCTMR counter. If Vcc OK is not set, (bit VCCOK) at this time, a deactivation will be initiated. VCCSEL bits are not automatically cleared. The firmware must clear the VCCSEL bits before starting a new activation.

t2: Time from VCCTMR timeout and VCC OK to IO reception (high), typically 2-3 CLK cycles if RDYST = 0. If RDYST = 1, t2 starts when VCCOK = 1.

t3: Time from IO = high to CLK start, typically 2-3 CLK cycles.

t4: Time allowed for start of CLK to de-assertion of RST. Programmable by RLength register.

t5: Time allowed for ATR timeout, set by the STSTO register.

Note: If the RSTCRD bit is set, RST is asserted (low). Upon clearing RSTCRD bit, RST will be de-asserted after t4.

Figure 17: Asynchronous Activation Sequence Timing

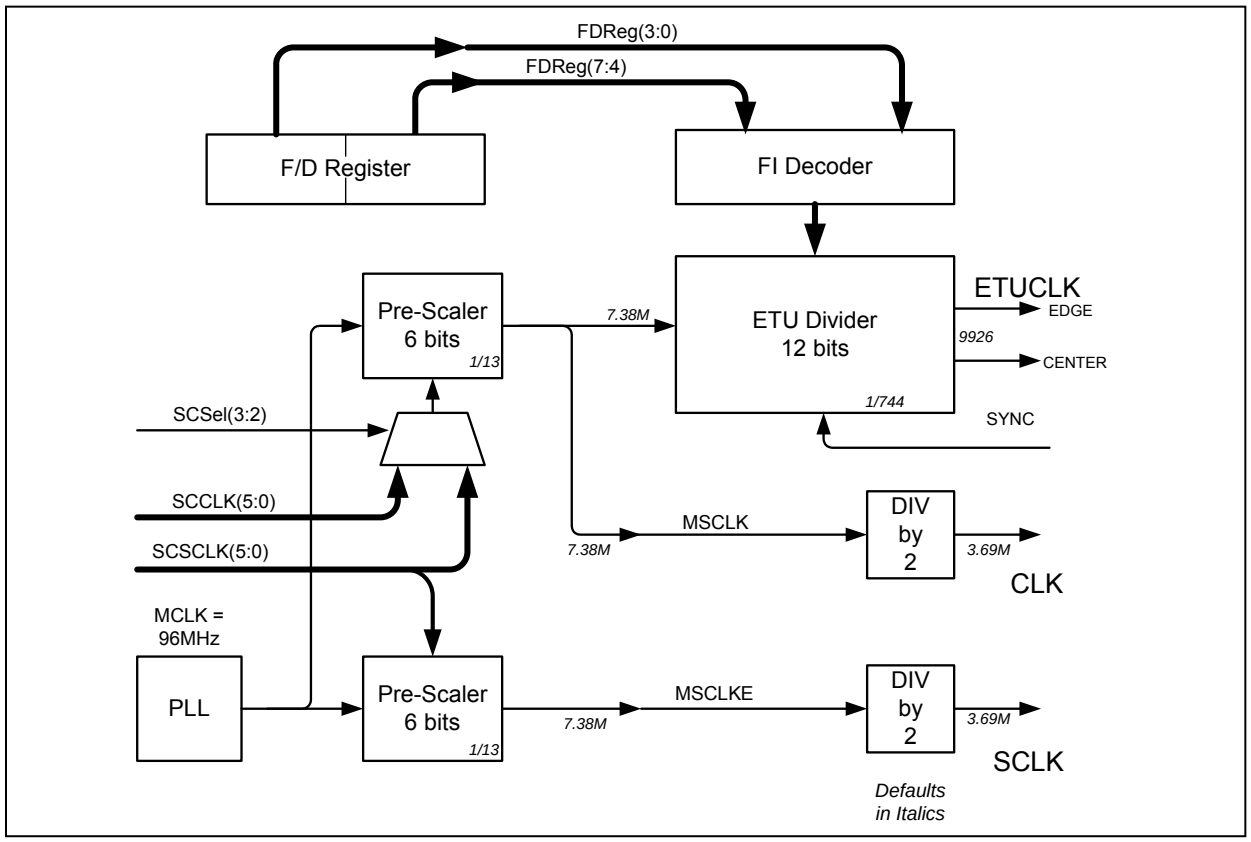


Figure 19: Smart Card CLK and ETU Generation

There are two, two-byte FIFOs that are used to buffer transmit and receive data. During a T=0 processing, if a parity error is detected by the 73S1215F during message reception, an error signal (BREAK) will be generated to the smart card. The byte received will be discarded and the firmware notified of the error. Break generation and receive byte dropping can be disabled under firmware control. During the transmission of a byte, if an error signal (BREAK) is detected, the last byte is retransmitted again and the firmware notified. Retransmission can be disabled by firmware. When a correct byte is received, an interrupt is generated to the firmware, which then reads the byte from the receive FIFO. Receive overruns are detected by the hardware and reported via an interrupt. During transmission of a message, the firmware will write bytes into the transmit FIFO. The hardware will send them to the smart card. When the last byte of a message has been written, the firmware will need to set the LASTTX bit in the STXCtl SFR. This will cause the hardware to insert the CRC/LRC if in a T=1 protocol mode. CRC/LRC generation/checking is only provided during T=1 processing. Firmware will need to instruct the smart function to go into receive mode after this last transmit data byte if it expects a response from the smart card. At the end of the smart card response, the firmware will put the interface back into transmit mode if appropriate.

The hardware can check for the following card-related timeouts:

- Character Waiting Time (CWT)
- Block Waiting Time (BWT)
- Initial Waiting Time (IWT)

The firmware will load the Wait Time registers with the appropriate value for the operating mode at the appropriate time. Figure 20 shows the guard, block, wait and ATR time definitions. If a timeout occurs, an interrupt will be generated and the firmware can take appropriate recovery steps. Support is provided for adding additional guard times between characters (Extra Guard Time register) and between the last byte received by the 73S1215F and the first byte transmitted by the 73S1215F Block Guard Time register (BGT). Other than the protocol checks described above, the firmware is responsible for all protocol checking and error recovery.

SRX Data Register (SRXData): 0xFE09 ← 0x00

Table 89: The SRXData Register

MSB LSB

SRXDAT.7	SRXDAT.6	SRXDAT.5	SRXDAT.4	SRXDAT.3	SRXDAT.2	SRXDAT.1	SRXDAT.0

Bit	Function
SRXData.7	(Read only) Data received from the smart card. Data received from the smart card gets stored in a FIFO that is read by the firmware.
SRXData.6	
SRXData.5	
SRXData.4	
SRXData.3	
SRXData.2	
SRXData.1	
SRXData.0	

Smart Card Control Register (SCCtl): 0xFE0A ← 0x21

This register is used to monitor reception of data from the smart card.

Table 90: The SCCtl Register

MSB LSB

RSTCRD	–	IO	IOD	C8	C4	CLKLVL	CLKOFF

Bit	Symbol	Function
SCCtl.7	RSTCRD	1 = Asserts the RST (set RST = 0) to the smart card interface, 0 = De-assert the RST (set RST = 1) to the smart card interface. Can be used to extend RST to the smart card. Refer to the RLength register description. This bit is operational in all modes and can be used to extend RST during activation or perform a "Warm Reset" as required. In auto-sequence mode, this bit should be set = 0 to allow the sequencer to de-assert RST per the RLength parameters. In sync mode (see the SPrtcol register) the sense of this bit is non-inverted, if set =1 , RST = 1, if set = 0, RST = 0. Rlen has no effect on Reset in sync mode.
SCCtl.6	–	
SCCtl.5	IO	Smart Card I/O. Read is state of I/O signal (Caution, this signal is not synchronized to the MPU clock). In Bypass mode, write value is state of signal on I/O. In sync mode, this bit will contain the value of I/O pin on the latest rising edge of CLK.
SCCtl.4	IOD	Smart Card I/O Direction control Bypass mode or sync mode. 1 = input (default), 0 = output.
SCCtl.3	C8	Smart Card C8. When C8 is an output, the value written to this bit will appear on the C8 line. The value read when C8 is an output is the value stored in the register. When C8 is an input, the value read is the value on the C8 pin (Caution, this signal is not synchronized to the MPU clock). When C8 is an input, the value written will be stored in the register but not presented to the C8 pin.
SCCtl.2	C4	Smart Card C4. When C4 is an output, the value written to this bit will appear on the C4 line. The value read when C4 is an output is the value stored in the register. When C4 is an input, the value read is the value on the C4 pin (Caution, this signal is not synchronized to the MPU clock). When C4 is an input, the value written will be stored in the register but not presented to the C4 pin.
SCCtl.1	CLKLVL	1 = High, 0 = Low. If CLKOFF is set = 1, the CLK to smart card will be at the logic level indicated by this bit. If in bypass mode, this bit directly controls the state of CLK.
SCCtl.0	CLKOFF	0 = CLK is enabled. 1 = CLK is not enabled. When asserted, the CLK will stop at the level selected by CLKLVL. This bit has no effect if in bypass mode.

Protocol Mode Register (SPrtcol): 0xFE0D ← 0x03

This register determines the protocol to be use when communicating with the selected smart card. This register should be updated as required when switching between smart card interfaces.

Table 93: The SPrtcol Register

MSB LSB

SCISYN	MOD9/8B	SCESYN	0	TMODE	CRCEN	CRCMS	RCVATR

Bit	Symbol	Function
SPrtcol.7	SCISYN	Smart Card Internal Synchronous mode – Configures internal smart card interface for synchronous mode. This mode routes the internal interface buffers for RST, IO, C4, C8 to SCCtl register bits for direct firmware control. CLK is generated by the ETU counter.
SPrtcol.6	MOD9/8B	Synchronous 8/9 bit mode select – For sync mode, in protocols with 9-bit words, set this bit. The first eight bits read go into the RX FIFO and the ninth bit read will be stored in the IO (or SIO) data bit of the SRXCtl register.
SPrtcol.5	SCESYN	Smart Card External Synchronous mode – Configures External Smart Card interface for synchronous mode. This mode routes the external smart card interface buffers for SIO to SCECtl register bits for direct firmware control. SCLK is generated by the ETU counter.
SPrtcol.4	0	Reserved bit, must always be set to 0.
SPrtcol.3	TMODE	Protocol mode select – 0: T=0, 1: T=1. Determines which smart card protocol is to be used during message processing.
SPrtcol.2	CRCEN	CRC Enable – 1 = Enabled, 0 = Disabled. Enables the checking/generation of CRC/LRC while in T=1 mode. Has no effect in T=0 mode. If enabled and a message is being transmitted to the smart card, the CRC/LRC will be inserted into the message stream after the last TX byte is transmitted to the smart card. If enabled, CRC/LRC will be checked on incoming messages and the value made available to the firmware via the CRC LS/MS registers.
SPrtcol.1	CRCMS	CRC Mode Select - 1 = CRC, 0 = LRC. Determines type of checking algorithm to be used.
SPrtcol.0	RCVATR	Receive ATR – 1 = Enable ATR timeout, 0 = Disable ATR timeout. Set by firmware after the smart card has been turned on and the hardware is expecting ATR.

3 Electrical Specification

3.1 Absolute Maximum Ratings

Operation outside these rating limits may cause permanent damage to the device. The smart card interface pins are protected against short circuits to V_{CC}, ground, and each other.

Parameter	Rating
DC Supply voltage, V_{DD}	-0.5 to 4.0 VDC
Supply Voltage V_{PC}	-0.5 to 6.5 VDC
Storage Temperature	-60 to 150°C
Pin Voltage (except card interface)	-0.3 to (V_{DD}+0.5) VDC
Pin Voltage (card interface)	-0.3 to (V_{CC}+0.5) VDC
ESD tolerance (except card interface)	+/- 2KV
ESD tolerance (card interface)	+/- 6KV
Pin Current	± 200 mA

Note: ESD testing on smart card pins is HBM condition, 3 pulses, each polarity referenced to ground.
Note: Smart Card pins are protected against shorts between any combinations of Smart Card pins.

3.2 Recommended Operating Conditions

Unless otherwise noted all specifications are valid over these temperatures and supply voltage ranges:

Parameter	Rating
DC Voltage Supply VDD	2.7 to 3.6 VDC
DC Voltage Supply VDD for USB operation	3.0 to 3.6 VDC
Supply Voltage V_{PC} for Class A-B-C Reader	4.75 to 6.0 VDC
Ambient Operating Temperature (Ta)	-40°C to +85°C

3.6 USB Interface Requirements

Parameter		Condition	Min	Typ.	Max	Unit
Receiver Parameters						
Differential input sensitivity	VDI	|(DP)-(DM)|	0.2			V
Differential common mode range	VCM	Includes VDI range	0.8		2.5	V
Single ended receiver threshold	VSE		0.8		2.0	V
Transmitter Levels						
Low Level Output Voltage	VOL	USBCon = 1 (DP pullup enabled)			0.3	V
High Level Output Voltage	VOH	15KΩ resistor to ground	VDD – 0.1V		VDD	V
Output Resistance (1)						
Driver output resistance	ZDRV	Steady state drive[1]	28		44	Ω
PD Pullup Resistor (to VDD)	Zpu	USBCon = 1	1.2	1.5	1.8	kΩ
Transceiver Power Requirements						
Operating supply current(output)	IPSO	Outputs enabled			5	mA
Operating supply current (input)	IPSI	Outputs Hi-Z			1	mA
Supply current in powerdown	IPDN				10	nA
Supply current in suspend.	IPSS				10	nA

[1] External source (series) termination resistors of 24Ω must be included on circuit board.

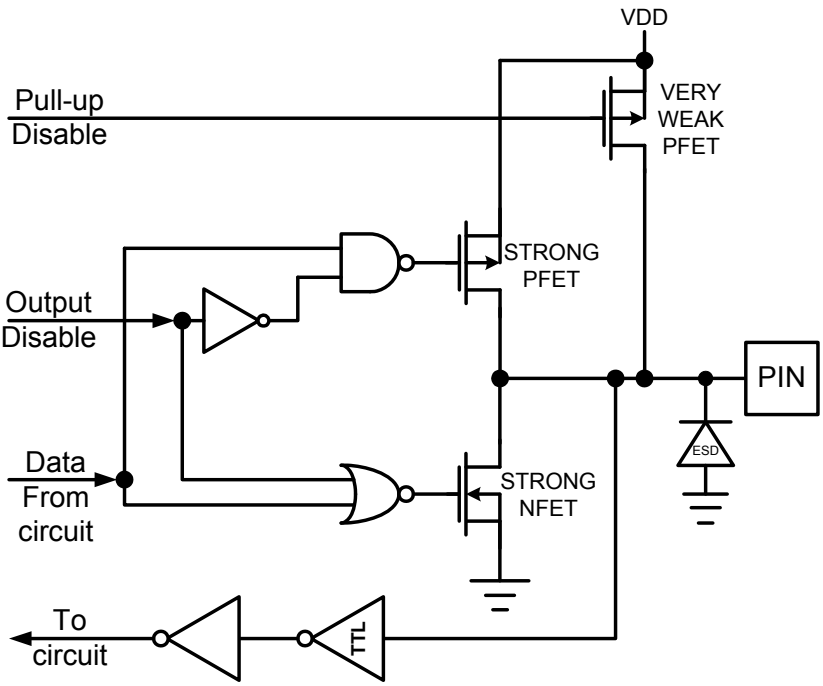


Figure 31: Digital I/O with Pull Up Circuit

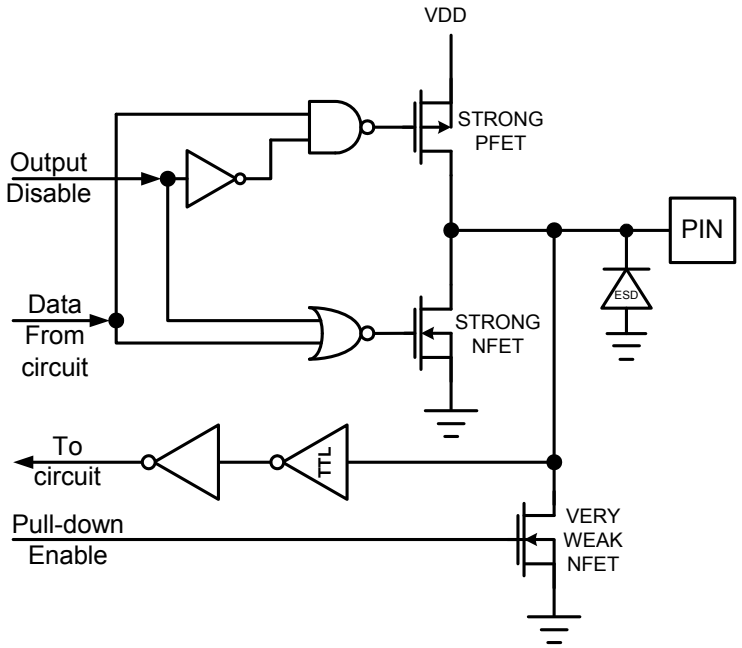


Figure 32: Digital I/O with Pull-Down Circuit

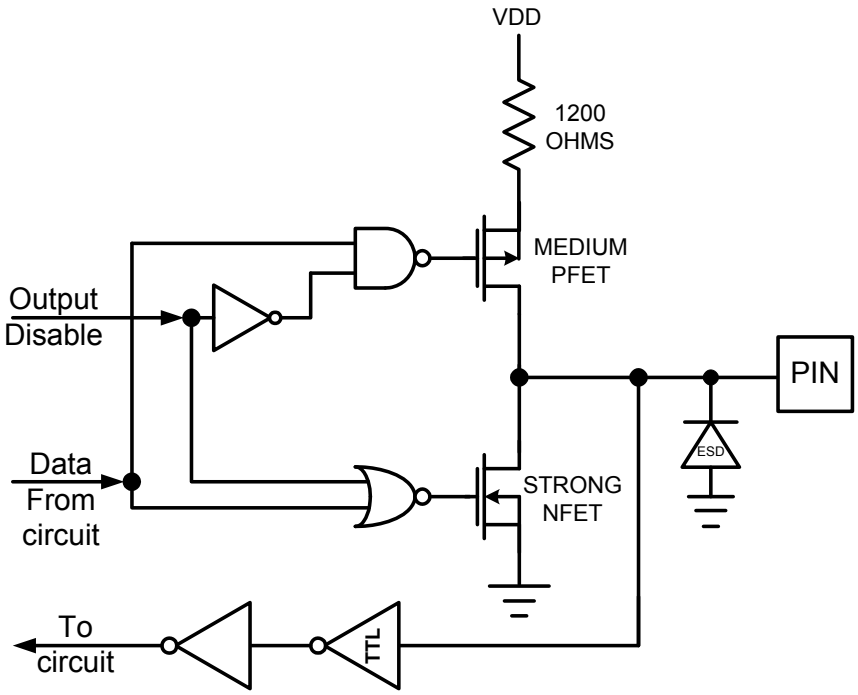


Figure 35: Keypad Column Circuit