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### Understanding [Embedded - FPGAs \(Field Programmable Gate Array\)](#)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

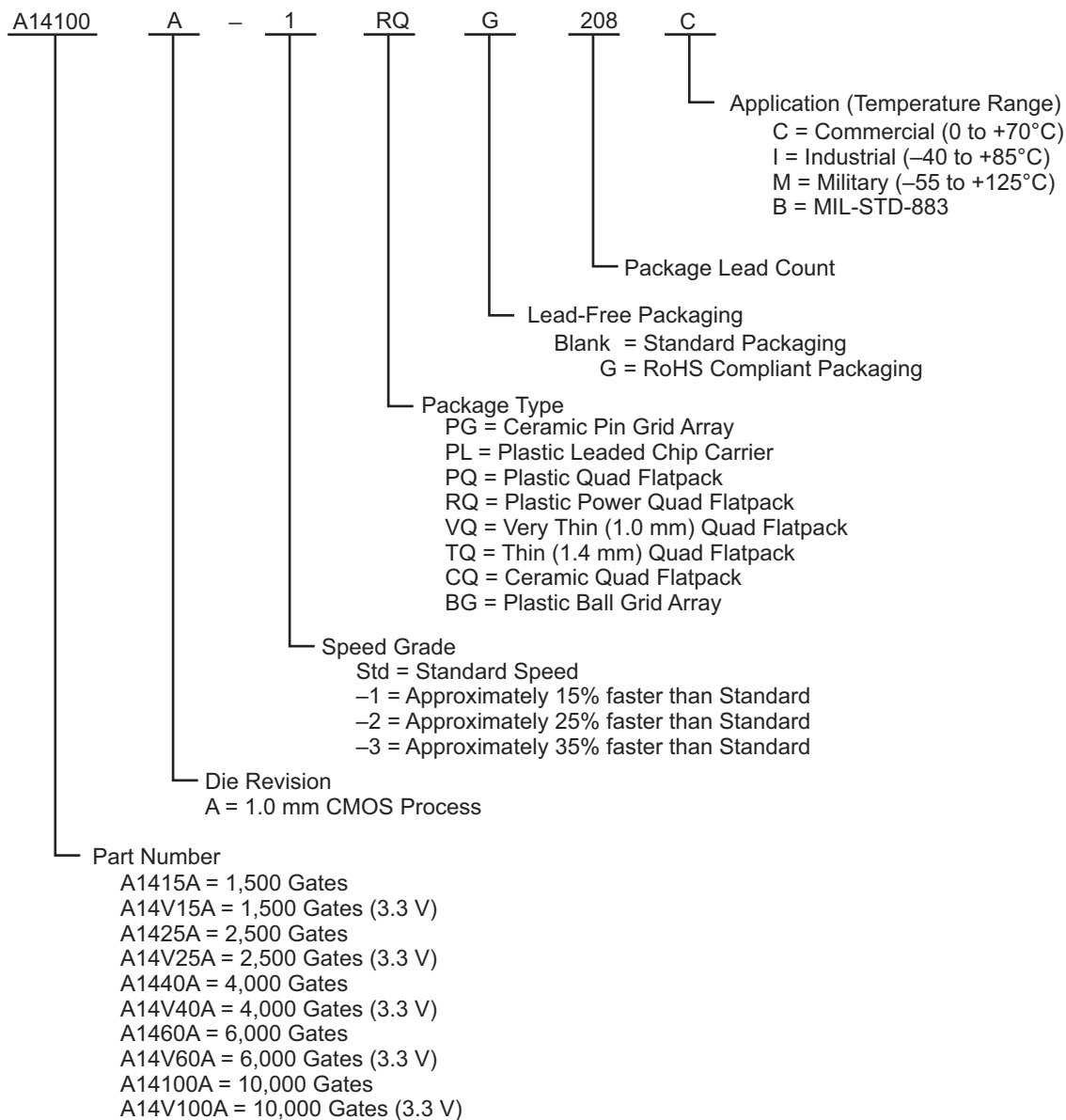
### Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

#### Details

Product Status	Obsolete
Number of LABs/CLBs	1377
Number of Logic Elements/Cells	-
Total RAM Bits	-
Number of I/O	228
Number of Gates	10000
Voltage - Supply	4.5V ~ 5.5V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 70°C (TA)
Package / Case	256-BFCQFP with Tie Bar
Supplier Device Package	256-CQFP (75x75)
Purchase URL	<a href="https://www.e-xfl.com/product-detail/microsemi/a14100a-1cq256c">https://www.e-xfl.com/product-detail/microsemi/a14100a-1cq256c</a>

## Ordering Information



### Notes:

1. The -2 and -3 speed grades have been discontinued.
2. The Ceramic Pin Grid Array packages PG100, PG133, and PG175 have been discontinued in all device densities, speed grades, and temperature grades.
3. The Plastic Ball Grid Array package BG225 has been discontinued in all device densities (specifically for A1460A), all speed grades, and all temperature grades.
4. Military Grade devices are no longer available for the A1440A device.
5. For more information about discontinued devices, refer to the Product Discontinuation Notices (PDNs) listed below, available on the Microsemi SoC Products Group website:  
 PDN March 2001  
 PDN 0104  
 PDN 0203  
 PDN 0604  
 PDN 1004

## Product Plan

Device/Package	Speed Grade <sup>1</sup>				Application <sup>1</sup>			
	Std.	–1	–2	–3	C	I	M	B
<b>A1415A Device</b>								
84-Pin Plastic Leaded Chip Carrier (PLCC)	✓	✓	D	D	✓	✓	✓	–
100-Pin Plastic Quad Flatpack (PQFP)	✓	✓	D	D	✓	✓	✓	–
100-Pin Very Thin Quad Flatpack (VQFP)	✓	✓	D	D	✓	✓	✓	–
100-Pin Ceramic Pin Grid Array (CPGA)	D	D	D	D	D	–	–	–
<b>A14V15A Device</b>								
84-Pin Plastic Leaded Chip Carrier (PLCC)	✓	–	–	–	✓	–	–	–
100-Pin Very Thin Quad Flatpack (VQFP)	✓	–	–	–	✓	–	–	–
<b>A1425A Device</b>								
84-Pin Plastic Leaded Chip Carrier (PLCC)	✓	✓	D	D	✓	✓		
100-Pin Plastic Quad Flatpack (PQFP)	✓	✓	D	D	✓	✓	–	–
100-Pin Very Thin Quad Flatpack (VQFP)	✓	✓	D	D	✓	✓	–	–
132-Pin Ceramic Quad Flatpack (CQFP)	✓	✓	–	–	✓	–	✓	✓
133-Pin Ceramic Pin Grid Array (CPGA)	D	D	D	D	D	–	D	D
160-Pin Plastic Quad Flatpack (PQFP)	✓	✓	D	D	✓	✓	–	–
<b>A14V25A Device</b>								
84-Pin Plastic Leaded Chip Carrier (PLCC)	✓	–	–	–	✓	–	–	–
100-Pin Very Thin Quad Flatpack (VQFP)	✓	–	–	–	✓	–	–	–
160-Pin Plastic Quad Flatpack (PQFP)	✓	–	–	–	✓	–	–	–
<b>A1440A Device</b>								
84-Pin Plastic Leaded Chip Carrier (PLCC)	✓	✓	D	D	✓	✓	–	–
100-Pin Very Thin Quad Flatpack (VQFP)	✓	✓	D	D	✓	✓	–	–
160-Pin Plastic Quad Flatpack (PQFP)	✓	✓	D	D	✓	✓	–	–
175-Pin Ceramic Pin Grid Array (CPGA)	D	D	D	D	D	–	–	–
176-Pin Thin Quad Flatpack (TQFP)	✓	✓	D	D	✓	✓	–	–

**Notes:**

- Applications:**  
C = Commercial  
I = Industrial  
M = Military  
2. Commercial only

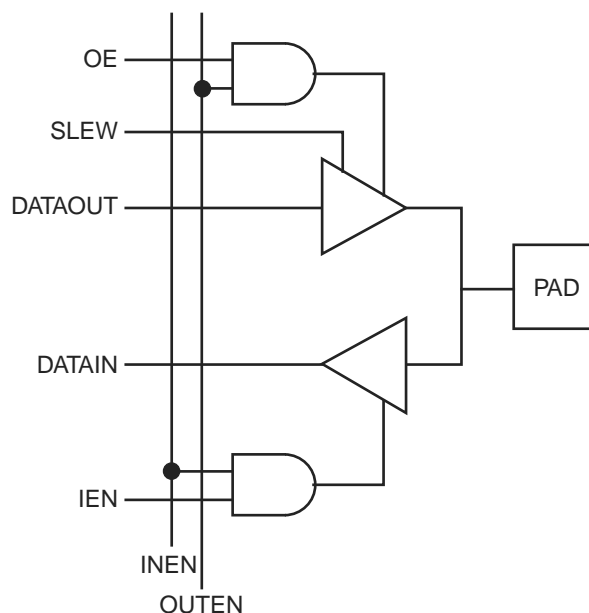
**Availability:**  
✓ = Available  
P = Planned  
– = Not planned  
D = Discontinued

**Speed Grade:**  
–1 = Approx. 15% faster than Std.  
–2 = Approx. 25% faster than Std.  
–3 = Approx. 35% faster than Std.  
(–2 and –3 speed grades have been discontinued.)

The I/O module output Y is used to bring Pad signals into the array or to feed the output register back into the array. This allows the output register to be used in high-speed state machine applications. Side I/O modules have a dedicated output segment for Y extending into the routing channels above and below (similar to logic modules). Top/Bottom I/O modules have no dedicated output segment. Signals coming into the chip from the top or bottom are routed using F-fuses and LVTs (F-fuses and LVTs are explained in detail in the routing section).

## I/O Pad Drivers

All pad drivers are capable of being tristate. Each buffer connects to an associated I/O module with four signals: OE (Output Enable), IE (Input Enable), DataOut, and DataIn. Certain special signals used only during programming and test also connect to the pad drivers: OUTEN (global output enable), INEN (global input enable), and SLEW (individual slew selection). See Figure 2-5.



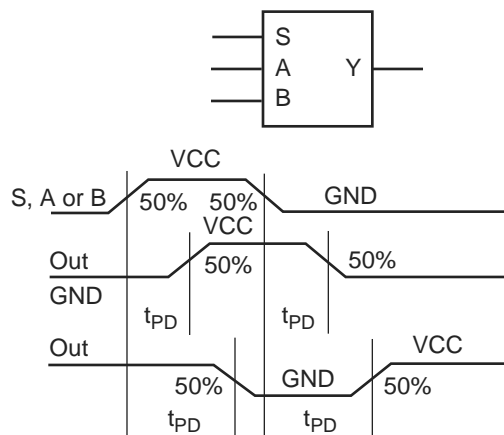
**Figure 2-5 • Function Diagram for I/O Pad Driver**

## Special I/Os

The special I/Os are of two types: temporary and permanent. Temporary special I/Os are used during programming and testing. They function as normal I/Os when the MODE pin is inactive. Permanent special I/Os are user programmed as either normal I/Os or special I/Os. Their function does not change once the device has been programmed. The permanent special I/Os consist of the array clock input buffers (CLKA and CLKB), the hard-wired array clock input buffer (HCLK), the hard-wired I/O clock input buffer (IOCLK), and the hard-wired I/O register preset/clear input buffer (IOPCL). Their function is determined by the I/O macros selected.

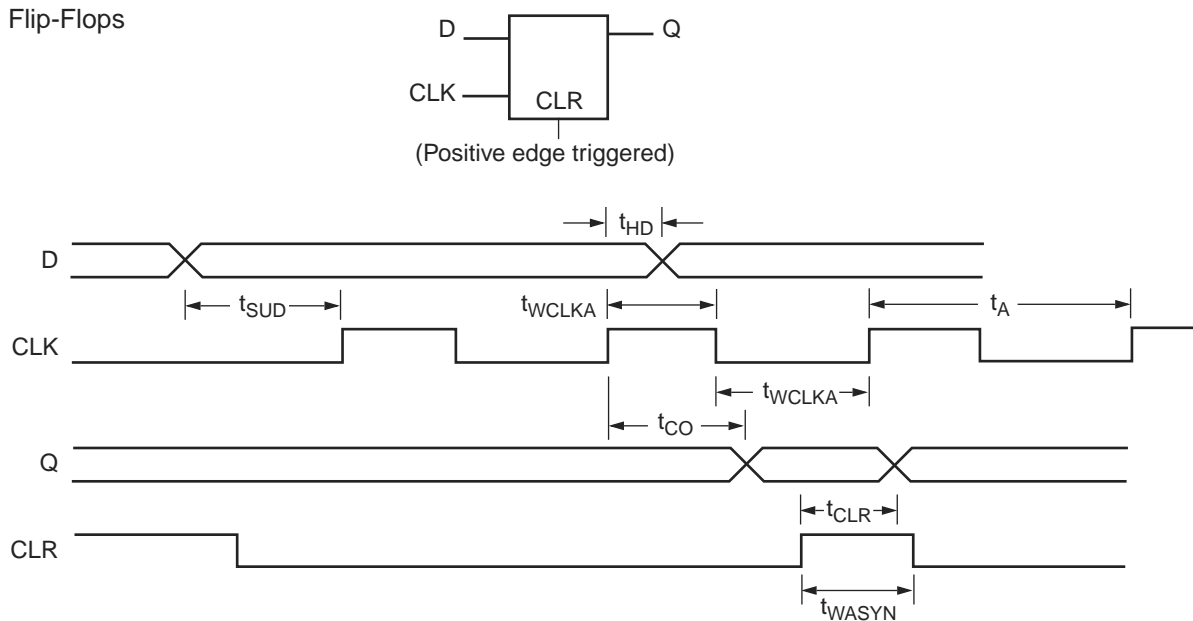
## Clock Networks

The ACT 3 architecture contains four clock networks: two high-performance dedicated clock networks and two general purpose routed networks. The high-performance networks function up to 200 MHz, while the general purpose routed networks function up to 150 MHz.



**Figure 2-14 • Module Delays**

Flip-Flops



**Figure 2-15 • Sequential Module Timing Characteristics**

## A1425A, A14V25A Timing Characteristics (continued)

**Table 2-23 • A1425A, A14V25A Worst-Case Commercial Conditions, VCC = 4.75 V, T<sub>J</sub> = 70°C**

I/O Module Input Propagation Delays		–3 Speed <sup>1</sup>		–2 Speed <sup>1</sup>		–1 Speed		Std. Speed		3.3 V Speed <sup>1</sup>		Units
Parameter/Description		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t <sub>INY</sub>	Input Data Pad to Y		2.8		3.2		3.6		4.2		5.5	ns
t <sub>ICKY</sub>	Input Reg IOCLK Pad to Y		4.7		5.3		6.0		7.0		9.2	ns
t <sub>OCKY</sub>	Output Reg IOCLK Pad to Y		4.7		5.3		6.0		7.0		9.2	ns
t <sub>ICLRY</sub>	Input Asynchronous Clear to Y		4.7		5.3		6.0		7.0		9.2	ns
t <sub>OCLRY</sub>	Output Asynchronous Clear to Y		4.7		5.3		6.0		7.0		9.2	ns
<b>Predicted Input Routing Delays<sup>2</sup></b>												
t <sub>RD1</sub>	FO = 1 Routing Delay		0.9		1.0		1.1		1.3		1.7	ns
t <sub>RD2</sub>	FO = 2 Routing Delay		1.2		1.4		1.6		1.8		2.4	ns
t <sub>RD3</sub>	FO = 3 Routing Delay		1.4		1.6		1.8		2.1		2.8	ns
t <sub>RD4</sub>	FO = 4 Routing Delay		1.7		1.9		2.2		2.5		3.3	ns
t <sub>RD8</sub>	FO = 8 Routing Delay		2.8		3.2		3.6		4.2		5.5	ns
<b>I/O Module Sequential Timing (wrt IOCLK pad)</b>												
t <sub>INH</sub>	Input F-F Data Hold	0.0		0.0		0.0		0.0		0.0		ns
t <sub>INSU</sub>	Input F-F Data Setup	1.8		2.0		2.3		2.7		3.0		ns
t <sub>IDEH</sub>	Input Data Enable Hold	0.0		0.0		0.0		0.0		0.0		ns
t <sub>IDESU</sub>	Input Data Enable Setup	5.8		6.5		7.5		8.6		8.6		ns
t <sub>OUTH</sub>	Output F-F Data hold	0.7		0.8		0.9		1.0		1.0		ns
t <sub>OUTSU</sub>	Output F-F Data Setup	0.7		0.8		0.9		1.0		1.0		ns
t <sub>ODEH</sub>	Output Data Enable Hold	0.3		0.4		0.4		0.5		0.5		ns
f <sub>ODESU</sub>	Output Data Enable Setup	1.3		1.5		1.7		2.0		2.0		ns

Notes: \*

1. The –2 and –3 speed grades have been discontinued. Refer to PDN 0104, PDN 0203, PDN 0604, and PDN 1004 at <http://www.microsemi.com/soc/support/notifications/default.aspx#pdn>.
2. Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual worst-case performance. Post-route timing is based on actual routing delay measurements performed on the device prior to shipment.

## A1440A, A14V40A Timing Characteristics

**Table 2-26 • A1440A, A14V40A Worst-Case Commercial Conditions, VCC = 4.75 V, T<sub>J</sub> = 70°C<sup>1</sup>**

Logic Module Propagation Delays <sup>2</sup>		–3 Speed <sup>3</sup>		–2 Speed <sup>3</sup>		–1 Speed		Std. Speed		3.3 V Speed <sup>1</sup>		Units
Parameter/Description		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t <sub>PD</sub>	Internal Array Module		2.0		2.3		2.6		3.0		3.9	ns
t <sub>CO</sub>	Sequential Clock to Q		2.0		2.3		2.6		3.0		3.9	ns
t <sub>CLR</sub>	Asynchronous Clear to Q		2.0		2.3		2.6		3.0		3.9	ns
<b>Predicted Routing Delays<sup>4</sup></b>												
t <sub>RD1</sub>	FO = 1 Routing Delay		0.9		1.0		1.1		1.3		1.7	ns
t <sub>RD2</sub>	FO = 2 Routing Delay		1.2		1.4		1.6		1.8		2.4	ns
t <sub>RD3</sub>	FO = 3 Routing Delay		1.4		1.6		1.8		2.1		2.8	ns
t <sub>RD4</sub>	FO = 4 Routing Delay		1.7		1.9		2.2		2.5		3.3	ns
t <sub>RD8</sub>	FO = 8 Routing Delay		2.8		3.2		3.6		4.2		5.5	ns
<b>Logic Module Sequential Timing</b>												
t <sub>SUD</sub>	Flip-Flop Data Input Setup	0.5		0.6		0.7		0.8		0.8		ns
t <sub>HD</sub>	Flip-Flop Data Input Hold	0.0		0.0		0.0		0.0		0.0		ns
t <sub>SUD</sub>	Latch Data Input Setup	0.5		0.6		0.7		0.8		0.8		ns
t <sub>HD</sub>	Latch Data Input Hold	0.0		0.0		0.0		0.0		0.0		ns
t <sub>WASYN</sub>	Asynchronous Pulse Width	1.9		2.4		3.2		3.8		4.8		ns
t <sub>WCLKA</sub>	Flip-Flop Clock Pulse Width	1.9		2.4		3.2		3.8		4.8		ns
t <sub>A</sub>	Flip-Flop Clock Input Period	4.0		5.0		6.8		8.0		10.0		ns
f <sub>MAX</sub>	Flip-Flop Clock Frequency		250		200		150		125		100	MHz

**Notes:**

1. VCC = 3.0 V for 3.3 V specifications.
2. For dual-module macros, use t<sub>PD</sub> + t<sub>RD1</sub> + t<sub>PDn</sub> + t<sub>CO</sub> + t<sub>RD1</sub> + t<sub>PDn</sub> or t<sub>PD1</sub> + t<sub>RD1</sub> + t<sub>SUD</sub>, whichever is appropriate.
3. The –2 and –3 speed grades have been discontinued. Refer to PDN 0104, PDN 0203, PDN 0604, and PDN 1004 at <http://www.microsemi.com/soc/support/notifications/default.aspx#pdn>.
4. Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual worst-case performance. Post-route timing is based on actual routing delay measurements performed on the device prior to shipment.

## A1440A, A14V40A Timing Characteristics (continued)

**Table 2-29 • A1440A, A14V40A Worst-Case Commercial Conditions, VCC = 4.75 V, T<sub>J</sub> = 70°C**

Dedicated (hardwired) I/O Clock Network		–3 Speed <sup>1</sup>		–2 Speed <sup>1</sup>		–1 Speed		Std. Speed		3.3 V Speed <sup>1</sup>		Units
Parameter/Description		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t <sub>IOCKH</sub>	Input Low to High (pad to I/O module input)		2.0		2.3		2.6		3.0		3.5	ns
t <sub>IOPWH</sub>	Minimum Pulse Width High	1.9		2.4		3.3		3.8		4.8		ns
t <sub>IPOWL</sub>	Minimum Pulse Width Low	1.9		2.4		3.3		3.8		4.8		ns
t <sub>IOSAPW</sub>	Minimum Asynchronous Pulse Width	1.9		2.4		3.3		3.8		4.8		ns
t <sub>IOCKSW</sub>	Maximum Skew		0.4		0.4		0.4		0.4		0.4	ns
t <sub>IOP</sub>	Minimum Period	4.0		5.0		6.8		8.0		10.0		ns
f <sub>IOMAX</sub>	Maximum Frequency		250		200		150		125		100	MHz
<b>Dedicated (hardwired) Array Clock</b>												
t <sub>HCKH</sub>	Input Low to High (pad to S-module input)		3.0		3.4		3.9		4.5		5.5	ns
t <sub>HCKL</sub>	Input High to Low (pad to S-module input)		3.0		3.4		3.9		4.5		5.5	ns
t <sub>HPWH</sub>	Minimum Pulse Width High	1.9		2.4		3.3		3.8		4.8		ns
t <sub>HPWL</sub>	Minimum Pulse Width Low	1.9		2.4		3.3		3.8		4.8		ns
t <sub>HCKSW</sub>	Delta High to Low, Low Slew		0.3		0.3		0.3		0.3		0.3	ns
t <sub>HP</sub>	Minimum Period	4.0		5.0		6.8		8.0		10.0		ns
f <sub>HMAX</sub>	Maximum Frequency		250		200		150		125		100	MHz
<b>Routed Array Clock Networks</b>												
t <sub>RCKH</sub>	Input Low to High (FO = 64)		3.7		4.1		4.7		5.5		9.0	ns
t <sub>RCKL</sub>	Input High to Low (FO = 64)		4.0		4.5		5.1		6.0		9.0	ns
t <sub>RPWH</sub>	Min. Pulse Width High (FO = 64)	3.3		3.8		4.2		4.9		6.5		ns
t <sub>RPWL</sub>	Min. Pulse Width Low (FO = 64)	3.3		3.8		4.2		4.9		6.5		ns
t <sub>RCKSW</sub>	Maximum Skew (FO = 128)		0.7		0.8		0.9		1.0		1.0	ns
t <sub>RP</sub>	Minimum Period (FO = 64)	6.8		8.0		8.7		10.0		13.4		ns
f <sub>RMAX</sub>	Maximum Frequency (FO = 64)		150		125		115		100		75	MHz
<b>Clock-to-Clock Skews</b>												
t <sub>IOHCKSW</sub>	I/O Clock to H-Clock Skew	0.0	1.7	0.0	1.8	0.0	2.0	0.0	2.2	0.0	3.0	ns
t <sub>IORCKSW</sub>	I/O Clock to R-Clock Skew (FO = 64) (FO = 144)	0.0	1.0	0.0	1.0	0.0	1.0	0.0	1.0	0.0	3.0	ns
		0.0	3.0	0.0	3.0	0.0	3.0	0.0	3.0	0.0	3.0	
t <sub>HRCKSW</sub>	H-Clock to R-Clock Skew (FO = 64) (FO = 144)	0.0	1.0	0.0	1.0	0.0	1.0	0.0	1.0	0.0	1.0	ns
		0.0	3.0	0.0	3.0	0.0	3.0	0.0	3.0	0.0	3.0	

**Notes:**

1. The –2 and –3 speed grades have been discontinued. Refer to PDN 0104, PDN 0203, PDN 0604, and PDN 1004 at <http://www.microsemi.com/soc/support/notifications/default.aspx#pdn>.
2. Delays based on 35 pF loading.



## A14100A, A14V100A Timing Characteristics (continued)

**Table 2-35 • A14100A, A14V100A Worst-Case Commercial Conditions, VCC = 4.75 V, T<sub>J</sub> = 70°C**

I/O Module Input Propagation Delays		–3 Speed <sup>1</sup>		–2 Speed <sup>1</sup>		–1 Speed		Std. Speed		3.3 V Speed <sup>1</sup>		Units
Parameter/Description		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t <sub>INY</sub>	Input Data Pad to Y		2.8		3.2		3.6		4.2		5.5	ns
t <sub>ICKY</sub>	Input Reg IOCLK Pad to Y		4.7		5.3		6.0		7.0		9.2	ns
t <sub>OCKY</sub>	Output Reg IOCLK Pad to Y		4.7		5.3		6.0		7.0		9.2	ns
t <sub>ICLRY</sub>	Input Asynchronous Clear to Y		4.7		5.3		6.0		7.0		9.2	ns
t <sub>OCLRY</sub>	Output Asynchronous Clear to Y		4.7		5.3		6.0		7.0		9.2	ns
<b>Predicted Input Routing Delays<sup>2</sup></b>												
t <sub>RD1</sub>	FO = 1 Routing Delay		0.9		1.0		1.1		1.3		1.7	ns
t <sub>RD2</sub>	FO = 2 Routing Delay		1.2		1.4		1.6		1.8		2.4	ns
t <sub>RD3</sub>	FO = 3 Routing Delay		1.4		1.6		1.8		2.1		2.8	ns
t <sub>RD4</sub>	FO = 4 Routing Delay		1.7		1.9		2.2		2.5		3.3	ns
t <sub>RD8</sub>	FO = 8 Routing Delay		2.8		3.2		3.6		4.2		5.5	ns
<b>I/O Module Sequential Timing (wrt IOCLK pad)</b>												
t <sub>INH</sub>	Input F-F Data Hold	0.0		0.0		0.0		0.0		0.0		ns
t <sub>INSU</sub>	Input F-F Data Setup	1.2		1.4		1.5		1.8		1.8		ns
t <sub>IDEH</sub>	Input Data Enable Hold	0.0		0.0		0.0		0.0		0.0		ns
t <sub>IDESU</sub>	Input Data Enable Setup	5.8		6.5		7.5		8.6		8.6		ns
t <sub>OUTH</sub>	Output F-F Data hold	0.7		0.8		1.0		1.0		1.0		ns
t <sub>OUTSU</sub>	Output F-F Data Setup	0.7		0.8		1.0		1.0		1.0		ns
t <sub>ODEH</sub>	Output Data Enable Hold	0.3		0.4		0.5		0.5		0.5		ns
f <sub>ODESU</sub>	Output Data Enable Setup	1.3		1.5		2.0		2.0		2.0		ns

Notes: \*

1. The –2 and –3 speed grades have been discontinued. Refer to PDN 0104, PDN 0203, PDN 0604, and PDN 1004 at <http://www.microsemi.com/soc/support/notifications/default.aspx#pdn>.
2. Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual worst-case performance. Post-route timing is based on actual routing delay measurements performed on the device prior to shipment.

## A14100A, A14V100A Timing Characteristics (continued)

**Table 2-37 • A14100A, A14V100A Worst-Case Commercial Conditions, VCC = 4.75 V, T<sub>J</sub> = 70°C**

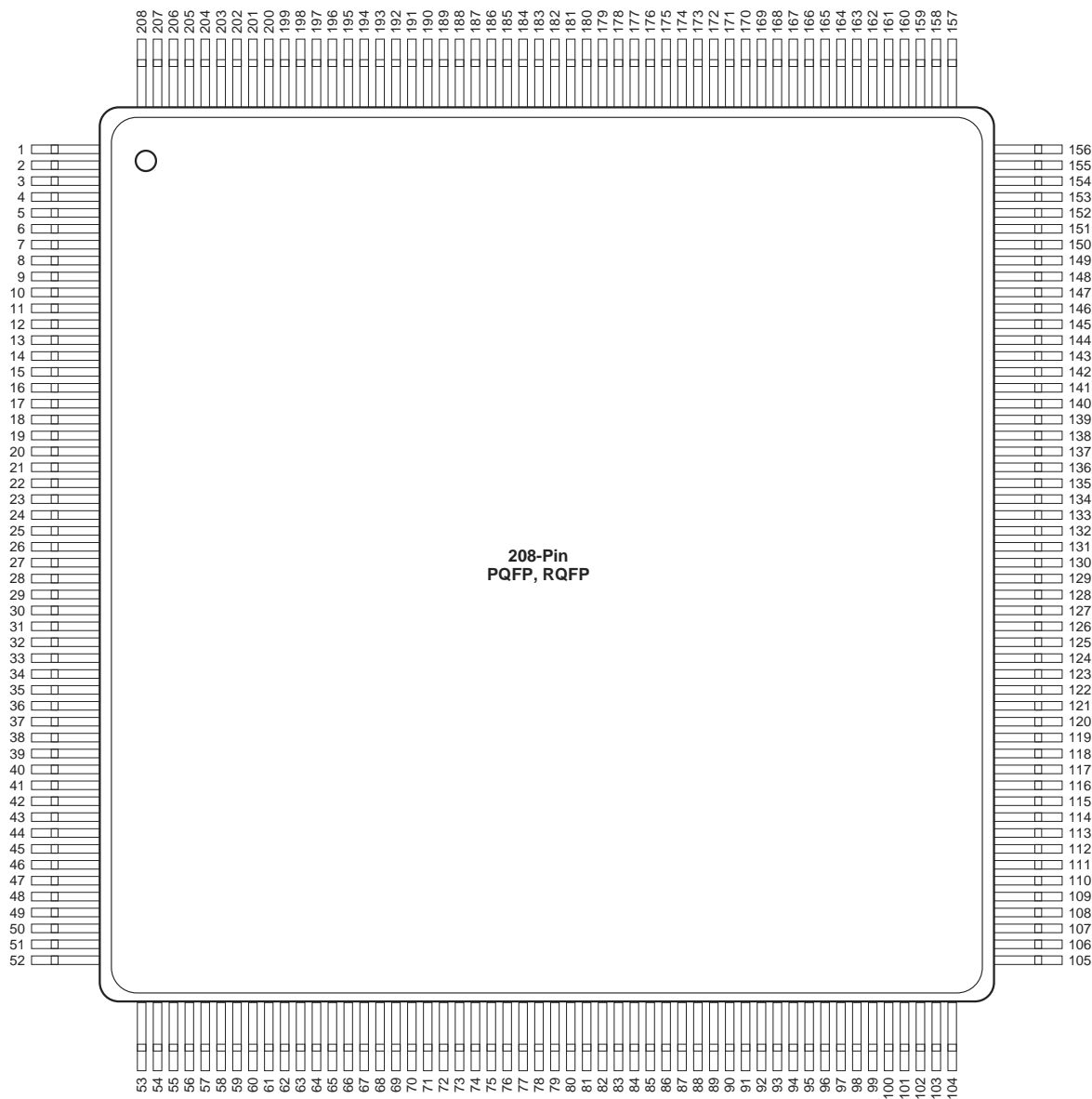
Dedicated (hardwired) I/O Clock Network		–3 Speed <sup>1</sup>		–2 Speed <sup>1</sup>		–1 Speed		Std. Speed		3.3 V Speed <sup>1</sup>		Units
Parameter/Description		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t <sub>IOCKH</sub>	Input Low to High (pad to I/O module input)		2.3		2.6		3.0		3.5		4.5	ns
t <sub>IOPWH</sub>	Minimum Pulse Width High	2.4		3.3		3.8		4.8		6.5		ns
t <sub>IPOWL</sub>	Minimum Pulse Width Low	2.4		3.3		3.8		4.8		6.5		ns
t <sub>IOSAPW</sub>	Minimum Asynchronous Pulse Width	2.4		3.3		3.8		4.8		6.5		ns
t <sub>IOCKSW</sub>	Maximum Skew		0.6		0.6		0.7		0.8		0.6	ns
t <sub>IOP</sub>	Minimum Period	5.0		6.8		8.0		10.0		13.4		ns
f <sub>IOMAX</sub>	Maximum Frequency		200		150		125		100		75	MHz
<b>Dedicated (hardwired) Array Clock</b>												
t <sub>HCKH</sub>	Input Low to High (pad to S-module input)		3.7		4.1		4.7		5.5		7.0	ns
t <sub>HCKL</sub>	Input High to Low (pad to S-module input)		3.7		4.1		4.7		5.5		7.0	ns
t <sub>HPWH</sub>	Minimum Pulse Width High	2.4		3.3		3.8		4.8		6.5		ns
t <sub>HPWL</sub>	Minimum Pulse Width Low	2.4		3.3		3.8		4.8		6.5		ns
t <sub>HCKSW</sub>	Delta High to Low, Low Slew		0.6		0.6		0.7		0.8		0.6	ns
t <sub>HP</sub>	Minimum Period	5.0		6.8		8.0		10.0		13.4		ns
f <sub>HMAX</sub>	Maximum Frequency		200		150		125		100		75	MHz
<b>Routed Array Clock Networks</b>												
t <sub>RCKH</sub>	Input Low to High (FO = 64)		6.0		6.8		7.7		9.0		11.8	ns
t <sub>RCKL</sub>	Input High to Low (FO = 64)		6.0		6.8		7.7		9.0		11.8	ns
t <sub>RPWH</sub>	Min. Pulse Width High (FO = 64)	4.1		4.5		5.4		6.1		8.2		ns
t <sub>RPWL</sub>	Min. Pulse Width Low (FO = 64)	4.1		4.5		5.4		6.1		8.2		ns
t <sub>RCKSW</sub>	Maximum Skew (FO = 128)		1.2		1.4		1.6		1.8		1.8	ns
t <sub>RP</sub>	Minimum Period (FO = 64)	8.3		9.3		11.1		12.5		16.7		ns
f <sub>RMAX</sub>	Maximum Frequency (FO = 64)		120		105		90		80		60	MHz
<b>Clock-to-Clock Skews</b>												
t <sub>IOHCKSW</sub>	I/O Clock to H-Clock Skew	0.0	2.6	0.0	2.7	0.0	2.9	0.0	3.0	0.0	3.0	ns
t <sub>IORCKSW</sub>	I/O Clock to R-Clock Skew (FO = 64) (FO = 350)	0.0	1.7	0.0	1.7	0.0	1.7	0.0	1.7	0.0	5.0	ns
		0.0	5.0	0.0	5.0	0.0	5.0	0.0	5.0	0.0	5.0	
t <sub>HRCKSW</sub>	H-Clock to R-Clock Skew (FO = 64) (FO = 350)	0.0	1.3	0.0	1.0	0.0	1.0	0.0	1.0	0.0	1.0	ns
		0.0	3.0	0.0	3.0	0.0	3.0	0.0	3.0	0.0	3.0	

Notes: \*

1. The –2 and –3 speed grades have been discontinued. Refer to PDN 0104, PDN 0203, PDN 0604, and PDN 1004 at <http://www.microsemi.com/soc/support/notifications/default.aspx#pdn>.
2. Delays based on 35 pF loading.

PQ160			
Pin Number	A1425, A14V25 Function	A1440, A14V40 Function	A1460, A14V60 Function
1	GND	GND	GND
2	SDI, I/O	SDI, I/O	SDI, I/O
5	NC	I/O	I/O
9	MODE	MODE	MODE
10	VCC	VCC	VCC
14	NC	I/O	I/O
15	GND	GND	GND
18	VCC	VCC	VCC
19	GND	GND	GND
20	NC	I/O	I/O
24	NC	I/O	I/O
27	NC	I/O	I/O
28	VCC	VCC	VCC
29	VCC	VCC	VCC
40	GND	GND	GND
41	NC	I/O	I/O
43	NC	I/O	I/O
45	NC	I/O	I/O
46	VCC	VCC	VCC
47	NC	I/O	I/O
49	NC	I/O	I/O
51	NC	I/O	I/O
53	NC	I/O	I/O
58	PRB, I/O	PRB, I/O	PRB, I/O
59	GND	GND	GND
60	VCC	VCC	VCC
62	HCLK, I/O	HCLK, I/O	HCLK, I/O
63	GND	GND	GND
74	NC	I/O	I/O
75	VCC	VCC	VCC
76	NC	I/O	I/O
77	NC	I/O	I/O
78	NC	I/O	I/O
79	SDO	SDO	SDO
80	IOPCL, I/O	IOPCL, I/O	IOPCL, I/O
81	GND	GND	GND
90	VCC	VCC	VCC
91	VCC	VCC	VCC

## PQ208, RQ208



*Note: This is the top view of the package*

### Note

For Package Manufacturing and Environmental information, visit the Resource Center at <http://www.microsemi.com/soc/products/solutions/package/docs.aspx>

CQ132	
Pin Number	A1425 Function
1	NC
2	GND
3	SDI, I/O
9	MODE
10	GND
11	VCC
22	VCC
26	GND
27	VCC
34	NC
36	GND
42	GND
43	VCC
48	PRB, I/O
50	HCLK, I/O
58	GND
59	VCC
63	SDO
64	IOPCL, I/O
65	GND
66	NC

CQ132	
Pin Number	A1425 Function
67	NC
74	GND
75	VCC
78	VCC
89	VCC
90	GND
91	VCC
92	GND
98	IOCLK, I/O
99	NC
100	NC
101	GND
106	GND
107	VCC
116	CLKA, I/O
117	CLKB, I/O
118	PRA, I/O
122	GND
123	VCC
131	DCLK, I/O
132	NC

*Notes:*

1. All unlisted pin numbers are user I/Os.
2. NC denotes no connection.
3. MODE should be terminated to GND through a 10K resistor to enable Actionprobe usage; otherwise it can be terminated directly to GND.

CQ256	
Pin Number	A14100 Function
1	GND
2	SDI, I/O
11	MODE
28	VCC
29	GND
30	VCC
31	GND
46	VCC
59	GND
90	PRB, I/O
91	GND
92	VCC
93	GND
94	VCC
96	HCLK, I/O
110	GND
126	SDO
127	IOPCL, I/O
128	GND

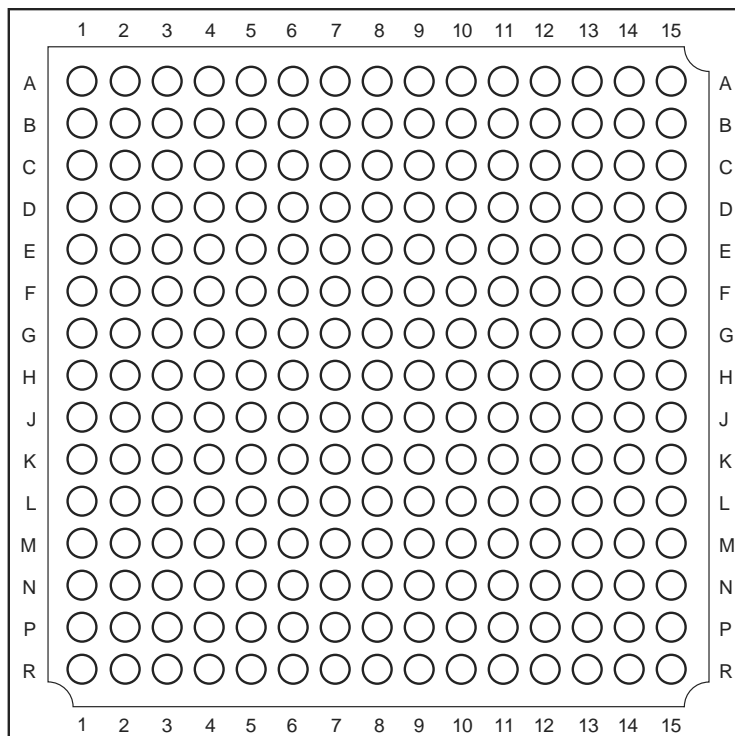
CQ256	
Pin Number	A14100 Function
141	VCC
158	GND
159	VCC
160	GND
161	VCC
174	VCC
175	GND
176	GND
188	IOCLK, I/O
189	GND
219	CLKA, I/O
220	CLKB, I/O
221	VCC
222	GND
223	VCC
224	GND
225	PRA, I/O
240	GND
256	DCLK, I/O

**Notes:**

1. All unlisted pin numbers are user I/Os.
2. NC denotes no connection.
3. MODE should be terminated to GND through a 10K resistor to enable Actionprobe usage; otherwise it can be terminated directly to GND.

## BG225

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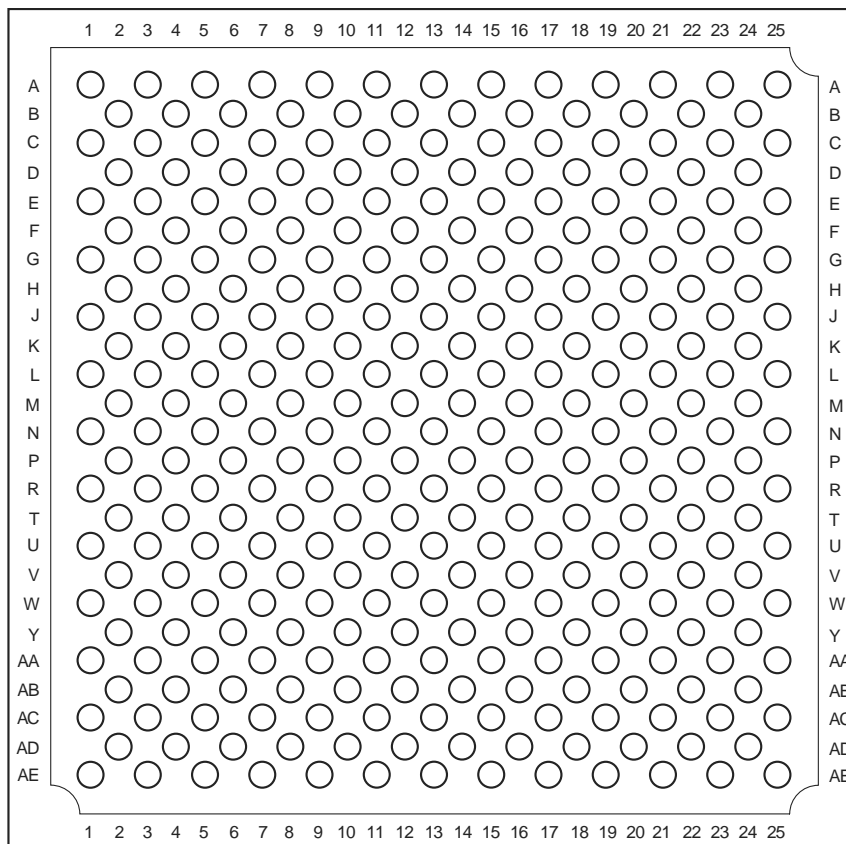
*Note:* This is the top view.

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### **Note**

For Package Manufacturing and Environmental information, visit the Resource Center at <http://www.microsemi.com/soc/products/solutions/package/docs.aspx>

## BG313



*Note: This is the top view.*

### **Note**

For Package Manufacturing and Environmental information, visit the Resource Center at <http://www.microsemi.com/soc/products/solutions/package/docs.aspx>



BG313	
A14100, A14V100 Function	Location
CLKA or I/O	J13
CLKB or I/O	G13
DCLK or I/O	B2
GND	A1, A25, AD2, AE25, J21, L13, M12, M14, N11, N13, N15, P12, P14, R13
HCLK or I/O	T14
IOCLK or I/O	B24
IOPCL or I/O	AD24
MODE	G3
NC	A3, A13, A23, AA5, AA9, AA23, AB2, AB4, AB20, AC13, AC25, AD22, AE1, AE21, B14, C5, C25, D4, D24, E3, E21, F6, F10, F16, G1, G25, H18, H24, J1, J7, J25, K12, L15, L17, M6, N1, N5, N7, N21, N23, P20, R11, T6, T8, U9, U13, U21, V16, W7, Y20, Y24
PRA or I/O	H12
PRB or I/O	AD12
SDI or I/O	C1
SDO	AE23
VCC	AB18, AD6, AE13, C13, C19, E13, G9, H22, K8, K20, M16, N3, N9, N25, U5, W13, V2, V22, V24

*Notes:*

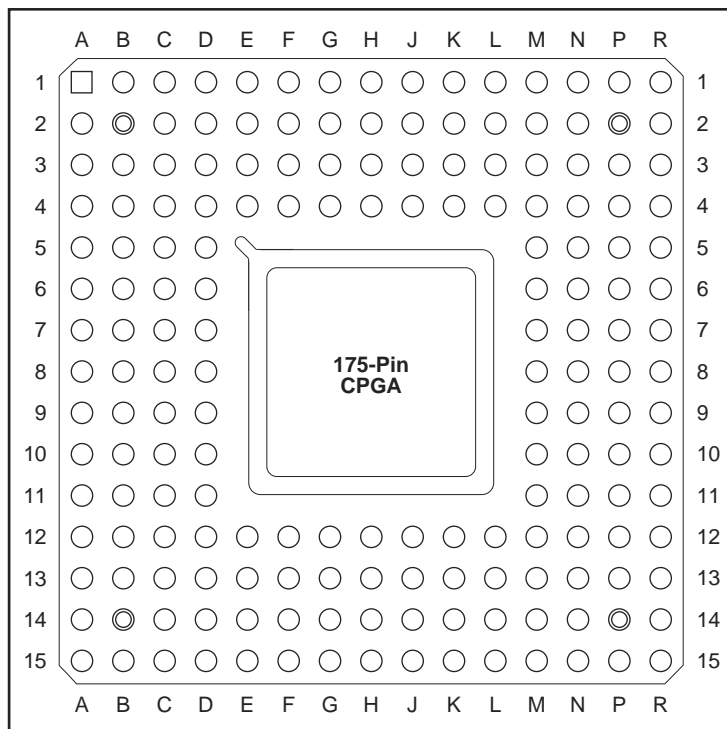
1. All unlisted pin numbers are user I/Os.
2. NC denotes no connection.
3. MODE should be terminated to GND through a 10K resistor to enable Actionprobe usage; otherwise it can be terminated directly to GND.

PG133	
A1425 Function	Location
CLKA or I/O	D7
CLKB or I/O	B6
DCLK or I/O	D4
GND	A2, C3, C7, C11, C12, F10, G3, G11, L3, L7, L11, M3, N12
HCLK or I/O	K7
IOCLK or I/O	C10
IOPCL or I/O	L10
MODE	E3
NC	A1, A7, A13, G1, G13, N1, N7, N13
PRA or I/O	A6
PRB or I/O	L6
SDI or I/O	C2
SDO	M11
VCC	B2, B7, B12, E11, G2, G12, J2, J12, M2, M7, M12

*Notes:*

1. All unlisted pin numbers are user I/Os.
2. NC denotes no connection.
3. MODE should be terminated to GND through a 10K resistor to enable Actionprobe usage; otherwise it can be terminated directly to GND.
4. The PG133 package has been discontinued.

## PG175



*Note:* This is the top view.

### Note

For Package Manufacturing and Environmental information, visit the Resource Center at <http://www.microsemi.com/soc/products/solutions/package/docs.aspx>





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