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Understanding [Embedded - FPGAs \(Field Programmable Gate Array\)](#)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

| | |
|--------------------------------|---|
| Product Status | Obsolete |
| Number of LABs/CLBs | 1377 |
| Number of Logic Elements/Cells | - |
| Total RAM Bits | - |
| Number of I/O | 228 |
| Number of Gates | 10000 |
| Voltage - Supply | 4.5V ~ 5.5V |
| Mounting Type | Through Hole |
| Operating Temperature | 0°C ~ 70°C (TA) |
| Package / Case | 257-BCPGA |
| Supplier Device Package | 257-CPGA (50x50) |
| Purchase URL | https://www.e-xfl.com/product-detail/microsemi/a14100a-1pg257c |

| Device/Package | Speed Grade ¹ | | | | Application ¹ | | | |
|---|--------------------------|----|----|----|--------------------------|---|---|---|
| | Std. | –1 | –2 | –3 | C | I | M | B |
| A14V40A Device | | | | | | | | |
| 84-Pin Plastic Leaded Chip Carrier (PLCC) | ✓ | – | – | – | ✓ | – | – | – |
| 100-Pin Very Thin Quad Flatpack (VQFP) | ✓ | – | – | – | ✓ | – | – | – |
| 160-Pin Plastic Quad Flatpack (PQFP) | ✓ | – | – | – | ✓ | – | – | – |
| 176-Pin Thin Quad Flatpack (TQFP) | ✓ | – | – | – | ✓ | – | – | – |
| A1460A Device | | | | | | | | |
| 160-Pin Plastic Quad Flatpack (PQFP) | ✓ | ✓ | D | D | ✓ | ✓ | – | – |
| 176-Pin Thin Quad Flatpack (TQFP) | ✓ | ✓ | D | D | ✓ | ✓ | – | – |
| 196-Pin Ceramic Quad Flatpack (CQFP) | ✓ | ✓ | – | – | ✓ | – | ✓ | ✓ |
| 207-Pin Ceramic Pin Grid Array (CPGA) | ✓ | ✓ | D | D | ✓ | – | ✓ | ✓ |
| 208-Pin Plastic Quad Flatpack (PQFP) | ✓ | ✓ | D | D | ✓ | ✓ | – | – |
| 225-Pin Plastic Ball Grid Array (BGA) | D | D | D | D | D | – | – | – |
| A14V60A Device | | | | | | | | |
| 160-Pin Plastic Quad Flatpack (PQFP) | ✓ | – | – | – | ✓ | – | – | – |
| 176-Pin Thin Quad Flatpack (TQFP) | ✓ | – | – | – | ✓ | – | – | – |
| 208-Pin Plastic Quad Flatpack (PQFP) | ✓ | – | – | – | ✓ | – | – | – |
| A14100A Device | | | | | | | | |
| 208-Pin Power Quad Flatpack (RQFP) | ✓ | ✓ | D | D | ✓ | ✓ | – | – |
| 257-Pin Ceramic Pin Grid Array (CPGA) | ✓ | ✓ | D | D | ✓ | – | ✓ | ✓ |
| 313-Pin Plastic Ball Grid Array (BGA) | ✓ | ✓ | D | D | ✓ | – | – | – |
| 256-Pin Ceramic Quad Flatpack (CQFP) | ✓ | ✓ | – | – | ✓ | – | ✓ | ✓ |
| A14V100A Device | | | | | | | | |
| 208-Pin Power Quad Flatpack (RQFP) | ✓ | – | – | – | ✓ | – | – | – |
| 313-Pin Plastic Ball Grid Array (BGA) | ✓ | – | – | – | ✓ | – | – | – |

Notes:

- Applications:**
C = Commercial
I = Industrial
M = Military
2. Commercial only

Availability:
✓ = Available
P = Planned
– = Not planned
D = Discontinued

Speed Grade:
–1 = Approx. 15% faster than Std.
–2 = Approx. 25% faster than Std.
–3 = Approx. 35% faster than Std.
(–2 and –3 speed grades have been discontinued.)

1 – ACT 3 Family Overview

General Description

Microsemi's ACT 3 Accelerator Series of FPGAs offers the industry's fastest high-capacity programmable logic device. ACT 3 FPGAs offer a high performance, PCI compliant programmable solution capable of 186 MHz on-chip performance and 9.0 nanosecond clock-to-output (–1 speed grade), with capacities spanning from 1,500 to 10,000 gate array equivalent gates.

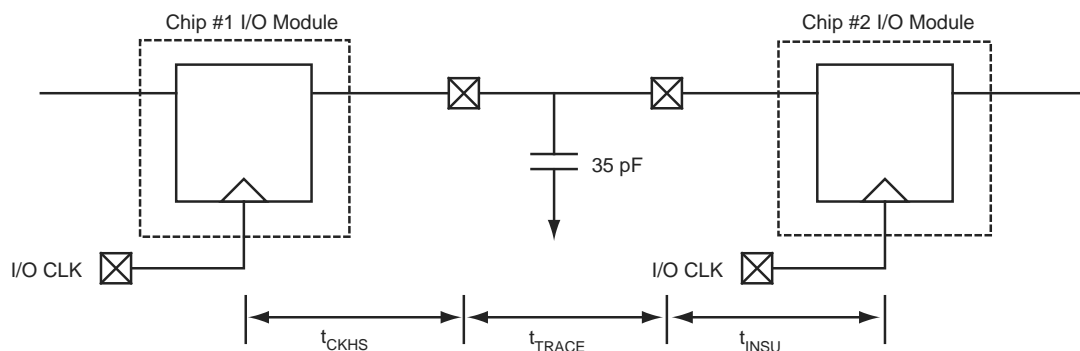
The ACT 3 family builds on the proven two-module architecture consisting of combinatorial and sequential logic modules used in Microsemi's 3200DX and 1200XL families. In addition, the ACT 3 I/O modules contain registers which deliver 9.0 nanosecond clock-to-out times (–1 speed grade). The devices contain four clock distribution networks, including dedicated array and I/O clocks, supporting very fast synchronous and asynchronous designs. In addition, routed clocks can be used to drive high fanout signals such as flip-flop resets and output.

The ACT 3 family is supported by Microsemi's Designer Series Development System which offers automatic placement and routing (with automatic or fixed pin assignments), static timing analysis, user programming, and debug and diagnostic probe capabilities.

| | |
|--------------------------------------|---------|
| Accumulators (16-Bit) | 47 MHz |
| Loadable Counters (16-Bit) | 82 MHz |
| Prescaled Loadable Counters (16-Bit) | 186 MHz |
| Shift Registers | 186 MHz |

Figure 1-1 • Predictable Performance (worst-case commercial, –1 speed grade)

System Performance Model



Dedicated Clocks

Dedicated clock networks support high performance by providing sub-nanosecond skew and guaranteed performance. Dedicated clock networks contain no programming elements in the path from the I/O Pad Driver to the input of S-modules or I/O modules. There are two dedicated clock networks: one for the array registers (HCLK), and one for the I/O registers (IOCLK). The clock networks are accessed by special I/Os.

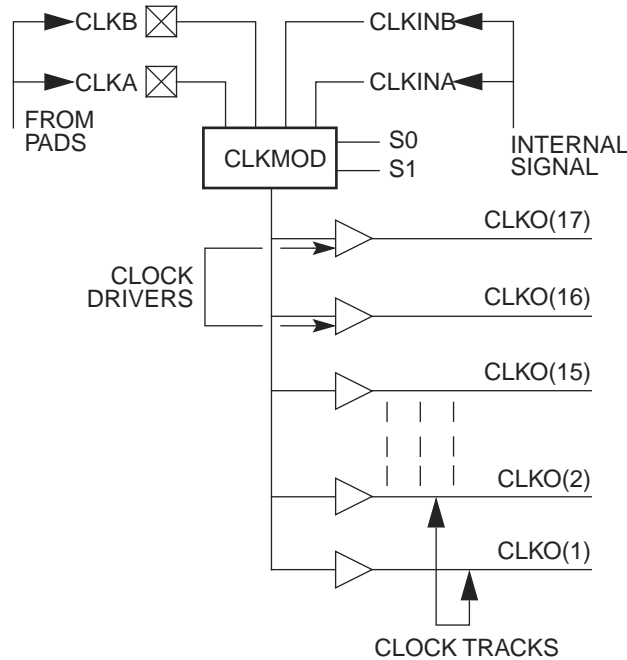


Figure 2-6 • Clock Networks

The routed clock networks are referred to as CLK0 and CLK1. Each network is connected to a clock module (CLKMOD) that selects the source of the clock signal and may be driven as follows (Figure 2-6):

- Externally from the CLKA pad
- Externally from the CLKB pad
- Internally from the CLKINA input
- Internally from the CLKINB input

The clock modules are located in the top row of I/O modules. Clock drivers and a dedicated horizontal clock track are located in each horizontal routing channel. The function of the clock module is determined by the selection of clock macros from the macro library. The macro CLKBUF is used to connect one of the two external clock pins to a clock network, and the macro CLKINT is used to connect an internally generated clock signal to a clock network. Since both clock networks are identical, the user does not care whether CLK0 or CLK1 is being used. Routed clocks can also be used to drive high fanout nets like resets, output enables, or data enables. This saves logic modules and results in performance increases in some cases.

Routing Structure

The ACT 3 architecture uses vertical and horizontal routing tracks to connect the various logic and I/O modules. These routing tracks are metal interconnects that may either be of continuous length or broken into segments. Segments can be joined together at the ends using antifuses to increase their lengths up to the full length of the track.

Power Dissipation

$$P = [ICC_{\text{standby}} + I_{\text{active}}] * VCC * IOL * VOL * N + IOH * (VCC - VOH) * M$$

EQ 3

where:

ICC standby is the current flowing when no inputs or outputs are changing

Iactive is the current flowing due to CMOS switching.

IOL and IOH are TTL sink/source current.

VOL and VOH are TTL level output voltages.

N is the number of outputs driving TTL loads to VOL.

M equals the number of outputs driving TTL loads to VOH.

An accurate determination of N and M is problematical because their values depend on the design and on the system I/O. The power can be divided into two components: static and active.

Static Power Component

Microsemi FPGAs have small static power components that result in lower power dissipation than PALs or PLDs. By integrating multiple PALs/PLDs into one FPGA, an even greater reduction in board-level power dissipation can be achieved.

The power due to standby current is typically a small component of the overall power. Standby power is calculated in Table 2-9 for commercial, worst case conditions.

Table 2-9 • Standby Power Calculation

| ICC | VCC | Power |
|------|--------|---------|
| 2 mA | 5.25 V | 10.5 mW |

The static power dissipated by TTL loads depends on the number of outputs driving high or low and the DC load current. Again, this value is typically small. For instance, a 32-bit bus sinking 4 mA at 0.33 V will generate 42 mW with all outputs driving low, and 140 mW with all outputs driving high. The actual dissipation will average somewhere between as I/Os switch states with time.

Active Power Component

Power dissipation in CMOS devices is usually dominated by the active (dynamic) power dissipation. This component is frequency dependent, a function of the logic and the external I/O. Active power dissipation results from charging internal chip capacitances of the interconnect, unprogrammed antifuses, module inputs, and module outputs, plus external capacitance due to PC board traces and load device inputs.

An additional component of the active power dissipation is the totem-pole current in CMOS transistor pairs. The net effect can be associated with an equivalent capacitance that can be combined with frequency and voltage to represent active power dissipation.

Equivalent Capacitance

The power dissipated by a CMOS circuit can be expressed by EQ 4.

$$\text{Power } (\mu\text{W}) = C_{\text{EQ}} * VCC^2 * F$$

EQ 4

Where:

C_{EQ} is the equivalent capacitance expressed in pF.

VCC is the power supply in volts.

F is the switching frequency in MHz.

A1415A, A14V15A Timing Characteristics

Table 2-18 • A1415A, A14V15A Worst-Case Commercial Conditions, VCC = 4.75 V, T_J = 70°C¹

| Logic Module Propagation Delays ² | | –3 Speed ³ | | –2 Speed ³ | | –1 Speed | | Std. Speed | | 3.3 V Speed ¹ | | Units |
|--|------------------------------|-----------------------|------|-----------------------|------|----------|------|------------|------|--------------------------|------|-------|
| Parameter/Description | | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | |
| t _{PD} | Internal Array Module | | 2.0 | | 2.3 | | 2.6 | | 3.0 | | 3.9 | ns |
| t _{CO} | Sequential Clock to Q | | 2.0 | | 2.3 | | 2.6 | | 3.0 | | 3.9 | ns |
| t _{CLR} | Asynchronous Clear to Q | | 2.0 | | 2.3 | | 2.6 | | 3.0 | | 3.9 | ns |
| Predicted Routing Delays⁴ | | | | | | | | | | | | |
| t _{RD1} | FO = 1 Routing Delay | | 0.9 | | 1.0 | | 1.1 | | 1.3 | | 1.7 | ns |
| t _{RD2} | FO = 2 Routing Delay | | 1.2 | | 1.4 | | 1.6 | | 1.8 | | 2.4 | ns |
| t _{RD3} | FO = 3 Routing Delay | | 1.4 | | 1.6 | | 1.8 | | 2.1 | | 2.8 | ns |
| t _{RD4} | FO = 4 Routing Delay | | 1.7 | | 1.9 | | 2.2 | | 2.5 | | 3.3 | ns |
| t _{RD8} | FO = 8 Routing Delay | | 2.8 | | 3.2 | | 3.6 | | 4.2 | | 5.5 | ns |
| Logic Module Sequential Timing | | | | | | | | | | | | |
| t _{SUD} | Flip-Flop Data Input Setup | 0.5 | | 0.6 | | 0.7 | | 0.8 | | 0.8 | | ns |
| t _{HD} | Flip-Flop Data Input Hold | 0.0 | | 0.0 | | 0.0 | | 0.0 | | 0.0 | | ns |
| t _{SUD} | Latch Data Input Setup | 0.5 | | 0.6 | | 0.7 | | 0.8 | | 0.8 | | ns |
| t _{HD} | Latch Data Input Hold | 0.0 | | 0.0 | | 0.0 | | 0.0 | | 0.0 | | ns |
| t _{WASYN} | Asynchronous Pulse Width | 1.9 | | 2.4 | | 3.2 | | 3.8 | | 4.8 | | ns |
| t _{WCLKA} | Flip-Flop Clock Pulse Width | 1.9 | | 2.4 | | 3.2 | | 3.8 | | 4.8 | | ns |
| t _A | Flip-Flop Clock Input Period | 4.0 | | 5.0 | | 6.8 | | 8.0 | | 10.0 | | ns |
| f _{MAX} | Flip-Flop Clock Frequency | | 250 | | 200 | | 150 | | 125 | | 100 | MHz |

Notes:

- VCC = 3.0 V for 3.3 V specifications.
- For dual-module macros, use t_{PD} + t_{RD1} + t_{PDn} + t_{CO} + t_{RD1} + t_{PDn} or t_{PD1} + t_{RD1} + t_{SUD}, whichever is appropriate.
- The –2 and –3 speed grades have been discontinued. Please refer to the Product Discontinuation Notices (PDNs) listed below:
PDN March 2001
PDN 0104
PDN 0203
PDN 0604
PDN 1004
- Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual worst-case performance. Post-route timing is based on actual routing delay measurements performed on the device prior to shipment.

A1415A, A14V15A Timing Characteristics (continued)

Table 2-19 • A1415A, A14V15A Worst-Case Commercial Conditions, VCC = 4.75 V, T_J = 70°C

| I/O Module Input Propagation Delays | | –3 Speed ¹ | | –2 Speed ¹ | | –1 Speed | | Std. Speed | | 3.3 V Speed ² | | Units |
|---|--------------------------------|-----------------------|------|-----------------------|------|----------|------|------------|------|--------------------------|------|-------|
| Parameter/Description | | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | |
| t _{INY} | Input Data Pad to Y | | 2.8 | | 3.2 | | 3.6 | | 4.2 | | 5.5 | ns |
| t _{ICKY} | Input Reg IOCLK Pad to Y | | 4.7 | | 5.3 | | 6.0 | | 7.0 | | 9.2 | ns |
| t _{OCKY} | Output Reg IOCLK Pad to Y | | 4.7 | | 5.3 | | 6.0 | | 7.0 | | 9.2 | ns |
| t _{ICLRY} | Input Asynchronous Clear to Y | | 4.7 | | 5.3 | | 6.0 | | 7.0 | | 9.2 | ns |
| t _{OCLRY} | Output Asynchronous Clear to Y | | 4.7 | | 5.3 | | 6.0 | | 7.0 | | 9.2 | ns |
| Predicted Input Routing Delays² | | | | | | | | | | | | |
| t _{RD1} | FO = 1 Routing Delay | | 0.9 | | 1.0 | | 1.1 | | 1.3 | | 1.7 | ns |
| t _{RD2} | FO = 2 Routing Delay | | 1.2 | | 1.4 | | 1.6 | | 1.8 | | 2.4 | ns |
| t _{RD3} | FO = 3 Routing Delay | | 1.4 | | 1.6 | | 1.8 | | 2.1 | | 2.8 | ns |
| t _{RD4} | FO = 4 Routing Delay | | 1.7 | | 1.9 | | 2.2 | | 2.5 | | 3.3 | ns |
| t _{RD8} | FO = 8 Routing Delay | | 2.8 | | 3.2 | | 3.6 | | 4.2 | | 5.5 | ns |
| I/O Module Sequential Timing (wrt IOCLK pad) | | | | | | | | | | | | |
| t _{INH} | Input F-F Data Hold | 0.0 | | 0.0 | | 0.0 | | 0.0 | | 0.0 | | ns |
| t _{INSU} | Input F-F Data Setup | 2.0 | | 2.3 | | 2.5 | | 3.0 | | 3.0 | | ns |
| t _{IDEH} | Input Data Enable Hold | 0.0 | | 0.0 | | 0.0 | | 0.0 | | 0.0 | | ns |
| t _{IDESU} | Input Data Enable Setup | 5.8 | | 6.5 | | 7.5 | | 8.6 | | 8.6 | | ns |
| t _{OUTH} | Output F-F Data hold | 0.7 | | 0.8 | | 0.9 | | 1.0 | | 1.0 | | ns |
| t _{OUTSU} | Output F-F Data Setup | 0.7 | | 0.8 | | 0.9 | | 1.0 | | 1.0 | | ns |
| t _{ODEH} | Output Data Enable Hold | 0.3 | | 0.4 | | 0.4 | | 0.5 | | 0.5 | | ns |
| t _{ODESU} | Output Data Enable Setup | 1.3 | | 1.5 | | 1.7 | | 2.0 | | 2.0 | | ns |

Notes:

- The –2 and –3 speed grades have been discontinued. Please refer to the Product Discontinuation Notices (PDNs) listed below:
PDN March 2001
PDN 0104
PDN 0203
PDN 0604
PDN 1004
- Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual worst-case performance. Post-route timing is based on actual routing delay measurements performed on the device prior to shipment.

A1415A, A14V15A Timing Characteristics (continued)

Table 2-20 • A1415A, A14V15A Worst-Case Commercial Conditions, VCC = 4.75 V, T_J = 70°C

| I/O Module – TTL Output Timing ¹ | | –3 Speed ² | | –2 Speed ² | | –1 Speed | | Std. Speed | | 3.3 V Speed ¹ | | Units |
|--|------------------------------------|-----------------------|------|-----------------------|------|----------|------|------------|------|--------------------------|------|-------|
| Parameter/Description | | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | |
| t _{DHS} | Data to Pad, High Slew | | 5.0 | | 5.6 | | 6.4 | | 7.5 | | 9.8 | ns |
| t _{DLS} | Data to Pad, Low Slew | | 8.0 | | 9.0 | | 10.2 | | 12.0 | | 15.6 | ns |
| t _{ENZHS} | Enable to Pad, Z to H/L, High Slew | | 4.0 | | 4.5 | | 5.1 | | 6.0 | | 7.8 | ns |
| t _{ENZLS} | Enable to Pad, Z to H/L, Low Slew | | 7.4 | | 8.3 | | 9.4 | | 11.0 | | 14.3 | ns |
| t _{ENHSZ} | Enable to Pad, H/L to Z, High Slew | | 6.5 | | 7.5 | | 8.5 | | 10.0 | | 13.0 | ns |
| t _{ENLSZ} | Enable to Pad, H/L to Z, Low Slew | | 6.5 | | 7.5 | | 8.5 | | 10.0 | | 13.0 | ns |
| t _{CKHS} | IOCLK Pad to Pad H/L, High Slew | | 7.5 | | 7.5 | | 9.0 | | 10.0 | | 13.0 | ns |
| t _{CKLS} | IOCLK Pad to Pad H/L, Low Slew | | 11.3 | | 11.3 | | 13.5 | | 15.0 | | 19.5 | ns |
| d _{TLHHS} | Delta Low to High, High Slew | | 0.02 | | 0.02 | | 0.03 | | 0.03 | | 0.04 | ns/pF |
| d _{TLHLS} | Delta Low to High, Low Slew | | 0.05 | | 0.05 | | 0.06 | | 0.07 | | 0.09 | ns/pF |
| d _{THLHS} | Delta High to Low, High Slew | | 0.04 | | 0.04 | | 0.04 | | 0.05 | | 0.07 | ns/pF |
| d _{THLLS} | Delta High to Low, Low Slew | | 0.05 | | 0.05 | | 0.06 | | 0.07 | | 0.09 | ns/pF |
| I/O Module – CMOS Output Timing ¹ | | | | | | | | | | | | |
| t _{DHS} | Data to Pad, High Slew | | 6.2 | | 7.0 | | 7.9 | | 9.3 | | 12.1 | ns |
| t _{DLS} | Data to Pad, Low Slew | | 11.7 | | 13.1 | | 14.9 | | 17.5 | | 22.8 | ns |
| t _{ENZHS} | Enable to Pad, Z to H/L, High Slew | | 5.2 | | 5.9 | | 6.6 | | 7.8 | | 10.1 | ns |
| t _{ENZLS} | Enable to Pad, Z to H/L, Low Slew | | 8.9 | | 10.0 | | 11.3 | | 13.3 | | 17.3 | ns |
| t _{ENHSZ} | Enable to Pad, H/L to Z, High Slew | | 6.7 | | 7.5 | | 8.5 | | 10.0 | | 13.0 | ns |
| t _{ENLSZ} | Enable to Pad, H/L to Z, Low Slew | | 6.7 | | 7.5 | | 9.0 | | 10.0 | | 13.0 | ns |
| t _{CKHS} | IOCLK Pad to Pad H/L, High Slew | | 8.9 | | 8.9 | | 10.7 | | 11.8 | | 15.3 | ns |
| t _{CKLS} | IOCLK Pad to Pad H/L, Low Slew | | 13.0 | | 13.0 | | 15.6 | | 17.3 | | 22.5 | ns |
| d _{TLHHS} | Delta Low to High, High Slew | | 0.04 | | 0.04 | | 0.05 | | 0.06 | | 0.08 | ns/pF |
| d _{TLHLS} | Delta Low to High, Low Slew | | 0.07 | | 0.08 | | 0.09 | | 0.11 | | 0.14 | ns/pF |
| d _{THLHS} | Delta High to Low, High Slew | | 0.03 | | 0.03 | | 0.03 | | 0.04 | | 0.05 | ns/pF |
| d _{THLLS} | Delta High to Low, Low Slew | | 0.04 | | 0.04 | | 0.04 | | 0.05 | | 0.07 | ns/pF |

Notes:

- Delays based on 35 pF loading.
- The –2 and –3 speed grades have been discontinued. Please refer to the Product Discontinuation Notices (PDNs) listed below:

PDN March 2001
PDN 0104
PDN 0203
PDN 0604
PDN 1004

A1415A, A14V15A Timing Characteristics (continued)

Table 2-21 • A1415A, A14V15A Worst-Case Commercial Conditions, VCC = 4.75 V, T_J = 70°C

| Dedicated (hardwired) I/O Clock Network | | –3 Speed | | –2 Speed | | –1 Speed | | Std. Speed | | 3.3 V Speed ¹ | | Units |
|--|--|----------|------|----------|------|----------|------|------------|------|--------------------------|------|-------|
| Parameter/Description | | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | |
| t _{ILOCKH} | Input Low to High (pad to I/O module input) | | 2.0 | | 2.3 | | 2.6 | | 3.0 | | 3.5 | ns |
| t _{IOPWH} | Minimum Pulse Width High | 1.9 | | 2.4 | | 3.3 | | 3.8 | | 4.8 | | ns |
| t _{IPOWL} | Minimum Pulse Width Low | 1.9 | | 2.4 | | 3.3 | | 3.8 | | 4.8 | | ns |
| t _{IOSAPW} | Minimum Asynchronous Pulse Width | 1.9 | | 2.4 | | 3.3 | | 3.8 | | 4.8 | | ns |
| t _{ILOCKSW} | Maximum Skew | | 0.4 | | 0.4 | | 0.4 | | 0.4 | | 0.4 | ns |
| t _{IOP} | Minimum Period | 4.0 | | 5.0 | | 6.8 | | 8.0 | | 10.0 | | ns |
| f _{IOMAX} | Maximum Frequency | | 250 | | 200 | | 150 | | 125 | | 100 | MHz |
| Dedicated (hardwired) Array Clock | | | | | | | | | | | | |
| t _{HCKH} | Input Low to High (pad to S-module input) | | 3.0 | | 3.4 | | 3.9 | | 4.5 | | 5.5 | ns |
| t _{HCKL} | Input High to Low (pad to S-module input) | | 3.0 | | 3.4 | | 3.9 | | 4.5 | | 5.5 | ns |
| t _{HPWH} | Minimum Pulse Width High | 1.9 | | 2.4 | | 3.3 | | 3.8 | | 4.8 | | ns |
| t _{HPWL} | Minimum Pulse Width Low | 1.9 | | 2.4 | | 3.3 | | 3.8 | | 4.8 | | ns |
| t _{HCKSW} | Delta High to Low, Low Slew | | 0.3 | | 0.3 | | 0.3 | | 0.3 | | 0.3 | ns |
| t _{HP} | Minimum Period | 4.0 | | 5.0 | | 6.8 | | 8.0 | | 10.0 | | ns |
| f _{HMAX} | Maximum Frequency | | 250 | | 200 | | 150 | | 125 | | 100 | MHz |
| Routed Array Clock Networks | | | | | | | | | | | | |
| t _{RCKH} | Input Low to High (FO = 64) | | 3.7 | | 4.1 | | 4.7 | | 5.5 | | 9.0 | ns |
| t _{RCKL} | Input High to Low (FO = 64) | | 4.0 | | 4.5 | | 5.1 | | 6.0 | | 9.0 | ns |
| t _{RPWH} | Min. Pulse Width High (FO = 64) | 3.3 | | 3.8 | | 4.2 | | 4.9 | | 6.5 | | ns |
| t _{RPWL} | Min. Pulse Width Low (FO = 64) | 3.3 | | 3.8 | | 4.2 | | 4.9 | | 6.5 | | ns |
| t _{RCKSW} | Maximum Skew (FO = 128) | | 0.7 | | 0.8 | | 0.9 | | 1.0 | | 1.0 | ns |
| t _{RP} | Minimum Period (FO = 64) | 6.8 | | 8.0 | | 8.7 | | 10.0 | | 13.4 | | ns |
| f _{RMAX} | Maximum Frequency (FO = 64) | | 150 | | 125 | | 115 | | 100 | | 75 | MHz |
| Clock-to-Clock Skews | | | | | | | | | | | | |
| t _{IOHCKSW} | I/O Clock to H-Clock Skew | 0.0 | 1.7 | 0.0 | 1.8 | 0.0 | 2.0 | 0.0 | 2.2 | 0.0 | 3.0 | ns |
| t _{IORCKSW} | I/O Clock to R-Clock Skew (FO = 64) | 0.0 | 1.0 | 0.0 | 1.0 | 0.0 | 1.0 | 0.0 | 1.0 | 0.0 | 3.0 | ns |
| t _{HRCKSW} | H-Clock to R-Clock Skew (FO = 64) (FO = 50% maximum) | 0.0 | 1.0 | 0.0 | 1.0 | 0.0 | 1.0 | 0.0 | 1.0 | 0.0 | 3.0 | ns |

Notes:

- Delays based on 35 pF loading.
- The –2 and –3 speed grades have been discontinued. Refer to PDN 0104, PDN 0203, PDN 0604, and PDN 1004 at <http://www.microsemi.com/soc/support/notifications/default.aspx#pdn>.

A1440A, A14V40A Timing Characteristics (continued)

Table 2-27 • A1440A, A14V40A Worst-Case Commercial Conditions, VCC = 4.75 V, T_J = 70°C

| I/O Module Input Propagation Delays | | –3 Speed ¹ | | –2 Speed ¹ | | –1 Speed | | Std. Speed | | 3.3 V Speed ¹ | | Units |
|---|--------------------------------|-----------------------|------|-----------------------|------|----------|------|------------|------|--------------------------|------|-------|
| Parameter/Description | | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | |
| t _{INY} | Input Data Pad to Y | | 2.8 | | 3.2 | | 3.6 | | 4.2 | | 5.5 | ns |
| t _{ICKY} | Input Reg IOCLK Pad to Y | | 4.7 | | 5.3 | | 6.0 | | 7.0 | | 9.2 | ns |
| t _{OCKY} | Output Reg IOCLK Pad to Y | | 4.7 | | 5.3 | | 6.0 | | 7.0 | | 9.2 | ns |
| t _{ICLRY} | Input Asynchronous Clear to Y | | 4.7 | | 5.3 | | 6.0 | | 7.0 | | 9.2 | ns |
| t _{OCLRY} | Output Asynchronous Clear to Y | | 4.7 | | 5.3 | | 6.0 | | 7.0 | | 9.2 | ns |
| Predicted Input Routing Delays² | | | | | | | | | | | | |
| t _{RD1} | FO = 1 Routing Delay | | 0.9 | | 1.0 | | 1.1 | | 1.3 | | 1.7 | ns |
| t _{RD2} | FO = 2 Routing Delay | | 1.2 | | 1.4 | | 1.6 | | 1.8 | | 2.4 | ns |
| t _{RD3} | FO = 3 Routing Delay | | 1.4 | | 1.6 | | 1.8 | | 2.1 | | 2.8 | ns |
| t _{RD4} | FO = 4 Routing Delay | | 1.7 | | 1.9 | | 2.2 | | 2.5 | | 3.3 | ns |
| t _{RD8} | FO = 8 Routing Delay | | 2.8 | | 3.2 | | 3.6 | | 4.2 | | 5.5 | ns |
| I/O Module Sequential Timing (wrt IOCLK pad) | | | | | | | | | | | | |
| t _{INH} | Input F-F Data Hold | 0.0 | | 0.0 | | 0.0 | | 0.0 | | 0.0 | | ns |
| t _{INSU} | Input F-F Data Setup | 1.8 | | 1.7 | | 2.0 | | 2.3 | | 2.3 | | ns |
| t _{IDEH} | Input Data Enable Hold | 0.0 | | 0.0 | | 0.0 | | 0.0 | | 0.0 | | ns |
| t _{IDESU} | Input Data Enable Setup | 5.8 | | 6.5 | | 7.5 | | 8.6 | | 8.6 | | ns |
| t _{OUTH} | Output F-F Data hold | 0.7 | | 0.8 | | 0.9 | | 1.0 | | 1.0 | | ns |
| t _{OUTSU} | Output F-F Data Setup | 0.7 | | 0.8 | | 0.9 | | 1.0 | | 1.0 | | ns |
| t _{ODEH} | Output Data Enable Hold | 0.3 | | 0.4 | | 0.4 | | 0.5 | | 0.5 | | ns |
| f _{ODESU} | Output Data Enable Setup | 1.3 | | 1.5 | | 1.7 | | 2.0 | | 2.0 | | ns |

Notes:

1. The –2 and –3 speed grades have been discontinued. Refer to PDN 0104, PDN 0203, PDN 0604, and PDN 1004 at <http://www.microsemi.com/soc/support/notifications/default.aspx#pdn>.
2. Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual worst-case performance. Post-route timing is based on actual routing delay measurements performed on the device prior to shipment.

A1440A, A14V40A Timing Characteristics (continued)

Table 2-28 • A1440A, A14V40A Worst-Case Commercial Conditions, VCC = 4.75 V, T_J = 70°C

| I/O Module – TTL Output Timing ¹ | | –3 Speed ² | | –2 Speed ² | | –1 Speed | | Std. Speed | | 3.3 V Speed ¹ | | Units |
|--|------------------------------------|-----------------------|------|-----------------------|------|----------|------|------------|------|--------------------------|------|-------|
| Parameter/Description | | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | |
| t _{DHS} | Data to Pad, High Slew | | 5.0 | | 5.6 | | 6.4 | | 7.5 | | 9.8 | ns |
| t _{DLS} | Data to Pad, Low Slew | | 8.0 | | 9.0 | | 10.2 | | 12.0 | | 15.6 | ns |
| t _{ENZHS} | Enable to Pad, Z to H/L, High Slew | | 4.0 | | 4.5 | | 5.1 | | 6.0 | | 7.8 | ns |
| t _{ENZLS} | Enable to Pad, Z to H/L, Low Slew | | 7.4 | | 8.3 | | 9.4 | | 11.0 | | 14.3 | ns |
| t _{ENHSZ} | Enable to Pad, H/L to Z, High Slew | | 7.4 | | 8.3 | | 9.4 | | 11.0 | | 14.3 | ns |
| t _{ENLSZ} | Enable to Pad, H/L to Z, Low Slew | | 7.4 | | 8.3 | | 9.4 | | 11.0 | | 14.3 | ns |
| t _{CKHS} | IOCLK Pad to Pad H/L, High Slew | | 8.5 | | 8.5 | | 9.5 | | 11.0 | | 14.3 | ns |
| t _{CKLS} | IOCLK Pad to Pad H/L, Low Slew | | 11.3 | | 11.3 | | 13.5 | | 15.0 | | 19.5 | ns |
| d _{TLHHS} | Delta Low to High, High Slew | | 0.02 | | 0.02 | | 0.03 | | 0.03 | | 0.04 | ns/pF |
| d _{TLHLS} | Delta Low to High, Low Slew | | 0.05 | | 0.05 | | 0.06 | | 0.07 | | 0.09 | ns/pF |
| d _{THLHS} | Delta High to Low, High Slew | | 0.04 | | 0.04 | | 0.04 | | 0.05 | | 0.07 | ns/pF |
| d _{THLLS} | Delta High to Low, Low Slew | | 0.05 | | 0.05 | | 0.06 | | 0.07 | | 0.09 | ns/pF |
| I/O Module – CMOS Output Timing ¹ | | | | | | | | | | | | |
| t _{DHS} | Data to Pad, High Slew | | 6.2 | | 7.0 | | 7.9 | | 9.3 | | 12.1 | ns |
| t _{DLS} | Data to Pad, Low Slew | | 11.7 | | 13.1 | | 14.9 | | 17.5 | | 22.8 | ns |
| t _{ENZHS} | Enable to Pad, Z to H/L, High Slew | | 5.2 | | 5.9 | | 6.6 | | 7.8 | | 10.1 | ns |
| t _{ENZLS} | Enable to Pad, Z to H/L, Low Slew | | 8.9 | | 10.0 | | 11.3 | | 13.3 | | 17.3 | ns |
| t _{ENHSZ} | Enable to Pad, H/L to Z, High Slew | | 7.4 | | 8.3 | | 9.4 | | 11.0 | | 14.3 | ns |
| t _{ENLSZ} | Enable to Pad, H/L to Z, Low Slew | | 7.4 | | 8.3 | | 9.4 | | 11.0 | | 14.3 | ns |
| t _{CKHS} | IOCLK Pad to Pad H/L, High Slew | | 9.0 | | 9.0 | | 10.1 | | 11.8 | | 14.3 | ns |
| t _{CKLS} | IOCLK Pad to Pad H/L, Low Slew | | 13.0 | | 13.0 | | 15.6 | | 17.3 | | 22.5 | ns |
| d _{TLHHS} | Delta Low to High, High Slew | | 0.04 | | 0.04 | | 0.05 | | 0.06 | | 0.08 | ns/pF |
| d _{TLHLS} | Delta Low to High, Low Slew | | 0.07 | | 0.08 | | 0.09 | | 0.11 | | 0.14 | ns/pF |
| d _{THLHS} | Delta High to Low, High Slew | | 0.03 | | 0.03 | | 0.03 | | 0.04 | | 0.05 | ns/pF |
| d _{THLLS} | Delta High to Low, Low Slew | | 0.04 | | 0.04 | | 0.04 | | 0.05 | | 0.07 | ns/pF |

Notes:

1. Delays based on 35 pF loading.
2. The –2 and –3 speed grades have been discontinued. Refer to PDN 0104, PDN 0203, PDN 0604, and PDN 1004 at <http://www.microsemi.com/soc/support/notifications/default.aspx#pdn>.

A1440A, A14V40A Timing Characteristics (continued)

Table 2-29 • A1440A, A14V40A Worst-Case Commercial Conditions, VCC = 4.75 V, T_J = 70°C

| Dedicated (hardwired) I/O Clock Network | | –3 Speed ¹ | | –2 Speed ¹ | | –1 Speed | | Std. Speed | | 3.3 V Speed ¹ | | Units |
|--|---|-----------------------|------|-----------------------|------|----------|------|------------|------|--------------------------|------|-------|
| Parameter/Description | | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | |
| t _{ILOCKH} | Input Low to High (pad to I/O module input) | | 2.0 | | 2.3 | | 2.6 | | 3.0 | | 3.5 | ns |
| t _{IOPWH} | Minimum Pulse Width High | 1.9 | | 2.4 | | 3.3 | | 3.8 | | 4.8 | | ns |
| t _{IPOWL} | Minimum Pulse Width Low | 1.9 | | 2.4 | | 3.3 | | 3.8 | | 4.8 | | ns |
| t _{IOSAPW} | Minimum Asynchronous Pulse Width | 1.9 | | 2.4 | | 3.3 | | 3.8 | | 4.8 | | ns |
| t _{ILOCKSW} | Maximum Skew | | 0.4 | | 0.4 | | 0.4 | | 0.4 | | 0.4 | ns |
| t _{IOP} | Minimum Period | 4.0 | | 5.0 | | 6.8 | | 8.0 | | 10.0 | | ns |
| f _{IOMAX} | Maximum Frequency | | 250 | | 200 | | 150 | | 125 | | 100 | MHz |
| Dedicated (hardwired) Array Clock | | | | | | | | | | | | |
| t _{HCKH} | Input Low to High (pad to S-module input) | | 3.0 | | 3.4 | | 3.9 | | 4.5 | | 5.5 | ns |
| t _{HCKL} | Input High to Low (pad to S-module input) | | 3.0 | | 3.4 | | 3.9 | | 4.5 | | 5.5 | ns |
| t _{HPWH} | Minimum Pulse Width High | 1.9 | | 2.4 | | 3.3 | | 3.8 | | 4.8 | | ns |
| t _{HPWL} | Minimum Pulse Width Low | 1.9 | | 2.4 | | 3.3 | | 3.8 | | 4.8 | | ns |
| t _{HCKSW} | Delta High to Low, Low Slew | | 0.3 | | 0.3 | | 0.3 | | 0.3 | | 0.3 | ns |
| t _{HP} | Minimum Period | 4.0 | | 5.0 | | 6.8 | | 8.0 | | 10.0 | | ns |
| f _{HMAX} | Maximum Frequency | | 250 | | 200 | | 150 | | 125 | | 100 | MHz |
| Routed Array Clock Networks | | | | | | | | | | | | |
| t _{RCKH} | Input Low to High (FO = 64) | | 3.7 | | 4.1 | | 4.7 | | 5.5 | | 9.0 | ns |
| t _{RCKL} | Input High to Low (FO = 64) | | 4.0 | | 4.5 | | 5.1 | | 6.0 | | 9.0 | ns |
| t _{RPWH} | Min. Pulse Width High (FO = 64) | 3.3 | | 3.8 | | 4.2 | | 4.9 | | 6.5 | | ns |
| t _{RPWL} | Min. Pulse Width Low (FO = 64) | 3.3 | | 3.8 | | 4.2 | | 4.9 | | 6.5 | | ns |
| t _{RCKSW} | Maximum Skew (FO = 128) | | 0.7 | | 0.8 | | 0.9 | | 1.0 | | 1.0 | ns |
| t _{RP} | Minimum Period (FO = 64) | 6.8 | | 8.0 | | 8.7 | | 10.0 | | 13.4 | | ns |
| f _{RMAX} | Maximum Frequency (FO = 64) | | 150 | | 125 | | 115 | | 100 | | 75 | MHz |
| Clock-to-Clock Skews | | | | | | | | | | | | |
| t _{IOHCKSW} | I/O Clock to H-Clock Skew | 0.0 | 1.7 | 0.0 | 1.8 | 0.0 | 2.0 | 0.0 | 2.2 | 0.0 | 3.0 | ns |
| t _{IORCKSW} | I/O Clock to R-Clock Skew (FO = 64) (FO = 144) | 0.0 | 1.0 | 0.0 | 1.0 | 0.0 | 1.0 | 0.0 | 1.0 | 0.0 | 3.0 | ns |
| | | 0.0 | 3.0 | 0.0 | 3.0 | 0.0 | 3.0 | 0.0 | 3.0 | 0.0 | 3.0 | |
| t _{HRCKSW} | H-Clock to R-Clock Skew (FO = 64) (FO = 144) | 0.0 | 1.0 | 0.0 | 1.0 | 0.0 | 1.0 | 0.0 | 1.0 | 0.0 | 1.0 | ns |
| | | 0.0 | 3.0 | 0.0 | 3.0 | 0.0 | 3.0 | 0.0 | 3.0 | 0.0 | 3.0 | |

Notes:

1. The –2 and –3 speed grades have been discontinued. Refer to PDN 0104, PDN 0203, PDN 0604, and PDN 1004 at <http://www.microsemi.com/soc/support/notifications/default.aspx#pdn>.
2. Delays based on 35 pF loading.

A1460A, A14V60A Timing Characteristics (continued)

Table 2-31 • A1460A, A14V60A Worst-Case Commercial Conditions, VCC = 4.75 V, T_J = 70°C

| I/O Module Input Propagation Delays | | –3 Speed ¹ | | –2 Speed ¹ | | –1 Speed | | Std. Speed | | 3.3 V Speed ¹ | | Units |
|---|--------------------------------|-----------------------|------|-----------------------|------|----------|------|------------|------|--------------------------|------|-------|
| Parameter/Description | | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | |
| t _{INY} | Input Data Pad to Y | | 2.8 | | 3.2 | | 3.6 | | 4.2 | | 5.5 | ns |
| t _{ICKY} | Input Reg IOCLK Pad to Y | | 4.7 | | 5.3 | | 6.0 | | 7.0 | | 9.2 | ns |
| t _{OCKY} | Output Reg IOCLK Pad to Y | | 4.7 | | 5.3 | | 6.0 | | 7.0 | | 9.2 | ns |
| t _{ICLRY} | Input Asynchronous Clear to Y | | 4.7 | | 5.3 | | 6.0 | | 7.0 | | 9.2 | ns |
| t _{OCLRY} | Output Asynchronous Clear to Y | | 4.7 | | 5.3 | | 6.0 | | 7.0 | | 9.2 | ns |
| Predicted Input Routing Delays² | | | | | | | | | | | | |
| t _{RD1} | FO = 1 Routing Delay | | 0.9 | | 1.0 | | 1.1 | | 1.3 | | 1.7 | ns |
| t _{RD2} | FO = 2 Routing Delay | | 1.2 | | 1.4 | | 1.6 | | 1.8 | | 2.4 | ns |
| t _{RD3} | FO = 3 Routing Delay | | 1.4 | | 1.6 | | 1.8 | | 2.1 | | 2.8 | ns |
| t _{RD4} | FO = 4 Routing Delay | | 1.7 | | 1.9 | | 2.2 | | 2.5 | | 3.3 | ns |
| t _{RD8} | FO = 8 Routing Delay | | 2.8 | | 3.2 | | 3.6 | | 4.2 | | 5.5 | ns |
| I/O Module Sequential Timing (wrt IOCLK pad) | | | | | | | | | | | | |
| t _{INH} | Input F-F Data Hold | 0.0 | | 0.0 | | 0.0 | | 0.0 | | 0.0 | | ns |
| t _{INSU} | Input F-F Data Setup | 1.3 | | 1.5 | | 1.8 | | 2.0 | | 2.0 | | ns |
| t _{IDEH} | Input Data Enable Hold | 0.0 | | 0.0 | | 0.0 | | 0.0 | | 0.0 | | ns |
| t _{IDESU} | Input Data Enable Setup | 5.8 | | 6.5 | | 7.5 | | 8.6 | | 8.6 | | ns |
| t _{OUTH} | Output F-F Data hold | 0.7 | | 0.8 | | 0.9 | | 1.0 | | 1.0 | | ns |
| t _{OUTSU} | Output F-F Data Setup | 0.7 | | 0.8 | | 0.9 | | 1.0 | | 1.0 | | ns |
| t _{ODEH} | Output Data Enable Hold | 0.3 | | 0.4 | | 0.4 | | 0.5 | | 0.5 | | ns |
| f _{ODESU} | Output Data Enable Setup | 1.3 | | 1.5 | | 1.7 | | 2.0 | | 2.0 | | ns |

Notes:

5. The –2 and –3 speed grades have been discontinued. Refer to PDN 0104, PDN 0203, PDN 0604, and PDN 1004 at <http://www.microsemi.com/soc/support/notifications/default.aspx#pdn>.
6. Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual worst-case performance. Post-route timing is based on actual routing delay measurements performed on the device prior to shipment.

Pin Descriptions

CLKA **Clock A (Input)**

Clock input for clock distribution networks. The Clock input is buffered prior to clocking the logic modules. This pin can also be used as an I/O.

CLKB **Clock B (Input)**

Clock input for clock distribution networks. The Clock input is buffered prior to clocking the logic modules. This pin can also be used as an I/O.

GND **Ground**

LOW supply voltage.

HCLK **Dedicated (Hard-wired) Array Clock (Input)**

Clock input for sequential modules. This input is directly wired to each S-Module and offers clock speeds independent of the number of S-Modules being driven. This pin can also be used as an I/O.

I/O **Input/Output (Input, Output)**

The I/O pin functions as an input, output, three-state, or bidirectional buffer. Input and output levels are compatible with standard TTL and CMOS specifications. Unused I/O pins are tristated by the Designer Series software.

IOCLK **Dedicated (Hard-wired) I/O Clock (Input)**

Clock input for I/O modules. This input is directly wired to each I/O module and offers clock speeds independent of the number of I/O modules being driven. This pin can also be used as an I/O.

IOPCL **Dedicated (Hard-wired) I/O Preset/Clear (Input)**

Input for I/O preset or clear. This global input is directly wired to the preset and clear inputs of all I/O registers. This pin functions as an I/O when no I/O preset or clear macros are used.

MODE **Mode (Input)**

The MODE pin controls the use of diagnostic pins (DCLK, PRA, PRB, SDI). When the MODE pin is HIGH, the special functions are active. When the MODE pin is LOW, the pins function as I/Os. To provide Actionprobe capability, the MODE pin should be terminated to GND through a 10K resistor so that the MODE pin can be pulled high when required.

NC **No Connection**

This pin is not connected to circuitry within the device.

PRA **Probe A (Output)**

The Probe A pin is used to output data from any user-defined design node within the device. This independent diagnostic pin can be used in conjunction with the Probe B pin to allow real-time diagnostic output of any signal path within the device. The Probe A pin can be used as a user-defined I/O when debugging has been completed. The pin's probe capabilities can be permanently disabled to protect programmed design confidentiality. PRA is accessible when the MODE pin is HIGH. This pin functions as an I/O when the MODE pin is LOW.

PRB **Probe B (Output)**

The Probe B pin is used to output data from any user-defined design node within the device. This independent diagnostic pin can be used in conjunction with the Probe A pin to allow real-time diagnostic output of any signal path within the device. The Probe B pin can be used as a user-defined I/O when debugging has been completed. The pin's probe capabilities can be permanently disabled to protect programmed design confidentiality. PRB is accessible when the MODE pin is HIGH. This pin functions as an I/O when the MODE pin is LOW.

SDI **Serial Data Input (Input)**

Serial data input for diagnostic probe and device programming. SDI is active when the MODE pin is HIGH. This pin functions as an I/O when the MODE pin is LOW.

| PL84 | | | |
|------------|------------------------|------------------------|------------------------|
| Pin Number | A1415, A14V15 Function | A1425, A14V25 Function | A1440, A14V40 Function |
| 1 | VCC | VCC | VCC |
| 2 | GND | GND | GND |
| 3 | VCC | VCC | VCC |
| 4 | PRA, I/O | PRA, I/O | PRA, I/O |
| 11 | DCLK, I/O | DCLK, I/O | DCLK, I/O |
| 12 | SDI, I/O | SDI, I/O | SDI, I/O |
| 16 | MODE | MODE | MODE |
| 27 | GND | GND | GND |
| 28 | VCC | VCC | VCC |
| 40 | PRB, I/O | PRB, I/O | PRB, I/O |
| 41 | VCC | VCC | VCC |
| 42 | GND | GND | GND |
| 43 | VCC | VCC | VCC |
| 45 | HCLK, I/O | HCLK, I/O | HCLK, I/O |
| 52 | SDO | SDO | SDO |
| 53 | IOPCL, I/O | IOPCL, I/O | IOPCL, I/O |
| 59 | VCC | VCC | VCC |
| 60 | VCC | VCC | VCC |
| 61 | GND | GND | GND |
| 68 | VCC | VCC | VCC |
| 69 | GND | GND | GND |
| 74 | IOCLK, I/O | IOCLK, I/O | IOCLK, I/O |
| 83 | CLKA, I/O | CLKA, I/O | CLKA, I/O |
| 84 | CLKB, I/O | CLKB, I/O | CLKB, I/O |

Notes:

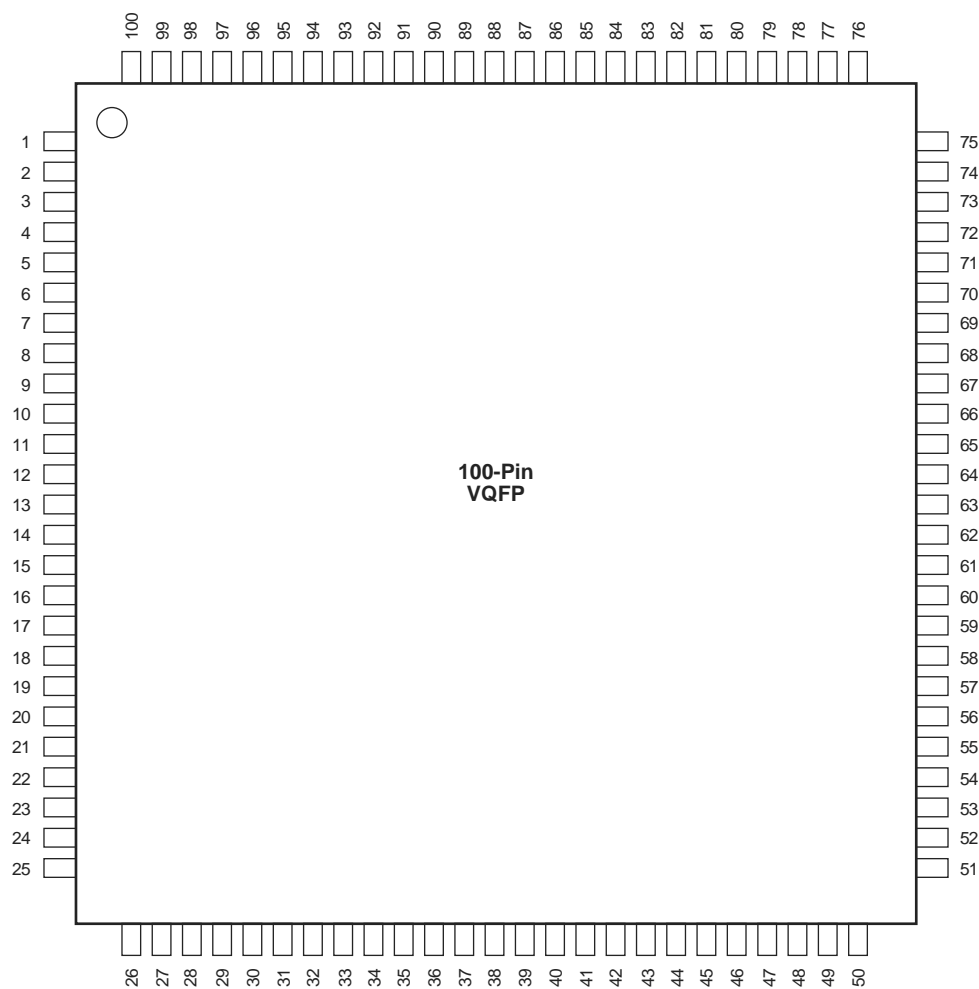
1. All unlisted pin numbers are user I/Os.
2. NC denotes no connection.
3. MODE should be terminated to GND through a 10K resistor to enable Actionprobe usage; otherwise it can be terminated directly to GND.

| PQ160 | | | |
|------------|------------------------|------------------------|------------------------|
| Pin Number | A1425, A14V25 Function | A1440, A14V40 Function | A1460, A14V60 Function |
| 92 | NC | I/O | I/O |
| 93 | NC | I/O | I/O |
| 98 | GND | GND | GND |
| 99 | VCC | VCC | VCC |
| 100 | NC | I/O | I/O |
| 103 | GND | GND | GND |
| 107 | NC | I/O | I/O |
| 109 | NC | I/O | I/O |
| 110 | VCC | VCC | VCC |
| 111 | GND | GND | GND |
| 112 | VCC | VCC | VCC |
| 113 | NC | I/O | I/O |
| 119 | NC | I/O | I/O |
| 120 | IOCLK, I/O | IOCLK, I/O | IOCLK, I/O |
| 121 | GND | GND | GND |
| 124 | NC | I/O | I/O |
| 127 | NC | I/O | I/O |
| 136 | CLKA, I/O | CLKA, I/O | CLKA, I/O |
| 137 | CLKB, I/O | CLKB, I/O | CLKB, I/O |
| 138 | VCC | VCC | VCC |
| 139 | GND | GND | GND |
| 140 | VCC | VCC | VCC |
| 141 | GND | GND | GND |
| 142 | PRA, I/O | PRA, I/O | PRA, I/O |
| 143 | NC | I/O | I/O |
| 145 | NC | I/O | I/O |
| 147 | NC | I/O | I/O |
| 149 | NC | I/O | I/O |
| 151 | NC | I/O | I/O |
| 153 | NC | I/O | I/O |
| 154 | VCC | VCC | VCC |
| 160 | DCLK, I/O | DCLK, I/O | DCLK, I/O |

Notes:

1. All unlisted pin numbers are user I/Os.
2. NC denotes no connection.
3. MODE should be terminated to GND through a 10K resistor to enable Actionprobe usage; otherwise it can be terminated directly to GND.

VQ100



Note: This is the top view.

Note

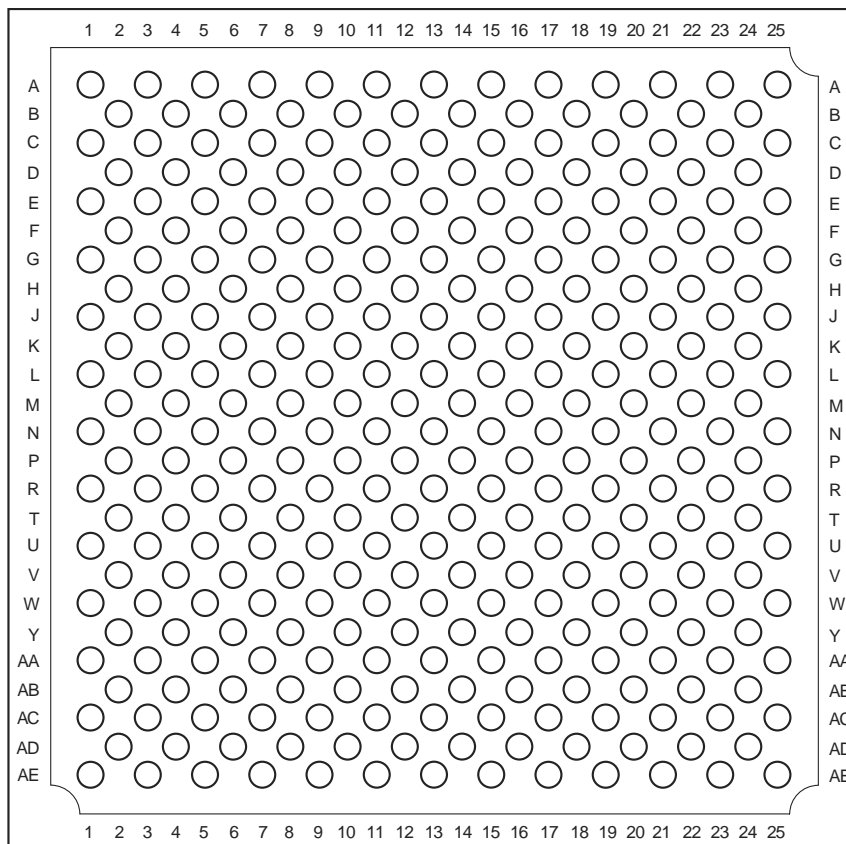
For Package Manufacturing and Environmental information, visit the Resource Center at <http://www.microsemi.com/soc/products/solutions/package/docs.aspx>

| BG225 | |
|----------------|---|
| A1460 Function | Location |
| CLKA or I/O | C8 |
| CLKB or I/O | B8 |
| DCLK or I/O | B2 |
| GND | A1, A15, D15, F8, G7, G8, G9, H6, H7, H8, H9, H10, J7, J8, J9, K8, P2, R15 |
| HCLK or I/O | P9 |
| IOCLK or I/O | B14 |
| IOPCL or I/O | P14 |
| MODE | D1 |
| NC | A11, B5, B7, D8, D12, F6, F11, H1, H12, H14, K11, L1, L13, N8, P5, R1, R8, R11, R14 |
| PRA or I/O | A7 |
| PRB or I/O | L7 |
| SDI or I/O | D4 |
| SDO | N13 |
| VCC | A8, B12, D5, D14, E3, E8, E13, H2, H3, H11, H15, K4, L2, L12, M8, M15, P4, P8, R13 |

Notes:

1. All unlisted pin numbers are user I/Os.
2. NC denotes no connection.
3. MODE should be terminated to GND through a 10K resistor to enable Actionprobe usage; otherwise it can be terminated directly to GND.
4. The BG225 package has been discontinued.

BG313



Note: This is the top view.

Note

For Package Manufacturing and Environmental information, visit the Resource Center at <http://www.microsemi.com/soc/products/solutions/package/docs.aspx>

| PG100 | |
|----------------|--|
| A1415 Function | Location |
| CLKA or I/O | C7 |
| CLKB or I/O | D6 |
| DCLK or I/O | C4 |
| GND | C3, C6, C9, E9, F3, F9, J3, J6, J8, J9 |
| HCLK or I/O | H6 |
| IOCLK or I/O | C10 |
| IOPCL or I/O | K9 |
| MODE | C2 |
| PRA or I/O | A6 |
| PRB or I/O | L3 |
| SDI or I/O | B3 |
| SDO | L9 |
| VCC | B6, B10, E11, F2, F10, G2, K2, K6, K10 |

Notes:

1. All unlisted pin numbers are user I/Os.
2. NC denotes no connection.
3. MODE should be terminated to GND through a 10K resistor to enable Actionprobe usage; otherwise it can be terminated directly to GND.
4. The PG100 package has been discontinued.

Datasheet Categories

Categories

In order to provide the latest information to designers, some datasheet parameters are published before data has been fully characterized from silicon devices. The data provided for a given device is designated as either "Product Brief," "Advance," "Preliminary," or "Production." The definitions of these categories are as follows:

Product Brief

The product brief is a summarized version of a datasheet (advance or production) and contains general product information. This document gives an overview of specific device and family information.

Advance

This version contains initial estimated information based on simulation, other products, devices, or speed grades. This information can be used as estimates, but not for production. This label only applies to the DC and Switching Characteristics chapter of the datasheet and will only be used when the data has not been fully characterized.

Preliminary

The datasheet contains information based on simulation and/or initial characterization. The information is believed to be correct, but changes are possible.

Production

This version contains information that is considered to be final.

Export Administration Regulations (EAR)

The products described in this document are subject to the Export Administration Regulations (EAR). They could require an approved export license prior to export from the United States. An export includes release of product or disclosure of technology to a foreign national inside or outside the United States.

Safety Critical, Life Support, and High-Reliability Applications Policy

The products described in this advance status document may not have completed the Microsemi qualification process. Products may be amended or enhanced during the product introduction and qualification process, resulting in changes in device functionality or performance. It is the responsibility of each customer to ensure the fitness of any product (but especially a new product) for a particular purpose, including appropriateness for safety-critical, life-support, and other high-reliability applications. Consult the Microsemi SoC Products Group Terms and Conditions for specific liability exclusions relating to life-support applications. A reliability report covering all of the SoC Products Group's products is available at http://www.microsemi.com/soc/documents/ORT_Report.pdf. Microsemi also offers a variety of enhanced qualification and lot acceptance screening procedures. Contact your local sales office for additional reliability information.