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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.
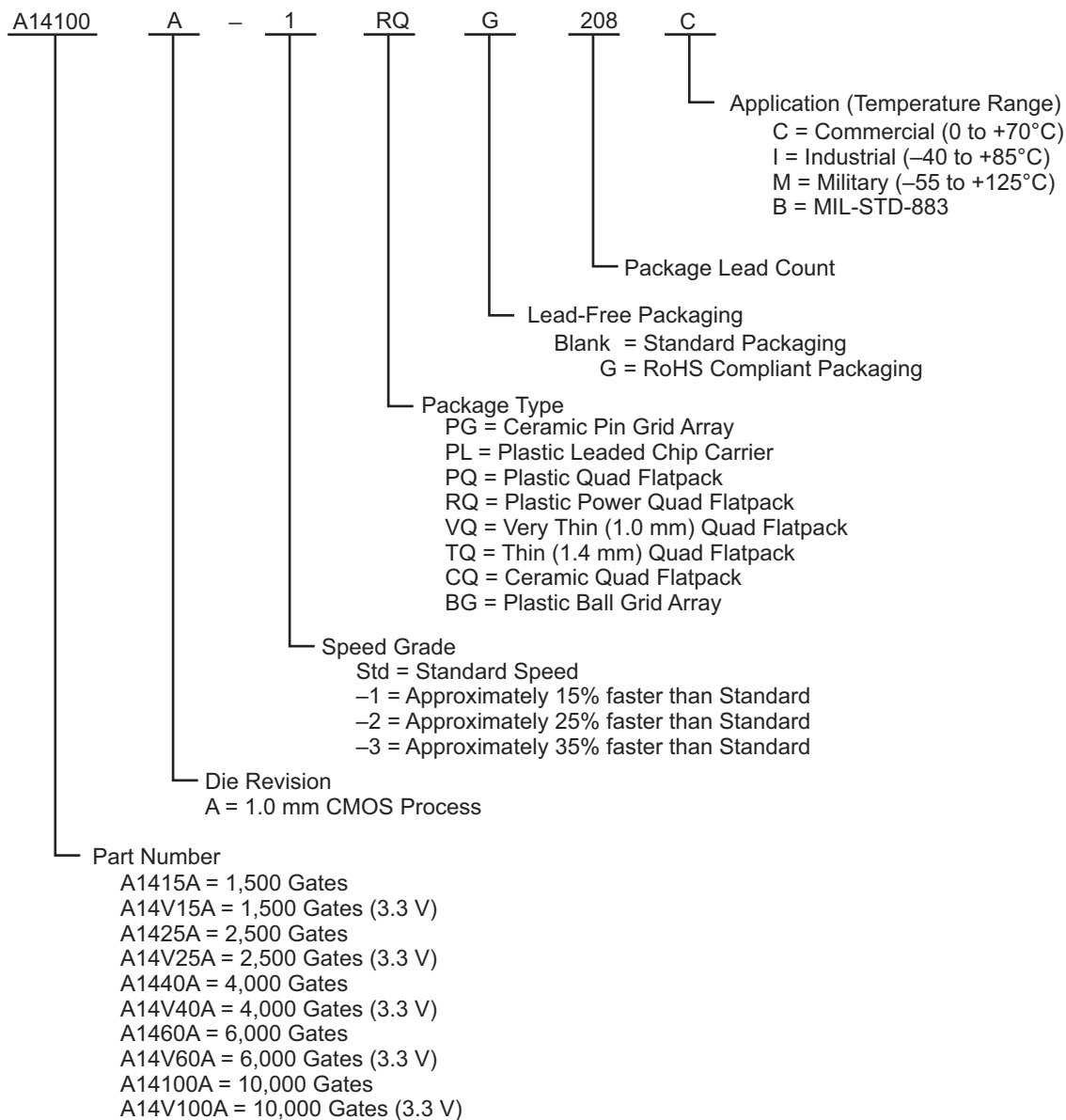
Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications,

Details	
Product Status	Obsolete
Number of LABs/CLBs	1377
Number of Logic Elements/Cells	-
Total RAM Bits	-
Number of I/O	228
Number of Gates	10000
Voltage - Supply	4.5V ~ 5.5V
Mounting Type	Surface Mount
Operating Temperature	-55°C ~ 125°C (TC)
Package / Case	256-BFCQFP with Tie Bar
Supplier Device Package	256-CQFP (75x75)
Purchase URL	https://www.e-xfl.com/product-detail/microsemi/a14100a-cq256m

Microsemi

Ordering Information

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A14100    A  –  1    RQ    G    208    C
```

Application (Temperature Range)
C = Commercial (0 to +70°C)
I = Industrial (–40 to +85°C)
M = Military (–55 to +125°C)
B = MIL-STD-883

Package Lead Count

Lead-Free Packaging
Blank = Standard Packaging
G = RoHS Compliant Packaging

Package Type
PG = Ceramic Pin Grid Array
PL = Plastic Leaded Chip Carrier
PQ = Plastic Quad Flatpack
RQ = Plastic Power Quad Flatpack
VQ = Very Thin (1.0 mm) Quad Flatpack
TQ = Thin (1.4 mm) Quad Flatpack
CQ = Ceramic Quad Flatpack
BG = Plastic Ball Grid Array

Speed Grade
Std = Standard Speed
–1 = Approximately 15% faster than Standard
–2 = Approximately 25% faster than Standard
–3 = Approximately 35% faster than Standard

Die Revision
A = 1.0 mm CMOS Process

Part Number
A1415A = 1,500 Gates
A14V15A = 1,500 Gates (3.3 V)
A1425A = 2,500 Gates
A14V25A = 2,500 Gates (3.3 V)
A1440A = 4,000 Gates
A14V40A = 4,000 Gates (3.3 V)
A1460A = 6,000 Gates
A14V60A = 6,000 Gates (3.3 V)
A14100A = 10,000 Gates
A14V100A = 10,000 Gates (3.3 V)

Notes:
1. The –2 and –3 speed grades have been discontinued.
2. The Ceramic Pin Grid Array packages PG100, PG133, and PG175 have been discontinued in all device densities, speed grades, and temperature grades.
3. The Plastic Ball Grid Array package BG225 has been discontinued in all device densities (specifically for A1460A), all speed grades, and all temperature grades.
4. Military Grade devices are no longer available for the A1440A device.
5. For more information about discontinued devices, refer to the Product Discontinuation Notices (PDNs) listed below, available on the Microsemi SoC Products Group website:
PDN March 2001
PDN 0104
PDN 0203
PDN 0604
PDN 1004

Product Plan

Device/Package	Speed Grade[1]				Application[1]			
	Std.	−1	−2	−3	C	I	M	B
A1415A Device								
84-Pin Plastic Leaded Chip Carrier (PLCC)	✓	✓	D	D	✓	✓	✓	−
100-Pin Plastic Quad Flatpack (PQFP)	✓	✓	D	D	✓	✓	✓	−
100-Pin Very Thin Quad Flatpack (VQFP)	✓	✓	D	D	✓	✓	✓	−
100-Pin Ceramic Pin Grid Array (CPGA)	D	D	D	D	D	−	−	−
A14V15A Device								
84-Pin Plastic Leaded Chip Carrier (PLCC)	✓	−	−	−	✓	−	−	−
100-Pin Very Thin Quad Flatpack (VQFP)	✓	−	−	−	✓	−	−	−
A1425A Device								
84-Pin Plastic Leaded Chip Carrier (PLCC)	✓	✓	D	D	✓	✓		
100-Pin Plastic Quad Flatpack (PQFP)	✓	✓	D	D	✓	✓	−	−
100-Pin Very Thin Quad Flatpack (VQFP)	✓	✓	D	D	✓	✓	−	−
132-Pin Ceramic Quad Flatpack (CQFP)	✓	✓	−	−	✓	−	✓	✓
133-Pin Ceramic Pin Grid Array (CPGA)	D	D	D	D	D	−	D	D
160-Pin Plastic Quad Flatpack (PQFP)	✓	✓	D	D	✓	✓	−	−
A14V25A Device								
84-Pin Plastic Leaded Chip Carrier (PLCC)	✓	−	−	−	✓	−	−	−
100-Pin Very Thin Quad Flatpack (VQFP)	✓	−	−	−	✓	−	−	−
160-Pin Plastic Quad Flatpack (PQFP)	✓	−	−	−	✓	−	−	−
A1440A Device								
84-Pin Plastic Leaded Chip Carrier (PLCC)	✓	✓	D	D	✓	✓	−	−
100-Pin Very Thin Quad Flatpack (VQFP)	✓	✓	D	D	✓	✓	−	−
160-Pin Plastic Quad Flatpack (PQFP)	✓	✓	D	D	✓	✓	−	−
175-Pin Ceramic Pin Grid Array (CPGA)	D	D	D	D	D	−	−	−
176-Pin Thin Quad Flatpack (TQFP)	✓	✓	D	D	✓	✓	−	−

Notes:
1. *Applications:*
   C = Commercial
   I = Industrial
   M = Military
2. *Commercial only*

Availability:
✓ = Available
P = Planned
− = Not planned
D = Discontinued

Speed Grade:
−1 = Approx. 15% faster than Std.
−2 = Approx. 25% faster than Std.
−3 = Approx. 35% faster than Std.
(−2 and −3 speed grades have been discontinued.)

5 V Operating Conditions

Table 2-2 • **Absolute Maximum Ratings[1], Free Air Temperature Range**

Symbol	Parameter	Limits	Units
VCC	DC supply voltage	−0.5 to +7.0	V
VI	Input voltage	−0.5 to VCC + 0.5	V
VO	Output voltage	−0.5 to VCC + 0.5	V
IIO	I/O source sink current[2]	±20	mA
T_{STG}	Storage temperature	−65 to +150	°C

Notes:

1. *Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum rated conditions for extended periods may affect device reliability. Device should not be operated outside the recommended operating conditions.*

2. *Device inputs are normally high impedance and draw extremely low current. However, when input voltage is greater than VCC + 0.5 V for less than GND −0.5 V, the internal protection diodes will forward bias and can draw excessive current.*

Table 2-3 • **Recommended Operating Conditions**

Parameter	Commercial	Industrial	Military	Units
Temperature range*	0 to +70	−40 to +85	−55 to +125	°C
5 V power supply tolerance	±5	±10	±10	%VCC

Note: **Ambient temperature (T_A) is used for commercial and industrial; case temperature (T_C) is used for military.*

Table 2-4 • **Electrical Specifications**

Symbol	Parameter	Test Condition	Commercial Min.	Commercial Max.	Industrial Min.	Industrial Max.	Military Min.	Military Max.	Units
VOH[1,2]	High level output	IOH = −4 mA (CMOS)	–	–	3.7	–	3.7	–	V
		IOH = −6 mA (CMOS)	3.84						V
		IOH = −10 mA (TTL)[3]	2.40						V
VOL[1,2]	Low level output	IOL = +6 mA (CMOS)		0.33		0.4		0.4	V
		IOL = +12 mA (TTL)[3]		0.50					V
VIH	High level input	TTL inputs	2.0	VCC + 0.3	2.0	VCC + 0.3	2.0	VCC + 0.3	V
VIL	Low level input	TTL inputs	−0.3	0.8	−0.3	0.8	−0.3	0.8	V
IIN	Input leakage	VI = VCC or GND	−10	+10	−10	+10	−10	+10	µA
IOZ	3-state output leakage	VO = VCC or GND	−10	+10	−10	+10	−10	+10	µA
C_{IO}	I/O capacitance[3,4]			10		10		10	pF
ICC(S)	Standby VCC supply current (typical = 0.7 mA)			2		10		20	mA
ICC(D)	Dynamic VCC supply current. See the Power Dissipation section.								

Notes:

1. *Microsemi devices can drive and receive either CMOS or TTL signal levels. No assignment of I/Os as TTL or CMOS is required.*

2. *Tested one output at a time, VCC = minimum.*

3. *Not tested; for information only.*

4. *VOUT = 0 V, f = 1 MHz*

5. *Typical standby current = 0.7 mA. All outputs unloaded. All inputs = VCC or GND.*

Package Thermal Characteristics

The device junction to case thermal characteristic is θjc, and the junction to ambient air characteristic is θja. The thermal characteristics for θja are shown with two different air flow rates.

Maximum junction temperature is 150°C.

A sample calculation of the absolute maximum power dissipation allowed for a CPGA 175-pin package at commercial temperature and still air is as follows:

$$\frac{\text{Max. junction temp. (°C)} - \text{Max. ambient temp. (°C)}}{\theta_{ja}\,°C/W} = \frac{150°C - 70°C}{25°C/W} = 3.2\ W$$

EQ 2

Table 2-8 • **Package Thermal Characteristics**

Package Type*	Pin Count	θ_{jc}	θ_{ja} Still Air	θ_{ja} 300 ft./min.	Units
Ceramic Pin Grid Array	100	20	35	17	°C/W
	133	20	30	15	°C/W
	175	20	25	14	°C/W
	207	20	22	13	°C/W
	257	20	15	8	°C/W
Ceramic Quad Flatpack	132	13	55	30	°C/W
	196	13	36	24	°C/W
	256	13	30	18	°C/W
Plastic Quad Flatpack	100	13	51	40	°C/W
	160	10	33	26	°C/W
	208	10	33	26	°C/W
Very Thin Quad Flatpack	100	12	43	35	°C/W
Thin Quad Flatpack	176	11	32	25	°C/W
Power Quad Flatpack	208	0.4	17	13	°C/W
Plastic Leaded Chip Carrier	84	12	37	28	°C/W
Plastic Ball Grid Array	225	10	25	19	°C/W
	313	10	23	17	°C/W

Note: Maximum power dissipation in still air:
PQ160 = 2.4 W
PQ208 = 2.4 W
PQ100 = 1.6 W
VQ100 = 1.9 W
TQ176 = 2.5 W
PL84 = 2.2 W
RQ208 = 4.7 W
BG225 = 3.2 W
BG313 = 3.5 W

Equivalent capacitance is calculated by measuring ICC active at a specified frequency and voltage for each circuit component of interest. Measurements have been made over a range of frequencies at a fixed value of VCC. Equivalent capacitance is frequency independent so that the results may be used over a wide range of operating conditions. Equivalent capacitance values are shown in Figure 2-10.

Table 2-10 • **CEQ Values for Microsemi FPGAs**

Item	CEQ Value
Modules (C_{EQM})	6.7
Input Buffers (C_{EQI})	7.2
Output Buffers (C_{EQO})	10.4
Routed Array Clock Buffer Loads (C_{EQCR})	1.6
Dedicated Clock Buffer Loads (C_{EQCD})	0.7
I/O Clock Buffer Loads (C_{EQCI})	0.9

To calculate the active power dissipated from the complete design, the switching frequency of each part of the logic must be known. EQ 5 shows a piece-wise linear summation over all components.

Power $= VCC^2 * [(m * C_{EQM} * f_m)_{modules} + (n * C_{EQI} * f_n)_{inputs}$

$+ (p * (C_{EQO} + C_L) * fp)_{outputs}$

$+ 0.5 * (q1 * C_{EQCR} * f_{q1})_{routed\_Clk1} + (r1 * fq1)_{routed\_Clk1}$

$+ 0.5 * (q2 * C_{EQCR} * fq2)_{routed\_Clk2}$

$+ (r_2 * f_{q2})_{routed\_Clk2} + 0.5 * (s_1 * C_{EQCD} * f_{s1})_{dedicated\_Clk}$

$+ (s_2 * C_{EQCI} * f_{s2})_{IO\_Clk}]$

EQ 5

Where:

m = Number of logic modules switching at f_m

n = Number of input buffers switching at f_n

p = Number of output buffers switching at f_p

q1 = Number of clock loads on the first routed array clock

q2 = Number of clock loads on the second routed array clock

r_1 = Fixed capacitance due to first routed array clock

r_2 = Fixed capacitance due to second routed array clock

s_1 = Fixed number of clock loads on the dedicated array clock

s_2 = Fixed number of clock loads on the dedicated I/O clock

C_{EQM} = Equivalent capacitance of logic modules in pF

C_{EQI} = Equivalent capacitance of input buffers in pF

C_{EQO} = Equivalent capacitance of output buffers in pF

C_{EQCR} = Equivalent capacitance of routed array clock in pF

C_{EQCD} = Equivalent capacitance of dedicated array clock in pF

C_{EQCI} = Equivalent capacitance of dedicated I/O clock in pF

C_L = Output lead capacitance in pF

f_m = Average logic module switching rate in MHz

f_n = Average input buffer switching rate in MHz

f_p = Average output buffer switching rate in MHz

f_{q1} = Average first routed array clock rate in MHz

f_{q2} = Average second routed array clock rate in MHz

f_{s1} = Average dedicated array clock rate in MHz

f_{s2} = Average dedicated I/O clock rate in MHz

A1440A, A14V40A Timing Characteristics (continued)

Table 2-27 • **A1440A, A14V40A Worst-Case Commercial Conditions, VCC = 4.75 V, T_J = 70°C**

I/O Module Input Propagation Delays		–3 Speed[1]		–2 Speed[1]		–1 Speed		Std. Speed		3.3 V Speed[1]		Units
Parameter/Description		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t_{INY}	Input Data Pad to Y		2.8		3.2		3.6		4.2		5.5	ns
t_{ICKY}	Input Reg IOCLK Pad to Y		4.7		5.3		6.0		7.0		9.2	ns
t_{OCKY}	Output Reg IOCLK Pad to Y		4.7		5.3		6.0		7.0		9.2	ns
t_{ICLRY}	Input Asynchronous Clear to Y		4.7		5.3		6.0		7.0		9.2	ns
t_{OCLRY}	Output Asynchronous Clear to Y		4.7		5.3		6.0		7.0		9.2	ns
Predicted Input Routing Delays[2]												
t_{RD1}	FO = 1 Routing Delay		0.9		1.0		1.1		1.3		1.7	ns
t_{RD2}	FO = 2 Routing Delay		1.2		1.4		1.6		1.8		2.4	ns
t_{RD3}	FO = 3 Routing Delay		1.4		1.6		1.8		2.1		2.8	ns
t_{RD4}	FO = 4 Routing Delay		1.7		1.9		2.2		2.5		3.3	ns
t_{RD8}	FO = 8 Routing Delay		2.8		3.2		3.6		4.2		5.5	ns
I/O Module Sequential Timing (wrt IOCLK pad)												
t_{INH}	Input F-F Data Hold	0.0		0.0		0.0		0.0		0.0		ns
t_{INSU}	Input F-F Data Setup	1.8		1.7		2.0		2.3		2.3		ns
t_{IDEH}	Input Data Enable Hold	0.0		0.0		0.0		0.0		0.0		ns
t_{IDESU}	Input Data Enable Setup	5.8		6.5		7.5		8.6		8.6		ns
t_{OUTH}	Output F-F Data hold	0.7		0.8		0.9		1.0		1.0		ns
t_{OUTSU}	Output F-F Data Setup	0.7		0.8		0.9		1.0		1.0		ns
t_{ODEH}	Output Data Enable Hold	0.3		0.4		0.4		0.5		0.5		ns
f_{ODESU}	Output Data Enable Setup	1.3		1.5		1.7		2.0		2.0		ns

Notes:

1. *The –2 and –3 speed grades have been discontinued. Refer to PDN 0104, PDN 0203, PDN 0604, and PDN 1004 at http://www.microsemi.com/soc/support/notifications/default.aspx#pdn.*

2. *Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual worst-case performance. Post-route timing is based on actual routing delay measurements performed on the device prior to shipment.*

A1460A, A14V60A Timing Characteristics (continued)

Table 2-31 • A1460A, A14V60A Worst-Case Commercial Conditions, VCC = 4.75 V, T_J = 70°C

I/O Module Input Propagation Delays		–3 Speed[1]		–2 Speed[1]		–1 Speed		Std. Speed		3.3 V Speed[1]		Units
Parameter/Description		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t_{INY}	Input Data Pad to Y		2.8		3.2		3.6		4.2		5.5	ns
t_{ICKY}	Input Reg IOCLK Pad to Y		4.7		5.3		6.0		7.0		9.2	ns
t_{OCKY}	Output Reg IOCLK Pad to Y		4.7		5.3		6.0		7.0		9.2	ns
t_{ICLRY}	Input Asynchronous Clear to Y		4.7		5.3		6.0		7.0		9.2	ns
t_{OCLRY}	Output Asynchronous Clear to Y		4.7		5.3		6.0		7.0		9.2	ns
Predicted Input Routing Delays[2]												
t_{RD1}	FO = 1 Routing Delay		0.9		1.0		1.1		1.3		1.7	ns
t_{RD2}	FO = 2 Routing Delay		1.2		1.4		1.6		1.8		2.4	ns
t_{RD3}	FO = 3 Routing Delay		1.4		1.6		1.8		2.1		2.8	ns
t_{RD4}	FO = 4 Routing Delay		1.7		1.9		2.2		2.5		3.3	ns
t_{RD8}	FO = 8 Routing Delay		2.8		3.2		3.6		4.2		5.5	ns
I/O Module Sequential Timing (wrt IOCLK pad)												
t_{INH}	Input F-F Data Hold	0.0		0.0		0.0		0.0		0.0		ns
t_{INSU}	Input F-F Data Setup	1.3		1.5		1.8		2.0		2.0		ns
t_{IDEH}	Input Data Enable Hold	0.0		0.0		0.0		0.0		0.0		ns
t_{IDESU}	Input Data Enable Setup	5.8		6.5		7.5		8.6		8.6		ns
t_{OUTH}	Output F-F Data hold	0.7		0.8		0.9		1.0		1.0		ns
t_{OUTSU}	Output F-F Data Setup	0.7		0.8		0.9		1.0		1.0		ns
t_{ODEH}	Output Data Enable Hold	0.3		0.4		0.4		0.5		0.5		ns
f_{ODESU}	Output Data Enable Setup	1.3		1.5		1.7		2.0		2.0		ns

Notes:

5. *The –2 and –3 speed grades have been discontinued. Refer to PDN 0104, PDN 0203, PDN 0604, and PDN 1004 at http://www.microsemi.com/soc/support/notifications/default.aspx#pdn.*

6. *Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual worst-case performance. Post-route timing is based on actual routing delay measurements performed on the device prior to shipment.*

A1460A, A14V60A Timing Characteristics (continued)

Table 2-32 • **A1460A, A14V60A Worst-Case Commercial Conditions, VCC = 4.75 V, T$_J$ = 70°C**

I/O Module – TTL Output Timing[1]		–3 Speed[2]		–2 Speed[2]		–1 Speed		Std. Speed		3.3 V Speed[1]		Units
Parameter/Description		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t$_{DHS}$	Data to Pad, High Slew		5.0		5.6		6.4		7.5		9.8	ns
t$_{DLS}$	Data to Pad, Low Slew		8.0		9.0		10.2		12.0		15.6	ns
t$_{ENZHS}$	Enable to Pad, Z to H/L, High Slew		4.0		4.5		5.1		6.0		7.8	ns
t$_{ENZLS}$	Enable to Pad, Z to H/L, Low Slew		7.4		8.3		9.4		11.0		14.3	ns
t$_{ENHSZ}$	Enable to Pad, H/L to Z, High Slew		7.8		8.7		9.9		11.6		15.1	ns
t$_{ENLSZ}$	Enable to Pad, H/L to Z, Low Slew		7.4		8.3		9.4		11.0		14.3	ns
t$_{CKHS}$	IOCLK Pad to Pad H/L, High Slew		9.0		9.0		10.0		11.5		15.0	ns
t$_{CKLS}$	IOCLK Pad to Pad H/L, Low Slew		12.8		12.8		15.3		17.0		22.1	ns
d$_{TLHHS}$	Delta Low to High, High Slew		0.02		0.02		0.03		0.03		0.04	ns/pF
d$_{TLHLS}$	Delta Low to High, Low Slew		0.05		0.05		0.06		0.07		0.09	ns/pF
d$_{THLHS}$	Delta High to Low, High Slew		0.04		0.04		0.04		0.05		0.07	ns/pF
d$_{THLLS}$	Delta High to Low, Low Slew		0.05		0.05		0.06		0.07		0.09	ns/pF
I/O Module – CMOS Output Timing[1]												
t$_{DHS}$	Data to Pad, High Slew		6.2		7.0		7.9		9.3		12.1	ns
t$_{DLS}$	Data to Pad, Low Slew		11.7		13.1		14.9		17.5		22.8	ns
t$_{ENZHS}$	Enable to Pad, Z to H/L, High Slew		5.2		5.9		6.6		7.8		10.1	ns
t$_{ENZLS}$	Enable to Pad, Z to H/L, Low Slew		8.9		10.0		11.3		13.3		17.3	ns
t$_{ENHSZ}$	Enable to Pad, H/L to Z, High Slew		7.4		8.3		9.4		11.0		14.3	ns
t$_{ENLSZ}$	Enable to Pad, H/L to Z, Low Slew		7.4		8.3		9.4		11.0		14.3	ns
t$_{CKHS}$	IOCLK Pad to Pad H/L, High Slew		10.4		10.4		12.1		13.8		17.9	ns
t$_{CKLS}$	IOCLK Pad to Pad H/L, Low Slew		14.5		14.5		17.4		19.3		25.1	ns
d$_{TLHHS}$	Delta Low to High, High Slew		0.04		0.04		0.05		0.06		0.08	ns/pF
d$_{TLHLS}$	Delta Low to High, Low Slew		0.07		0.08		0.09		0.11		0.14	ns/pF
d$_{THLHS}$	Delta High to Low, High Slew		0.03		0.03		0.03		0.04		0.05	ns/pF
d$_{THLLS}$	Delta High to Low, Low Slew		0.04		0.04		0.04		0.05		0.07	ns/pF

Notes:

1. *Delays based on 35 pF loading.*
2. *The –2 and –3 speed grades have been discontinued. Refer to PDN 0104, PDN 0203, PDN 0604, and PDN 1004 at http://www.microsemi.com/soc/support/notifications/default.aspx#pdn.*

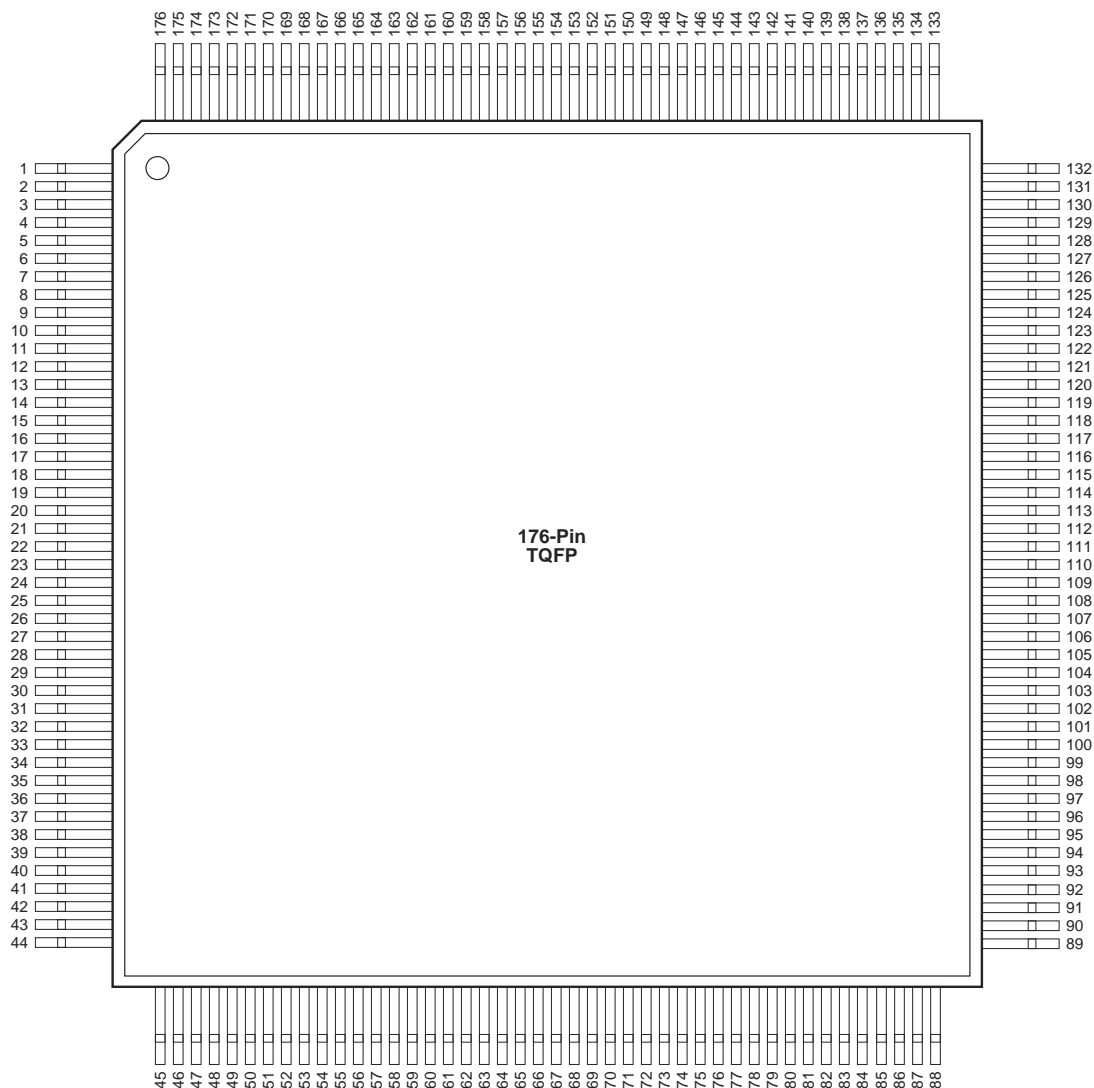### *A14100A, A14V100A Timing Characteristics (continued)*

Table 2-36 • **A14100A, A14V100A Worst-Case Commercial Conditions, VCC = 4.75 V, T$_J$ = 70°C**

I/O Module – TTL Output Timing[1]		–3 Speed[2]		–2 Speed[2]		–1 Speed		Std. Speed		3.3 V Speed[1]		Units
Parameter/Description		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t$_{DHS}$	Data to Pad, High Slew		5.0		5.6		6.4		7.5		9.8	ns
t$_{DLS}$	Data to Pad, Low Slew		8.0		9.0		10.2		12.0		15.6	ns
t$_{ENZHS}$	Enable to Pad, Z to H/L, High Slew		4.0		4.5		5.1		6.0		7.8	ns
t$_{ENZLS}$	Enable to Pad, Z to H/L, Low Slew		7.4		8.3		9.4		11.0		14.3	ns
t$_{ENHSZ}$	Enable to Pad, H/L to Z, High Slew		8.0		9.0		10.2		12.0		15.6	ns
t$_{ENLSZ}$	Enable to Pad, H/L to Z, Low Slew		7.4		8.3		9.4		11.0		14.3	ns
t$_{CKHS}$	IOCLK Pad to Pad H/L, High Slew		9.5		9.5		10.5		12.0		15.6	ns
t$_{CKLS}$	IOCLK Pad to Pad H/L, Low Slew		12.8		12.8		15.3		17.0		22.1	ns
d$_{TLHHS}$	Delta Low to High, High Slew		0.02		0.02		0.03		0.03		0.04	ns/pF
d$_{TLHLS}$	Delta Low to High, Low Slew		0.05		0.05		0.06		0.07		0.09	ns/pF
d$_{THLHS}$	Delta High to Low, High Slew		0.04		0.04		0.04		0.05		0.07	ns/pF
d$_{THLLS}$	Delta High to Low, Low Slew		0.05		0.05		0.06		0.07		0.09	ns/pF
I/O Module – CMOS Output Timing[1]												
t$_{DHS}$	Data to Pad, High Slew		6.2		7.0		7.9		9.3		12.1	ns
t$_{DLS}$	Data to Pad, Low Slew		11.7		13.1		14.9		17.5		22.8	ns
t$_{ENZHS}$	Enable to Pad, Z to H/L, High Slew		5.2		5.9		6.6		7.8		10.1	ns
t$_{ENZLS}$	Enable to Pad, Z to H/L, Low Slew		8.9		10.0		11.3		13.3		17.3	ns
t$_{ENHSZ}$	Enable to Pad, H/L to Z, High Slew		8.0		9.0		10.0		12.0		15.6	ns
t$_{ENLSZ}$	Enable to Pad, H/L to Z, Low Slew		7.4		8.3		9.4		11.0		14.3	ns
t$_{CKHS}$	IOCLK Pad to Pad H/L, High Slew		10.4		10.4		12.4		13.8		17.9	ns
t$_{CKLS}$	IOCLK Pad to Pad H/L, Low Slew		14.5		14.5		17.4		19.3		25.1	ns
d$_{TLHHS}$	Delta Low to High, High Slew		0.04		0.04		0.05		0.06		0.08	ns/pF
d$_{TLHLS}$	Delta Low to High, Low Slew		0.07		0.08		0.09		0.11		0.14	ns/pF
d$_{THLHS}$	Delta High to Low, High Slew		0.03		0.03		0.03		0.04		0.05	ns/pF
d$_{THLLS}$	Delta High to Low, Low Slew		0.04		0.04		0.04		0.05		0.07	ns/pF

Notes: *

1. Delays based on 35 pF loading.

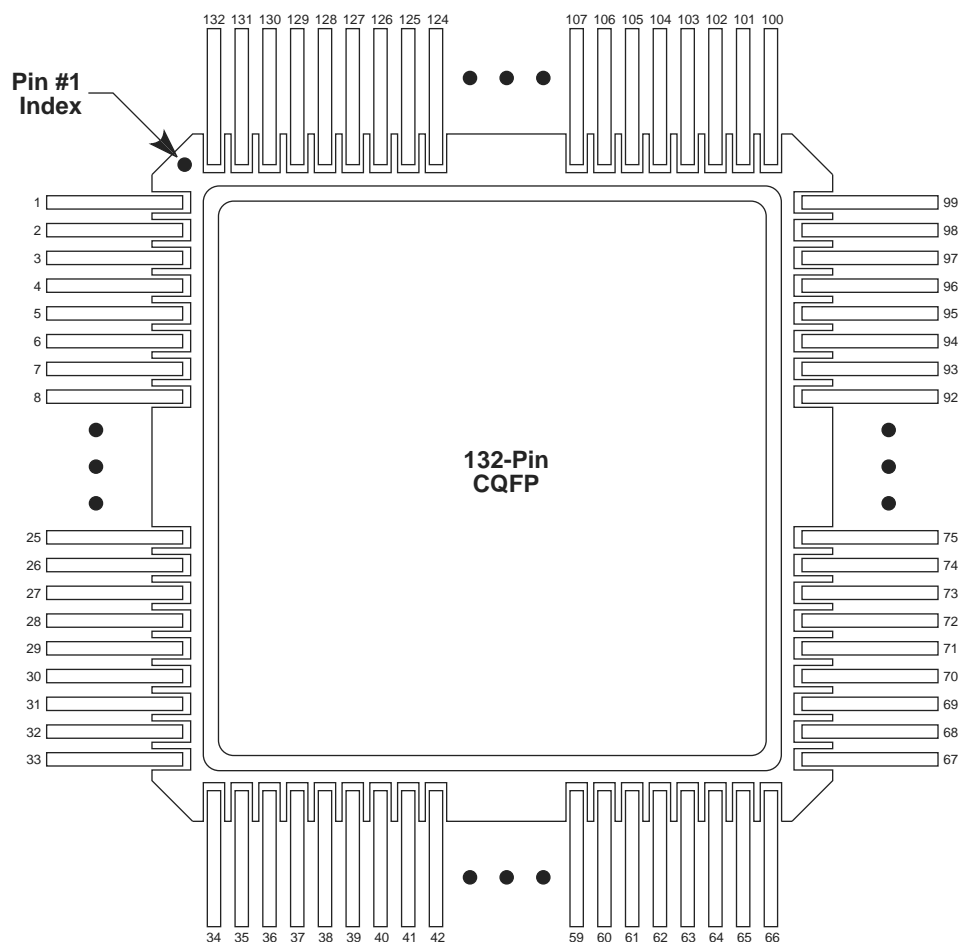*2. The –2 and –3 speed grades have been discontinued. Refer to PDN 0104, PDN 0203, PDN 0604, and PDN 1004 at http://www.microsemi.com/soc/support/notifications/default.aspx#pdn.*

TQ176

Note: This is the top view.

Note

For Package Manufacturing and Environmental information, visit the Resource Center at
http://www.microsemi.com/soc/products/solutions/package/docs.aspx

CQ132

Note: This is the top view

Note

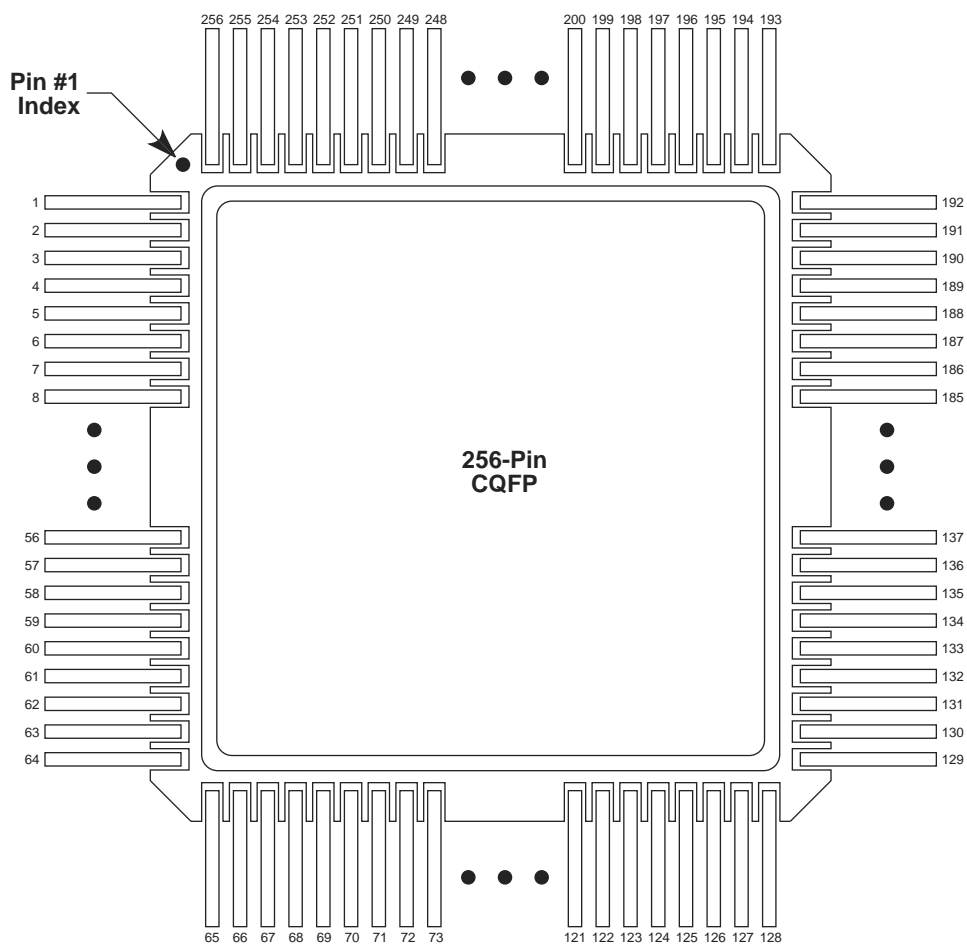For Package Manufacturing and Environmental information, visit the Resource Center at
http://www.microsemi.com/soc/products/solutions/package/docs.aspx

CQ196		CQ196	
Pin Number	**A1460 Function**	**Pin Number**	**A1460 Function**
1	GND	101	GND
2	SDI, I/O	110	VCC
11	MODE	111	VCC
12	VCC	112	GND
13	GND	137	VCC
37	GND	138	GND
38	VCC	139	GND
39	VCC	140	VCC
51	GND	148	IOCLK, I/O
52	GND	149	GND
59	VCC	155	VCC
64	GND	162	GND
77	HCLK, I/O	172	CLKA, I/O
79	PRB, I/O	173	CLKB, I/O
86	GND	174	PRA, I/O
94	VCC	183	GND
98	GND	189	VCC
99	SDO	193	GND
100	IOPCL, I/O	196	DCLK, I/O

Notes:

1. All unlisted pin numbers are user I/Os.
2. NC denotes no connection.
3. MODE should be terminated to GND through a 10K resistor to enable Actionprobe usage; otherwise it can be terminated directly to GND.

CQ256

Pin #1 Index

256-Pin CQFP

Note: This is the top view.

Note

For Package Manufacturing and Environmental information, visit the Resource Center at
http://www.microsemi.com/soc/products/solutions/package/docs.aspx

CQ256		CQ256	
Pin Number	**A14100 Function**	**Pin Number**	**A14100 Function**
1	GND	141	VCC
2	SDI, I/O	158	GND
11	MODE	159	VCC
28	VCC	160	GND
29	GND	161	VCC
30	VCC	174	VCC
31	GND	175	GND
46	VCC	176	GND
59	GND	188	IOCLK, I/O
90	PRB, I/O	189	GND
91	GND	219	CLKA, I/O
92	VCC	220	CLKB, I/O
93	GND	221	VCC
94	VCC	222	GND
96	HCLK, I/O	223	VCC
110	GND	224	GND
126	SDO	225	PRA, I/O
127	IOPCL, I/O	240	GND
128	GND	256	DCLK, I/O

Notes:

1. All unlisted pin numbers are user I/Os.
2. NC denotes no connection.
3. MODE should be terminated to GND through a 10K resistor to enable Actionprobe usage; otherwise it can be terminated directly to GND.

PG100	
A1415 Function	**Location**
CLKA or I/O	C7
CLKB or I/O	D6
DCLK or I/O	C4
GND	C3, C6, C9, E9, F3, F9, J3, J6, J8, J9
HCLK or I/O	H6
IOCLK or I/O	C10
IOPCL or I/O	K9
MODE	C2
PRA or I/O	A6
PRB or I/O	L3
SDI or I/O	B3
SDO	L9
VCC	B6, B10, E11, F2, F10, G2, K2, K6, K10

Notes:

1. All unlisted pin numbers are user I/Os.
2. NC denotes no connection.
3. MODE should be terminated to GND through a 10K resistor to enable Actionprobe usage; otherwise it can be terminated directly to GND.
4. The PG100 package has been discontinued.

PG175	
A1440 Function	**Location**
CLKA or I/O	C9
CLKB or I/O	A9
DCLK or I/O	D5
GND	D4, D8, D11, D12, E4, E14, H4, H12, L4, L12, M4, M8, M12
HCLK or I/O	R8
IOCLK or I/O	E12
IOPCL or I/O	P13
MODE	F3
NC	A1, A2, A15, B2, B3, P2, P14, R1, R2, R14, R15
PRA or I/O	B8
PRB or I/O	R7
SDI or I/O	D3
SDO	N12
VCC	C3, C8, C13, E15, H3, H13, L1, L14, N3, N8, N13

Notes:

1. All unlisted pin numbers are user I/Os.
2. NC denotes no connection.
3. MODE should be terminated to GND through a 10K resistor to enable Actionprobe usage; otherwise it can be terminated directly to GND.
4. The PG175 package has been discontinued.

PG257	
A14100 Function	**Location**
CLKA or I/O	L4
CLKB or I/O	L5
DCLK or I/O	E4
GND	B16, C4, D4, D10, D16, E11, J5, K4, K16, L15, R4, T4, T10, T16, T17, X7
HCLK or I/O	J16
IOCLK or I/O	T5
IOPCL or I/O	R16
MODE	A5
NC	E5
PRA or I/O	J1
PRB or I/O	J17
SDI or I/O	B4
SDO	R17
VCC	C3, C10, C13, C17, K3, K17, V3, V7, V10, V17, X14

Notes:

1. All unlisted pin numbers are user I/Os.
2. NC denotes no connection.
3. MODE should be terminated to GND through a 10K resistor to enable Actionprobe usage; otherwise it can be terminated directly to GND.

4 – Datasheet Information

List of Changes

The following table lists critical changes that were made in each version of the datasheet.

Revision	Changes	Page
Revision 3 (January 2012)	The description for SDO pins had earlier been removed from the datasheet and has now been included again, in the "Pin Descriptions" section (SAR 35820).	2-21
	SDO pin numbers had earlier been removed from package pin assignment tables in the datasheet, and have now been restored to the pin tables (SAR 35820).	3-1
Revision 2 (September 2011)	The ACT 3 datasheet was formatted newly in the style used for current datasheets. The same information is present (other than noted in the list of changes for this revision) but divided into chapters.	N/A
	The datasheet was revised to note in multiple places that speed grades −2 and −3 have been discontinued. The following device/package combinations have been discontinued for all speed grades and temperatures (SAR 33872): A1415 PG100 A1425 PG133 A1440 PG175 A1460 BG225 Refer to PDN 0104, PDN 0203, PDN 0604, and PDN 1004.	I and others
	The "Features" section was revised to state the clock-to-ouput time and on-chip performance for −1 speed grade as 9.0 ns and 186 MHz. The "General Description" section was revised in accordance (SAR 33872).	I
	The maximum performance values were updated in Table 1 • ACT 3 Family Product Information, and now reflect worst-case commercial for the −1 speed grade (SAR 33872).	I
	The "Product Plan" table was updated as follows to conform to current offerings (SAR 33872): The A1415A device is offered in PL84, PG100, and VQ100 packages for Military application. The A1440A device is offered in TQ176 and VQ100 packages for Industrial application.	III
	Table 1-1 • Chip-to-Chip Performance (worst-case commercial) was updated to include data for all speed grades instead of only −3 (SAR 33872).	1-2
	Figure 1-1 • Predictable Performance (worst-case commercial, −1 speed grade) was revised to reflect values for the −1 speed grade (SAR 33872).	1-1
	Figure 2-10 • Timing Model was updated to show data for the −1 speed grade instead of −3 (SAR 33872).	2-16
	Table 2-14 • Logic Module and Routing Delay by Fanout (ns); Worst-Case Commercial Conditions was updated to include data for all speed grades instead of only −3 (SAR 33872).	2-20
	Package names used in the "Package Pin Assignments" section and throughout the document were revised to match standards given in *Package Mechanical Drawings* (SAR 27395).	3-1

Datasheet Categories

Categories

In order to provide the latest information to designers, some datasheet parameters are published before data has been fully characterized from silicon devices. The data provided for a given device is designated as either "Product Brief," "Advance," "Preliminary," or "Production." The definitions of these categories are as follows:

Product Brief

The product brief is a summarized version of a datasheet (advance or production) and contains general product information. This document gives an overview of specific device and family information.

Advance

This version contains initial estimated information based on simulation, other products, devices, or speed grades. This information can be used as estimates, but not for production. This label only applies to the DC and Switching Characteristics chapter of the datasheet and will only be used when the data has not been fully characterized.

Preliminary

The datasheet contains information based on simulation and/or initial characterization. The information is believed to be correct, but changes are possible.

Production

This version contains information that is considered to be final.

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