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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Obsolete
Number of LABs/CLBs	200
Number of Logic Elements/Cells	-
Total RAM Bits	-
Number of I/O	80
Number of Gates	1500
Voltage - Supply	4.5V ~ 5.5V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 85°C (TA)
Package / Case	100-TQFP
Supplier Device Package	100-VQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/microsemi/a1415a-1vq100i

2 – Detailed Specifications

This section of the datasheet is meant to familiarize the user with the architecture of the ACT 3 family of FPGA devices. A generic description of the family will be presented first, followed by a detailed description of the logic blocks, the routing structure, the antifuses, and the special function circuits. The on-chip circuitry required to program the devices is not covered.

Topology

The ACT 3 family architecture is composed of six key elements: Logic modules, I/O modules, I/O Pad Drivers, Routing Tracks, Clock Networks, and Programming and Test Circuits. The basic structure is similar for all devices in the family, differing only in the number of rows, columns, and I/Os. The array itself consists of alternating rows of modules and channels. The logic modules and channels are in the center of the array; the I/O modules are located along the array periphery. A simplified floor plan is depicted in Figure 2-1.

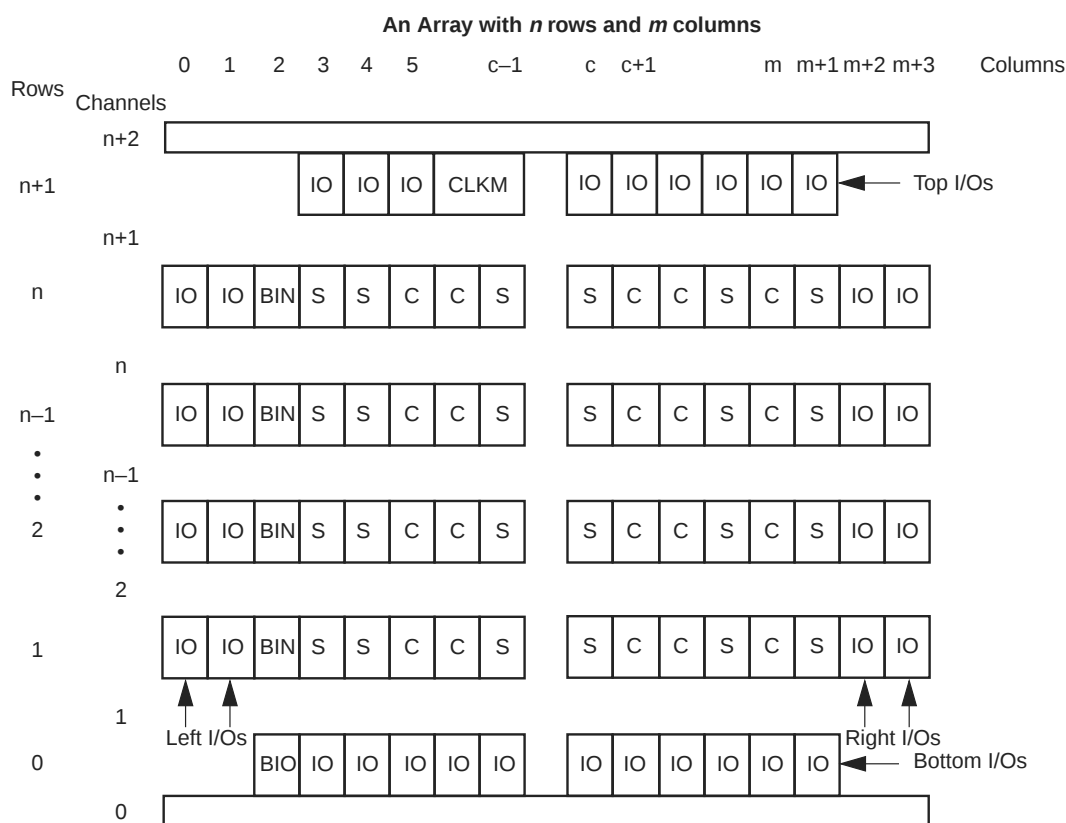


Figure 2-1 • Generalized Floor Plan of ACT 3 Device

Power Dissipation

$$P = [ICC_{\text{standby}} + I_{\text{active}}] * VCC * IOL * VOL * N + IOH * (VCC - VOH) * M$$

EQ 3

where:

ICC standby is the current flowing when no inputs or outputs are changing

Iactive is the current flowing due to CMOS switching.

IOL and IOH are TTL sink/source current.

VOL and VOH are TTL level output voltages.

N is the number of outputs driving TTL loads to VOL.

M equals the number of outputs driving TTL loads to VOH.

An accurate determination of N and M is problematical because their values depend on the design and on the system I/O. The power can be divided into two components: static and active.

Static Power Component

Microsemi FPGAs have small static power components that result in lower power dissipation than PALs or PLDs. By integrating multiple PALs/PLDs into one FPGA, an even greater reduction in board-level power dissipation can be achieved.

The power due to standby current is typically a small component of the overall power. Standby power is calculated in Table 2-9 for commercial, worst case conditions.

Table 2-9 • Standby Power Calculation

ICC	VCC	Power
2 mA	5.25 V	10.5 mW

The static power dissipated by TTL loads depends on the number of outputs driving high or low and the DC load current. Again, this value is typically small. For instance, a 32-bit bus sinking 4 mA at 0.33 V will generate 42 mW with all outputs driving low, and 140 mW with all outputs driving high. The actual dissipation will average somewhere between as I/Os switch states with time.

Active Power Component

Power dissipation in CMOS devices is usually dominated by the active (dynamic) power dissipation. This component is frequency dependent, a function of the logic and the external I/O. Active power dissipation results from charging internal chip capacitances of the interconnect, unprogrammed antifuses, module inputs, and module outputs, plus external capacitance due to PC board traces and load device inputs.

An additional component of the active power dissipation is the totem-pole current in CMOS transistor pairs. The net effect can be associated with an equivalent capacitance that can be combined with frequency and voltage to represent active power dissipation.

Equivalent Capacitance

The power dissipated by a CMOS circuit can be expressed by EQ 4.

$$\text{Power } (\mu\text{W}) = C_{\text{EQ}} * VCC^2 * F$$

EQ 4

Where:

C_{EQ} is the equivalent capacitance expressed in pF.

VCC is the power supply in volts.

F is the switching frequency in MHz.

Table 2-11 • Fixed Capacitance Values for Microsemi FPGAs

Device Type	r1, routed_Clk1	r2, routed_Clk2
A1415A	60	60
A14V15A	57	57
A1425A	75	75
A14V25A	72	72
A1440A	105	105
A14V40A	100	100
A1440B	105	105
A1460A	165	165
A14V60A	157	157
A1460B	165	165
A14100A	195	195
A14V100A	185	185
A14100B	195	195

Table 2-12 • Fixed Clock Loads (s1/s2)

Device Type	s1, Clock Loads on Dedicated Array Clock	s2, Clock Loads on Dedicated I/O Clock
A1415A	104	80
A14V15A	104	80
A1425A	160	100
A14V25A	160	100
A1440A	288	140
A14V40A	288	140
A1440B	288	140
A1460A	432	168
A14V60A	432	168
A1460B	432	168
A14100A	697	228
A14V100A	697	228
A14100B	697	228

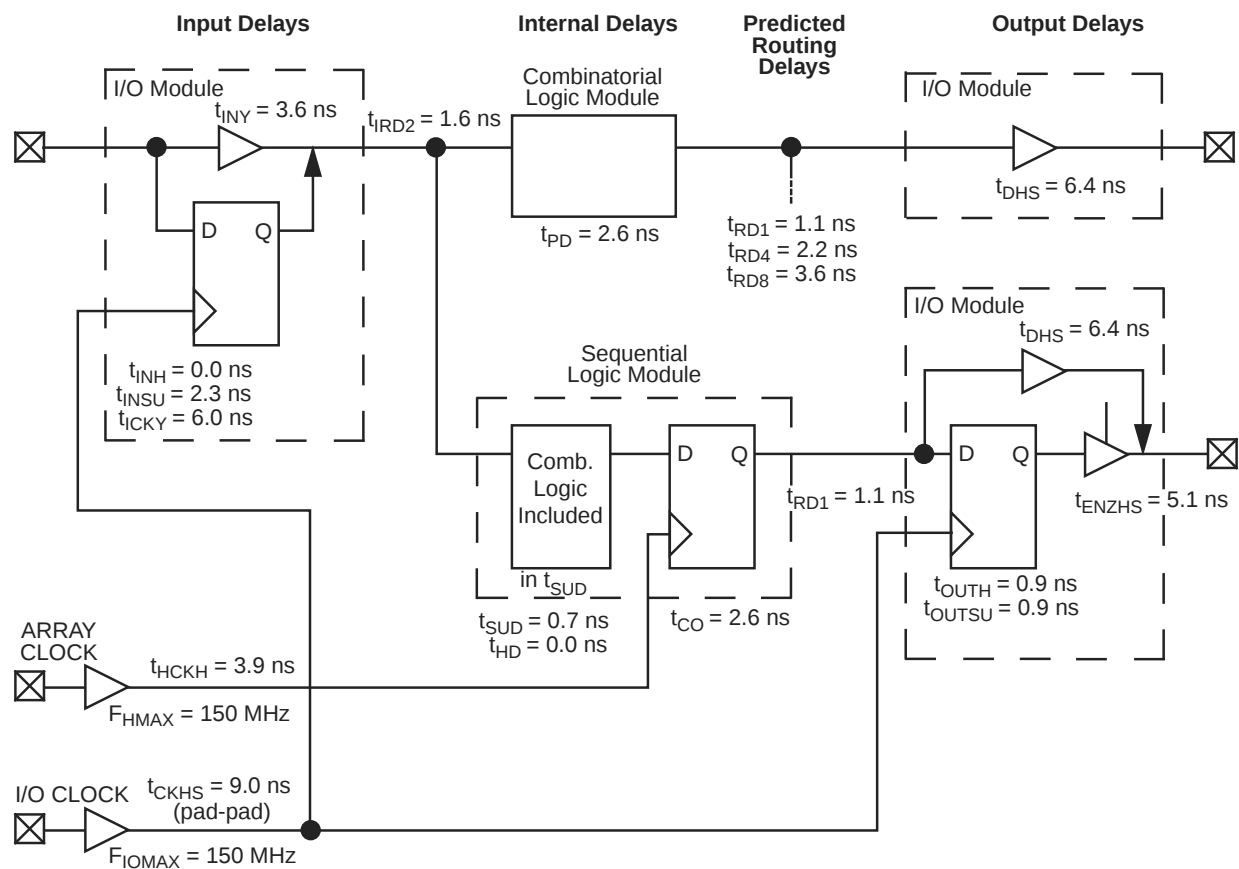
Determining Average Switching Frequency

To determine the switching frequency for a design, you must have a detailed understanding of the data input values to the circuit. The following guidelines are meant to represent worst-case scenarios so that they can be generally used to predict the upper limits of power dissipation. These guidelines are as follows:

Table 2-13 • Guidelines for Predicting Power Dissipation

Data	Value
Logic Modules (m)	80% of modules
Inputs switching (n)	# inputs/4
Outputs switching (p)	# output/4
First routed array clock loads (q1)	40% of sequential modules
Second routed array clock loads (q2)	40% of sequential modules
Load capacitance (CL)	35 pF
Average logic module switching rate (fm)	F/10
Average input switching rate (fn)	F/5
Average output switching rate (fp)	F/10
Average first routed array clock rate (fq1)	F/2
Average second routed array clock rate (fq2)	F/2
Average dedicated array clock rate (fs1)	F
Average dedicated I/O clock rate (fs2)	F

ACT 3 Timing Model



Note: Values shown for A1425A -1 speed grade device.

Figure 2-10 • Timing Model

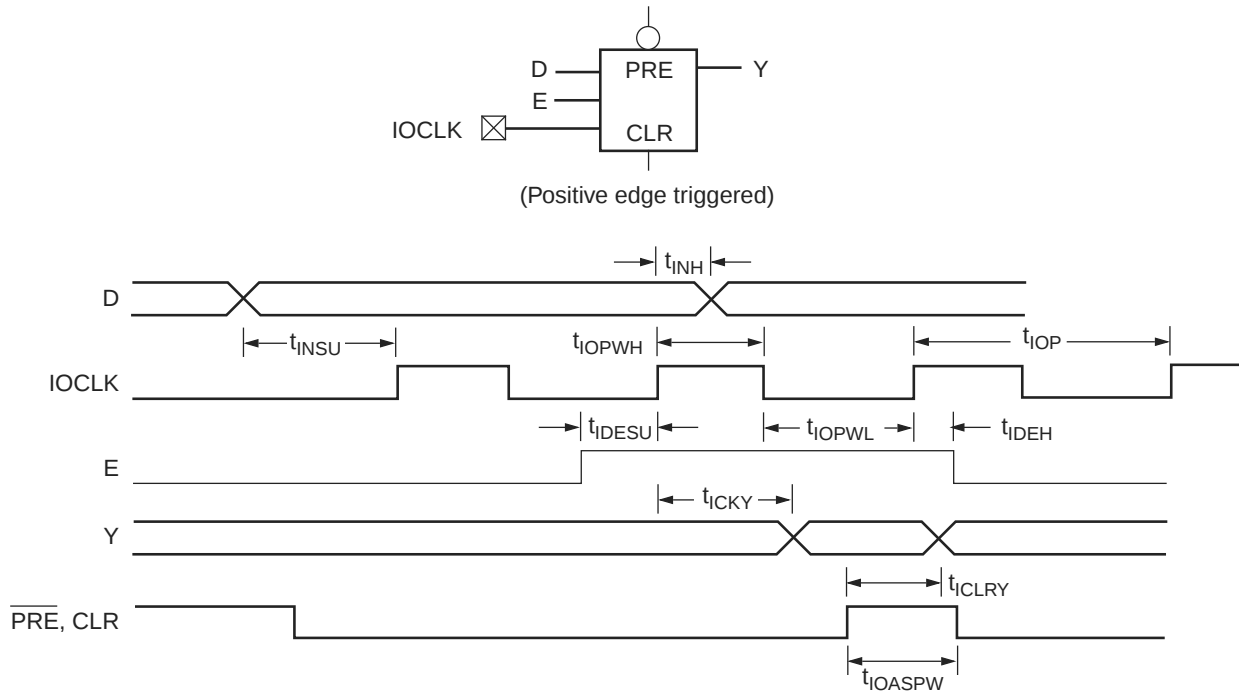


Figure 2-16 • I/O Module: Sequential Input Timing Characteristics

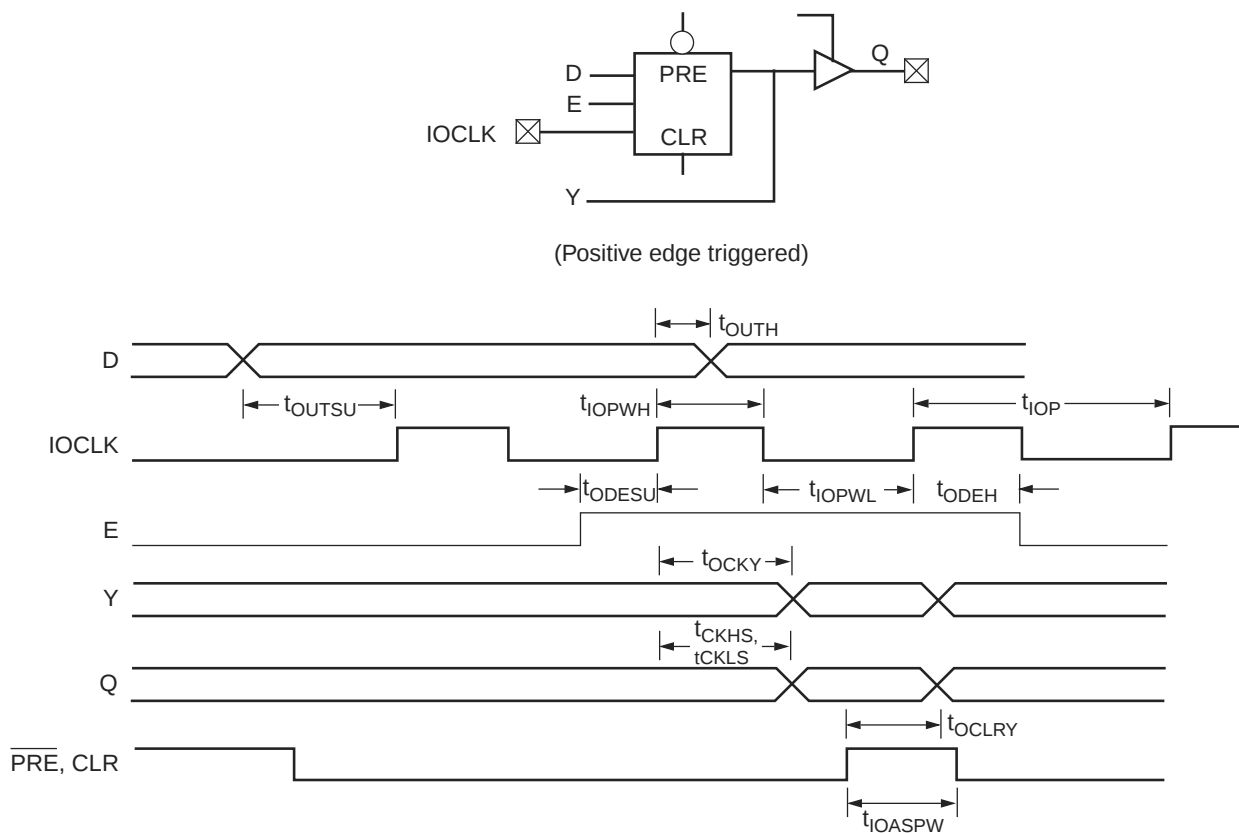


Figure 2-17 • I/O Module: Sequential Output Timing Characteristics

Timing Derating

ACT 3 devices are manufactured in a CMOS process. Therefore, device performance varies according to temperature, voltage, and process variations. Minimum timing parameters reflect maximum operating voltage, minimum operating temperature, and best-case processing. Maximum timing parameters reflect minimum operating voltage, maximum operating temperature, and worst-case processing.

Table 2-15 • Timing Derating Factor (Temperature and Voltage)

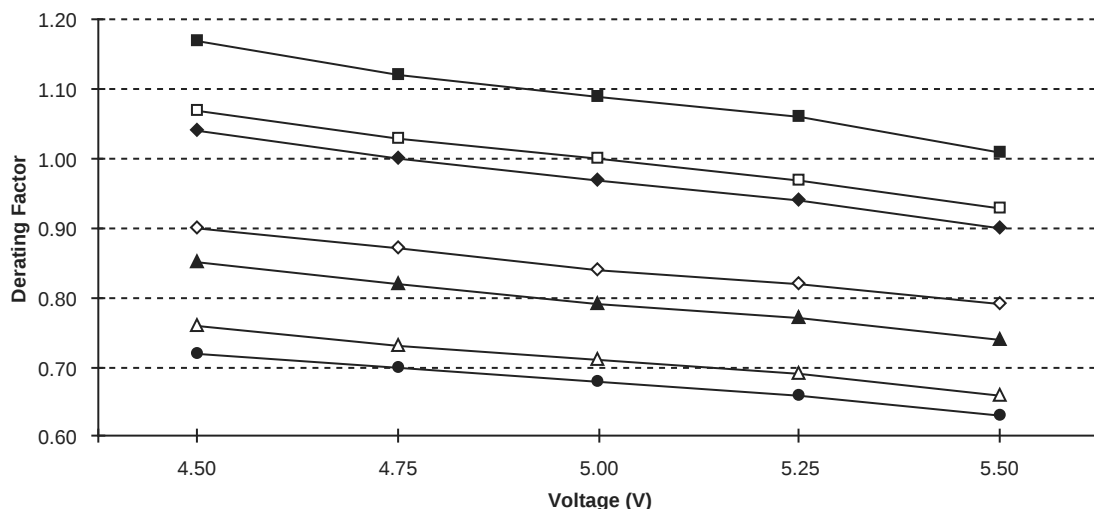
(Commercial Minimum/Maximum Specification) x	Industrial		Military	
	Min.	Max.	Min.	Max.
	0.66	1.07	0.63	1.17

Table 2-16 • Timing Derating Factor for Designs at Typical Temperature ($T_J = 25^\circ\text{C}$) and Voltage (5.0 V)

(Commercial Maximum Specification) x	0.85
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Table 2-17 • Temperature and Voltage Derating Factors (normalized to Worst-Case Commercial, $T_J = 4.75\text{ V}$, 70°C)

	-55	-40	0	25	70	85	125
4.50	0.72	0.76	0.85	0.90	1.04	1.07	1.117
4.75	0.70	0.73	0.82	0.87	1.00	1.03	1.12
5.00	0.68	0.71	0.79	0.84	0.97	1.00	1.09
5.25	0.66	0.69	0.77	0.82	0.94	0.97	1.06
5.50	0.63	0.66	0.74	0.79	0.90	0.93	1.01



Note: This derating factor applies to all routing and propagation delays.

Figure 2-18 • Junction Temperature and Voltage Derating Curves (normalized to Worst-Case Commercial, $T_J = 4.75\text{ V}$, 70°C)

A1415A, A14V15A Timing Characteristics

Table 2-18 • A1415A, A14V15A Worst-Case Commercial Conditions, VCC = 4.75 V, T_J = 70°C¹

Logic Module Propagation Delays ²		-3 Speed ³		-2 Speed ³		-1 Speed		Std. Speed		3.3 V Speed ¹		Units
Parameter/Description		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t _{PD}	Internal Array Module		2.0		2.3		2.6		3.0		3.9	ns
t _{CO}	Sequential Clock to Q		2.0		2.3		2.6		3.0		3.9	ns
t _{CLR}	Asynchronous Clear to Q		2.0		2.3		2.6		3.0		3.9	ns
Predicted Routing Delays⁴												
t _{RD1}	FO = 1 Routing Delay		0.9		1.0		1.1		1.3		1.7	ns
t _{RD2}	FO = 2 Routing Delay		1.2		1.4		1.6		1.8		2.4	ns
t _{RD3}	FO = 3 Routing Delay		1.4		1.6		1.8		2.1		2.8	ns
t _{RD4}	FO = 4 Routing Delay		1.7		1.9		2.2		2.5		3.3	ns
t _{RD8}	FO = 8 Routing Delay		2.8		3.2		3.6		4.2		5.5	ns
Logic Module Sequential Timing												
t _{SUD}	Flip-Flop Data Input Setup	0.5		0.6		0.7		0.8		0.8		ns
t _{HD}	Flip-Flop Data Input Hold	0.0		0.0		0.0		0.0		0.0		ns
t _{SUD}	Latch Data Input Setup	0.5		0.6		0.7		0.8		0.8		ns
t _{HD}	Latch Data Input Hold	0.0		0.0		0.0		0.0		0.0		ns
t _{WASYN}	Asynchronous Pulse Width	1.9		2.4		3.2		3.8		4.8		ns
t _{WCLKA}	Flip-Flop Clock Pulse Width	1.9		2.4		3.2		3.8		4.8		ns
t _A	Flip-Flop Clock Input Period	4.0		5.0		6.8		8.0		10.0		ns
f _{MAX}	Flip-Flop Clock Frequency		250		200		150		125		100	MHz

Notes:

- VCC = 3.0 V for 3.3 V specifications.
- For dual-module macros, use t_{PD} + t_{RD1} + t_{PDn} + t_{CO} + t_{RD1} + t_{PDn} or t_{PD1} + t_{RD1} + t_{SUD}, whichever is appropriate.
- The -2 and -3 speed grades have been discontinued. Please refer to the Product Discontinuation Notices (PDNs) listed below:
PDN March 2001
PDN 0104
PDN 0203
PDN 0604
PDN 1004
- Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual worst-case performance. Post-route timing is based on actual routing delay measurements performed on the device prior to shipment.

A1425A, A14V25A Timing Characteristics

Table 2-22 • A1425A, A14V25A Worst-Case Commercial Conditions, VCC = 4.75 V, T_J = 70°C¹

Logic Module Propagation Delays ²		–3 Speed ³		–2 Speed ³		–1 Speed		Std. Speed		3.3 V Speed ¹		Units
Parameter/Description		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t _{PD}	Internal Array Module		2.0		2.3		2.6		3.0		3.9	ns
t _{CO}	Sequential Clock to Q		2.0		2.3		2.6		3.0		3.9	ns
t _{CLR}	Asynchronous Clear to Q		2.0		2.3		2.6		3.0		3.9	ns
Predicted Routing Delays⁴												
t _{RD1}	FO = 1 Routing Delay		0.9		1.0		1.1		1.3		1.7	ns
t _{RD2}	FO = 2 Routing Delay		1.2		1.4		1.6		1.8		2.4	ns
t _{RD3}	FO = 3 Routing Delay		1.4		1.6		1.8		2.1		2.8	ns
t _{RD4}	FO = 4 Routing Delay		1.7		1.9		2.2		2.5		3.3	ns
t _{RD8}	FO = 8 Routing Delay		2.8		3.2		3.6		4.2		5.5	ns
Logic Module Sequential Timing												
t _{SUD}	Flip-Flop Data Input Setup	0.5		0.6		0.7		0.8		0.8		ns
t _{HD}	Flip-Flop Data Input Hold	0.0		0.0		0.0		0.0		0.0		ns
t _{SUD}	Latch Data Input Setup	0.5		0.6		0.7		0.8		0.8		ns
t _{HD}	Latch Data Input Hold	0.0		0.0		0.0		0.0		0.0		ns
t _{WASYN}	Asynchronous Pulse Width	1.9		2.4		3.2		3.8		4.8		ns
t _{WCLKA}	Flip-Flop Clock Pulse Width	1.9		2.4		3.2		3.8		4.8		ns
t _A	Flip-Flop Clock Input Period	4.0		5.0		6.8		8.0		10.0		ns
f _{MAX}	Flip-Flop Clock Frequency		250		200		150		125		100	MHz

Notes:

1. VCC = 3.0 V for 3.3 V specifications.
2. For dual-module macros, use t_{PD} + t_{RD1} + t_{PDn} + t_{CO} + t_{RD1} + t_{PDn} or t_{PD1} + t_{RD1} + t_{SUD}, whichever is appropriate.
3. The –2 and –3 speed grades have been discontinued. Refer to PDN 0104, PDN 0203, PDN 0604, and PDN 1004 at <http://www.microsemi.com/soc/support/notifications/default.aspx#pdn>.
4. Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual worst-case performance. Post-route timing is based on actual routing delay measurements performed on the device prior to shipment.

A14100A, A14V100A Timing Characteristics (continued)

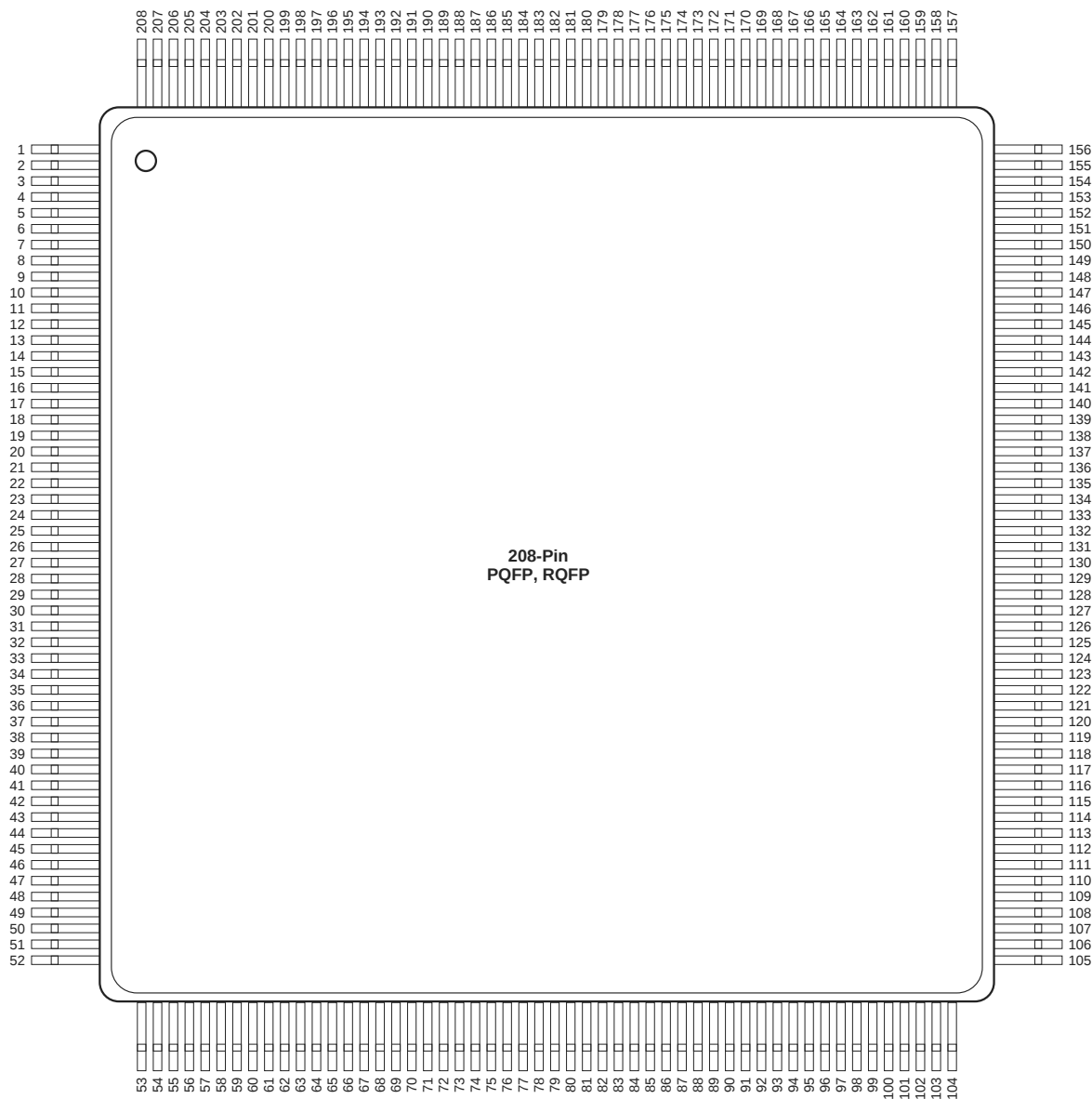
Table 2-35 • A14100A, A14V100A Worst-Case Commercial Conditions, VCC = 4.75 V, T_J = 70°C

I/O Module Input Propagation Delays		–3 Speed ¹		–2 Speed ¹		–1 Speed		Std. Speed		3.3 V Speed ¹		Units
Parameter/Description		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t _{INY}	Input Data Pad to Y		2.8		3.2		3.6		4.2		5.5	ns
t _{ICKY}	Input Reg IOCLK Pad to Y		4.7		5.3		6.0		7.0		9.2	ns
t _{OCKY}	Output Reg IOCLK Pad to Y		4.7		5.3		6.0		7.0		9.2	ns
t _{ICLRY}	Input Asynchronous Clear to Y		4.7		5.3		6.0		7.0		9.2	ns
t _{OCLRY}	Output Asynchronous Clear to Y		4.7		5.3		6.0		7.0		9.2	ns
Predicted Input Routing Delays²												
t _{RD1}	FO = 1 Routing Delay		0.9		1.0		1.1		1.3		1.7	ns
t _{RD2}	FO = 2 Routing Delay		1.2		1.4		1.6		1.8		2.4	ns
t _{RD3}	FO = 3 Routing Delay		1.4		1.6		1.8		2.1		2.8	ns
t _{RD4}	FO = 4 Routing Delay		1.7		1.9		2.2		2.5		3.3	ns
t _{RD8}	FO = 8 Routing Delay		2.8		3.2		3.6		4.2		5.5	ns
I/O Module Sequential Timing (wrt IOCLK pad)												
t _{INH}	Input F-F Data Hold	0.0		0.0		0.0		0.0		0.0		ns
t _{INSU}	Input F-F Data Setup	1.2		1.4		1.5		1.8		1.8		ns
t _{IDEH}	Input Data Enable Hold	0.0		0.0		0.0		0.0		0.0		ns
t _{IDESU}	Input Data Enable Setup	5.8		6.5		7.5		8.6		8.6		ns
t _{OUTH}	Output F-F Data hold	0.7		0.8		1.0		1.0		1.0		ns
t _{OUTSU}	Output F-F Data Setup	0.7		0.8		1.0		1.0		1.0		ns
t _{ODEH}	Output Data Enable Hold	0.3		0.4		0.5		0.5		0.5		ns
f _{ODESU}	Output Data Enable Setup	1.3		1.5		2.0		2.0		2.0		ns

Notes: *

1. The –2 and –3 speed grades have been discontinued. Refer to PDN 0104, PDN 0203, PDN 0604, and PDN 1004 at <http://www.microsemi.com/soc/support/notifications/default.aspx#pdn>.
2. Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual worst-case performance. Post-route timing is based on actual routing delay measurements performed on the device prior to shipment.

PQ208, RQ208



Note: This is the top view of the package

Note

For Package Manufacturing and Environmental information, visit the Resource Center at <http://www.microsemi.com/soc/products/solutions/package/docs.aspx>

PQ208, RQ208		
Pin Number	A1460, A14V60 Function	A14100, A14V100 Function
1	GND	GND
2	SDI, I/O	SDI, I/O
11	MODE	MODE
12	VCC	VCC
25	VCC	VCC
26	GND	GND
27	VCC	VCC
28	GND	GND
40	VCC	VCC
41	VCC	VCC
52	GND	GND
53	NC	I/O
60	VCC	VCC
65	NC	I/O
76	PRB, I/O	PRB, I/O
77	GND	GND
78	VCC	VCC
79	GND	GND
80	VCC	VCC
82	HCLK, I/O	HCLK, I/O
98	VCC	VCC
102	NC	I/O
103	SDO	SDO
104	IOPCL, I/O	IOPCL, I/O
105	GND	GND
114	VCC	VCC

PQ208, RQ208		
Pin Number	A1460, A14V60 Function	A14100, A14V100 Function
115	VCC	VCC
116	NC	I/O
129	GND	GND
130	VCC	VCC
131	GND	GND
132	VCC	VCC
145	VCC	VCC
146	GND	GND
147	NC	I/O
148	VCC	VCC
156	IOCLK, I/O	IOCLK, I/O
157	GND	GND
158	NC	I/O
164	VCC	VCC
180	CLKA, I/O	CLKA, I/O
181	CLKB, I/O	CLKB, I/O
182	VCC	VCC
183	GND	GND
184	VCC	VCC
185	GND	GND
186	PRA, I/O	PRA, I/O
195	NC	I/O
201	VCC	VCC
205	NC	I/O
208	DCLK, I/O	DCLK, I/O

Notes:

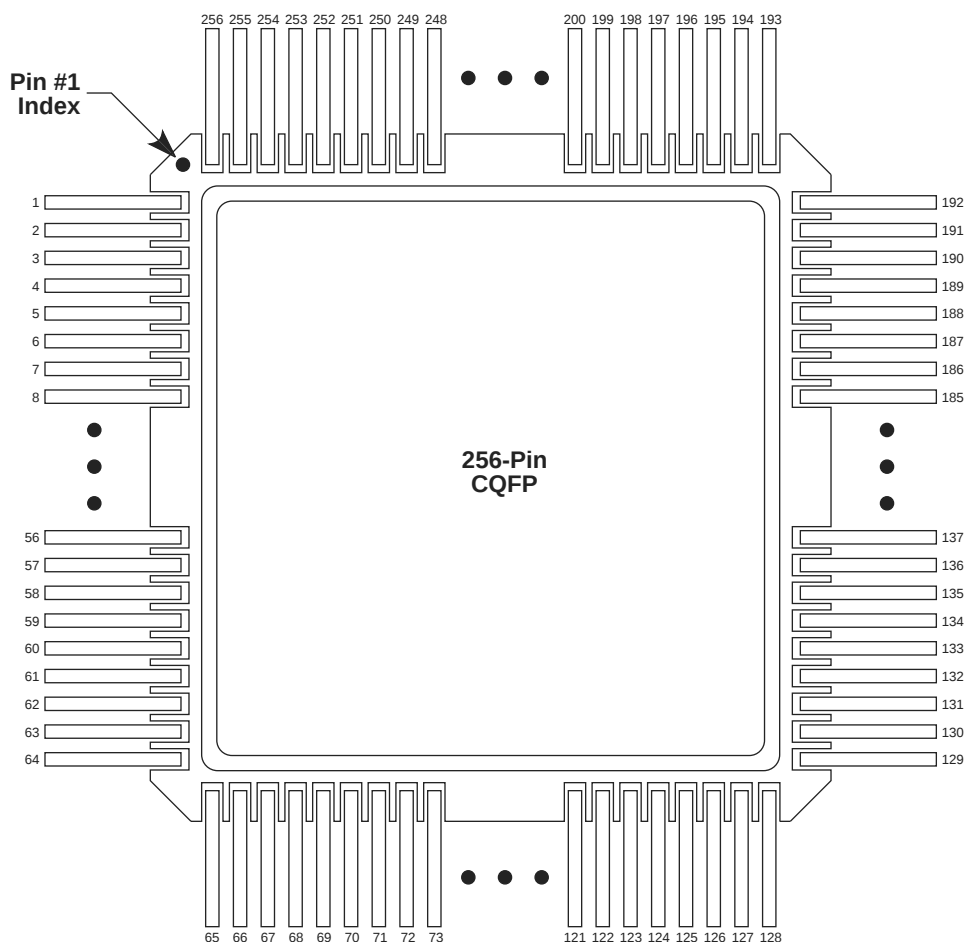
1. All unlisted pin numbers are user I/Os.
2. NC denotes no connection.
3. MODE should be terminated to GND through a 10K resistor to enable Actionprobe usage; otherwise it can be terminated directly to GND.

CQ132		CQ132	
Pin Number	A1425 Function	Pin Number	A1425 Function
1	NC	67	NC
2	GND	74	GND
3	SDI, I/O	75	VCC
9	MODE	78	VCC
10	GND	89	VCC
11	VCC	90	GND
22	VCC	91	VCC
26	GND	92	GND
27	VCC	98	IOCLK, I/O
34	NC	99	NC
36	GND	100	NC
42	GND	101	GND
43	VCC	106	GND
48	PRB, I/O	107	VCC
50	HCLK, I/O	116	CLKA, I/O
58	GND	117	CLKB, I/O
59	VCC	118	PRA, I/O
63	SDO	122	GND
64	IOPCL, I/O	123	VCC
65	GND	131	DCLK, I/O
66	NC	132	NC

Notes:

1. All unlisted pin numbers are user I/Os.
2. NC denotes no connection.
3. MODE should be terminated to GND through a 10K resistor to enable Actionprobe usage; otherwise it can be terminated directly to GND.

CQ256



Note: This is the top view.

Note

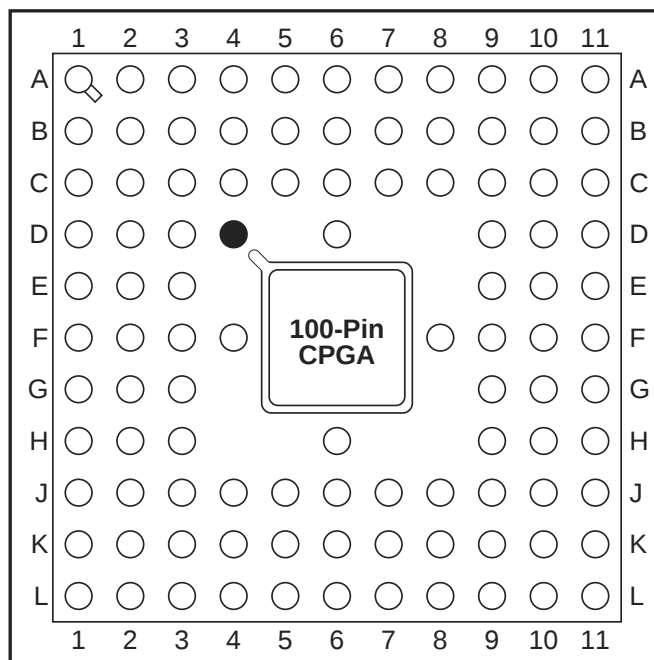
For Package Manufacturing and Environmental information, visit the Resource Center at <http://www.microsemi.com/soc/products/solutions/package/docs.aspx>

BG225	
A1460 Function	Location
CLKA or I/O	C8
CLKB or I/O	B8
DCLK or I/O	B2
GND	A1, A15, D15, F8, G7, G8, G9, H6, H7, H8, H9, H10, J7, J8, J9, K8, P2, R15
HCLK or I/O	P9
IOCLK or I/O	B14
IOPCL or I/O	P14
MODE	D1
NC	A11, B5, B7, D8, D12, F6, F11, H1, H12, H14, K11, L1, L13, N8, P5, R1, R8, R11, R14
PRA or I/O	A7
PRB or I/O	L7
SDI or I/O	D4
SDO	N13
VCC	A8, B12, D5, D14, E3, E8, E13, H2, H3, H11, H15, K4, L2, L12, M8, M15, P4, P8, R13

Notes:

1. All unlisted pin numbers are user I/Os.
2. NC denotes no connection.
3. MODE should be terminated to GND through a 10K resistor to enable Actionprobe usage; otherwise it can be terminated directly to GND.
4. The BG225 package has been discontinued.

PG100



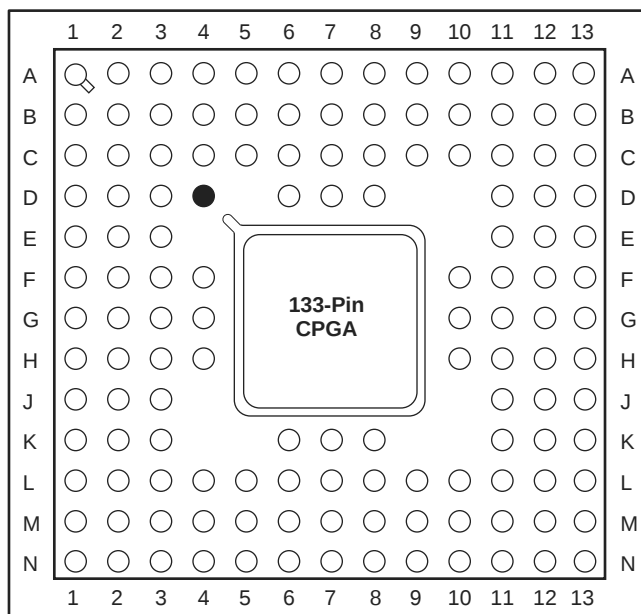
● Orientation Pin

Note: This is the top view.

Note

For Package Manufacturing and Environmental information, visit the Resource Center at <http://www.microsemi.com/soc/products/solutions/package/docs.aspx>

PG133

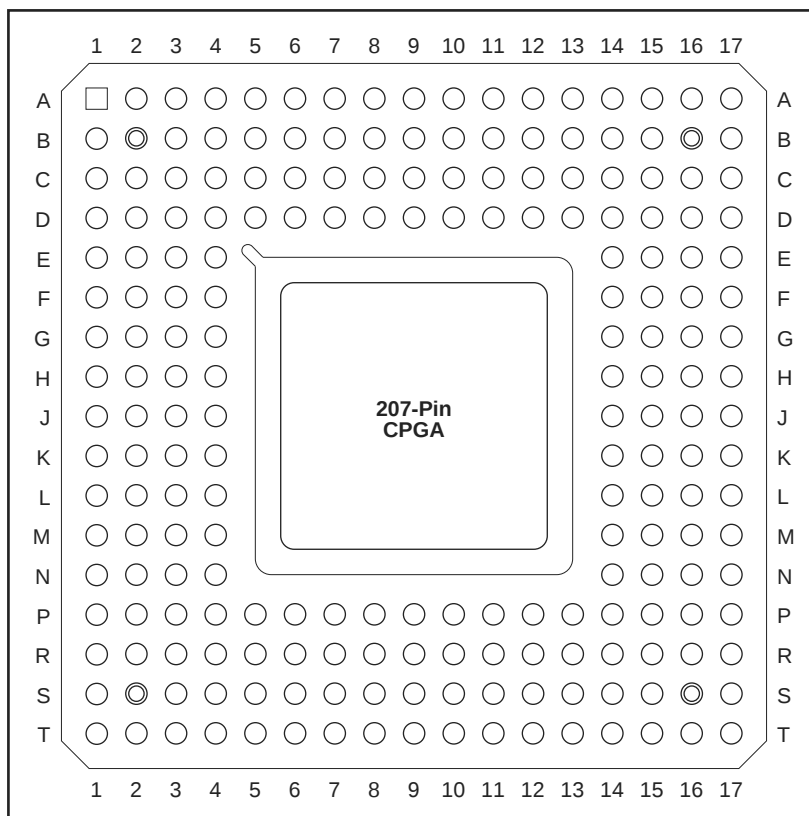


Note: This is the top view.

Note

For Package Manufacturing and Environmental information, visit the Resource Center at <http://www.microsemi.com/soc/products/solutions/package/docs.aspx>

PG207



Note: This is the top view.

Note

For Package Manufacturing and Environmental information, visit the Resource Center at <http://www.microsemi.com/soc/products/solutions/package/docs.aspx>

PG207	
A1460 Function	Location
CLKA or I/O	K1
CLKB or I/O	J3
DCLK or I/O	E4
GND	C14, D4, D5, D9, D14, J4, J14, P3, P4, P7, P9, P14, R15
HCLK or I/O	J15
IOCLK or I/O	P5
IOPCL or I/O	N14
MODE	D7
NC	A1, A2, A16, A17, B1, B17, C1, C2, S1, S3, S17, T1, T2, T16, T17
PRA or I/O	H1
PRB or I/O	K16
SDI or I/O	C3
SDO	P15
VCC	B2, B9, B16, D11, J2, J16, P12, S2, S9, S16, T5

Notes:

1. All unlisted pin numbers are user I/Os.
2. NC denotes no connection.
3. MODE should be terminated to GND through a 10K resistor to enable Actionprobe usage; otherwise it can be terminated directly to GND.



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