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## Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

## Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

| Details | |
|---|---|
| Product Status | Obsolete |
| Number of LABs/CLBs | 200 |
| Number of Logic Elements/Cells | - |
| Total RAM Bits | - |
| Number of I/O | 80 |
| Number of Gates | 1500 |
| Voltage - Supply | 4.5V ~ 5.5V |
| Mounting Type | Surface Mount |
| Operating Temperature | 0°C ~ 70°C (TA) |
| Package / Case | 100-BQFP |
| Supplier Device Package | 100-PQFP (20x14) |
| Purchase URL | https://www.e-xfl.com/product-detail/microsemi/a1415a-pqg100c |

# Ordering Information

A14100 A – 1 RQ G 208 C

- **Application (Temperature Range)**
  - C = Commercial (0 to +70°C)
  - I = Industrial (–40 to +85°C)
  - M = Military (–55 to +125°C)
  - B = MIL-STD-883
- **Package Lead Count**
- **Lead-Free Packaging**
  - Blank = Standard Packaging
  - G = RoHS Compliant Packaging
- **Package Type**
  - PG = Ceramic Pin Grid Array
  - PL = Plastic Leaded Chip Carrier
  - PQ = Plastic Quad Flatpack
  - RQ = Plastic Power Quad Flatpack
  - VQ = Very Thin (1.0 mm) Quad Flatpack
  - TQ = Thin (1.4 mm) Quad Flatpack
  - CQ = Ceramic Quad Flatpack
  - BG = Plastic Ball Grid Array
- **Speed Grade**
  - Std = Standard Speed
  - –1 = Approximately 15% faster than Standard
  - –2 = Approximately 25% faster than Standard
  - –3 = Approximately 35% faster than Standard
- **Die Revision**
  - A = 1.0 mm CMOS Process
- **Part Number**
  - A1415A = 1,500 Gates
  - A14V15A = 1,500 Gates (3.3 V)
  - A1425A = 2,500 Gates
  - A14V25A = 2,500 Gates (3.3 V)
  - A1440A = 4,000 Gates
  - A14V40A = 4,000 Gates (3.3 V)
  - A1460A = 6,000 Gates
  - A14V60A = 6,000 Gates (3.3 V)
  - A14100A = 10,000 Gates
  - A14V100A = 10,000 Gates (3.3 V)

Notes:

1. *The –2 and –3 speed grades have been discontinued.*
2. *The Ceramic Pin Grid Array packages PG100, PG133, and PG175 have been discontinued in all device densities, speed grades, and temperature grades.*
3. *The Plastic Ball Grid Array package BG225 has been discontinued in all device densities (specifically for A1460A), all speed grades, and all temperature grades.*
4. *Military Grade devices are no longer available for the A1440A device.*
5. *For more information about discontinued devices, refer to the Product Discontinuation Notices (PDNs) listed below, available on the Microsemi SoC Products Group website:*
   *PDN March 2001*
   *PDN 0104*
   *PDN 0203*
   *PDN 0604*
   *PDN 1004*

| Device/Package | Speed Grade[1] | | | | Application[1] | | | |
|---|---|---|---|---|---|---|---|---|
| | Std. | –1 | –2 | –3 | C | I | M | B |
| **A14V40A Device** | | | | | | | | |
| 84-Pin Plastic Leaded Chip Carrier (PLCC) | ✓ | – | – | – | ✓ | – | – | – |
| 100-Pin Very Thin Quad Flatpack (VQFP) | ✓ | – | – | – | ✓ | – | – | – |
| 160-Pin Plastic Quad Flatpack (PQFP) | ✓ | – | – | – | ✓ | – | – | – |
| 176-Pin Thin Quad Flatpack (TQFP) | ✓ | – | – | – | ✓ | – | – | – |
| **A1460A Device** | | | | | | | | |
| 160-Pin Plastic Quad Flatpack (PQFP) | ✓ | ✓ | D | D | ✓ | ✓ | – | – |
| 176-Pin Thin Quad Flatpack (TQFP) | ✓ | ✓ | D | D | ✓ | ✓ | – | – |
| 196-Pin Ceramic Quad Flatpack (CQFP) | ✓ | ✓ | – | – | ✓ | – | ✓ | ✓ |
| 207-Pin Ceramic Pin Grid Array (CPGA) | ✓ | ✓ | D | D | ✓ | – | ✓ | ✓ |
| 208-Pin Plastic Quad Flatpack (PQFP) | ✓ | ✓ | D | D | ✓ | ✓ | – | – |
| 225-Pin Plastic Ball Grid Array (BGA) | D | D | D | D | D | – | – | – |
| **A14V60A Device** | | | | | | | | |
| 160-Pin Plastic Quad Flatpack (PQFP) | ✓ | – | – | – | ✓ | – | – | – |
| 176-Pin Thin Quad Flatpack (TQFP) | ✓ | – | – | – | ✓ | – | – | – |
| 208-Pin Plastic Quad Flatpack (PQFP) | ✓ | – | – | – | ✓ | – | – | – |
| **A14100A Device** | | | | | | | | |
| 208-Pin Power Quad Flatpack (RQFP) | ✓ | ✓ | D | D | ✓ | ✓ | – | – |
| 257-Pin Ceramic Pin Grid Array (CPGA) | ✓ | ✓ | D | D | ✓ | – | ✓ | ✓ |
| 313-Pin Plastic Ball Grid Array (BGA) | ✓ | ✓ | D | D | ✓ | – | – | – |
| 256-Pin Ceramic Quad Flatpack (CQFP) | ✓ | ✓ | – | – | ✓ | – | ✓ | ✓ |
| **A14V100A Device** | | | | | | | | |
| 208-Pin Power Quad Flatpack (RQFP) | ✓ | – | – | – | ✓ | – | – | – |
| 313-Pin Plastic Ball Grid Array (BGA) | ✓ | – | – | – | ✓ | – | – | – |

*Notes:*

1. *Applications:*
   *C = Commercial*
   *I = Industrial*
   *M = Military*
2. *Commercial only*

*Availability:*
*✓ = Available*
*P = Planned*
*– = Not planned*
*D = Discontinued*

*Speed Grade:*
*–1 = Approx. 15% faster than Std.*
*–2 = Approx. 25% faster than Std.*
*–3 = Approx. 35% faster than Std.*
*(–2 and –3 speed grades have been discontinued.)*

# Logic Modules

ACT 3 logic modules are enhanced versions of the 1200XL family logic modules. As in the 1200XL family, there are two types of modules: C-modules and S-modules (Figure 2-2 and Figure 2-3). The C-module is functionally equivalent to the 1200XL C-module and implements high fanin combinatorial macros, such as 5-input AND, 5-input OR, and so on. It is available for use as the CM8 hard macro. The S-module is designed to implement high-speed sequential functions within a single module.

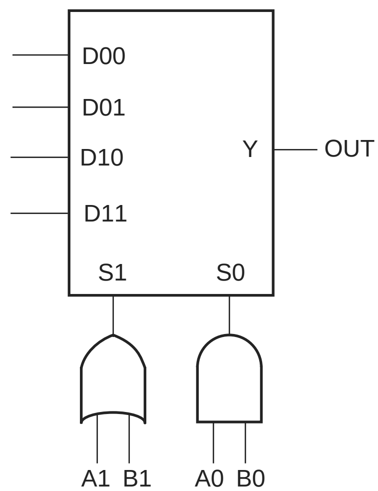



***Figure 2-2 •*** **C-Module Diagram**

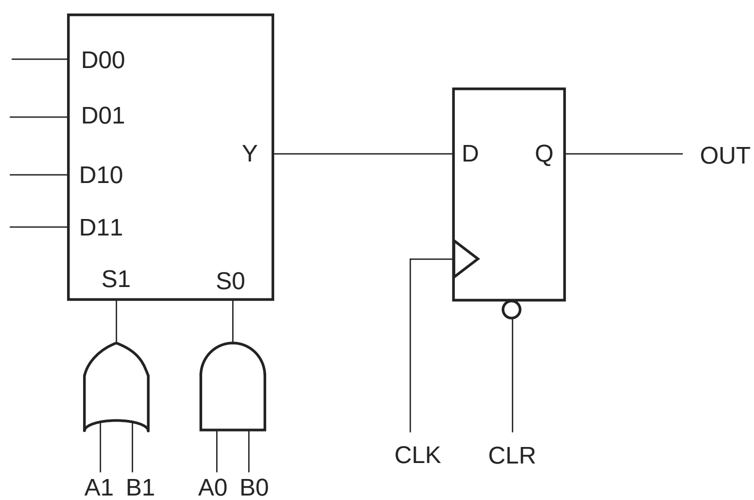



***Figure 2-3 •*** **S-Module Diagram**

S-modules consist of a full C-module driving a flip-flop, which allows an additional level of logic to be implemented without additional propagation delay. It is available for use as the DFM8A/B and DLM8A/B hard macros. C-modules and S-modules are arranged in pairs called module-pairs. Module-pairs are arranged in alternating patterns and make up the bulk of the array. This arrangement allows the placement software to support two-module macros of four types (CC, CS, SC, and SS). The C-module implements the following function:

Y = !S1 * !S0 * D00 + !S1 * S0 * D01 + S1 * !S0 * D10 + S1 * S0 * D11

*EQ 1*

where: S0 = A0 * B0 and S1 = A1 + B1

## Dedicated Clocks

Dedicated clock networks support high performance by providing sub-nanosecond skew and guaranteed performance. Dedicated clock networks contain no programming elements in the path from the I/O Pad Driver to the input of S-modules or I/O modules. There are two dedicated clock networks: one for the array registers (HCLK), and one for the I/O registers (IOCLK). The clock networks are accessed by special I/Os.

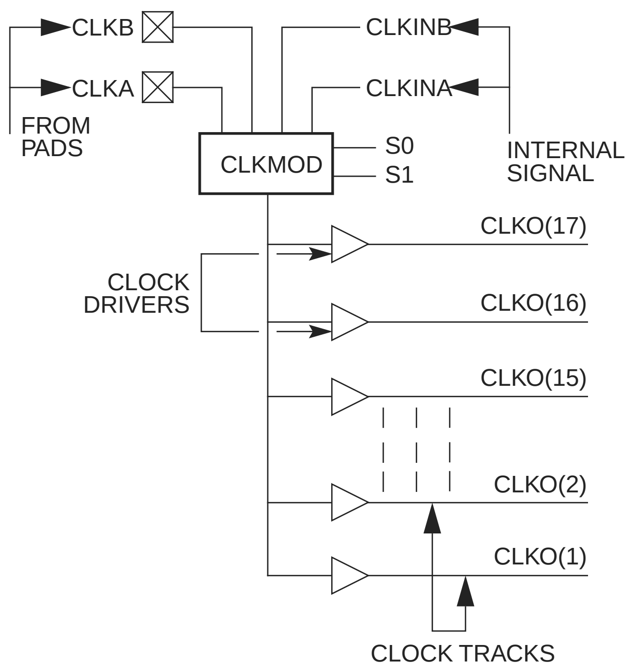



***Figure 2-6 •*** **Clock Networks**

The routed clock networks are referred to as CLK0 and CLK1. Each network is connected to a clock module (CLKMOD) that selects the source of the clock signal and may be driven as follows (Figure 2-6):

- Externally from the CLKA pad
- Externally from the CLKB pad
- Internally from the CLKINA input
- Internally from the CLKINB input

The clock modules are located in the top row of I/O modules. Clock drivers and a dedicated horizontal clock track are located in each horizontal routing channel. The function of the clock module is determined by the selection of clock macros from the macro library. The macro CLKBUF is used to connect one of the two external clock pins to a clock network, and the macro CLKINT is used to connect an internally generated clock signal to a clock network. Since both clock networks are identical, the user does not care whether CLK0 or CLK1 is being used. Routed clocks can also be used to drive high fanout nets like resets, output enables, or data enables. This saves logic modules and results in performance increases in some cases.

# Routing Structure

The ACT 3 architecture uses vertical and horizontal routing tracks to connect the various logic and I/O modules. These routing tracks are metal interconnects that may either be of continuous length or broken into segments. Segments can be joined together at the ends using antifuses to increase their lengths up to the full length of the track.

## Horizontal Routing

Horizontal channels are located between the rows of modules and are composed of several routing tracks. The horizontal routing tracks within the channel are divided into one or more segments. The minimum horizontal segment length is the width of a module-pair, and the maximum horizontal segment length is the full length of the channel. Any segment that spans more than one-third the row length is considered a long horizontal segment. A typical channel is shown in Figure 2-7. Undedicated horizontal routing tracks are used to route signal nets. Dedicated routing tracks are used for the global clock networks and for power and ground tie-off tracks.

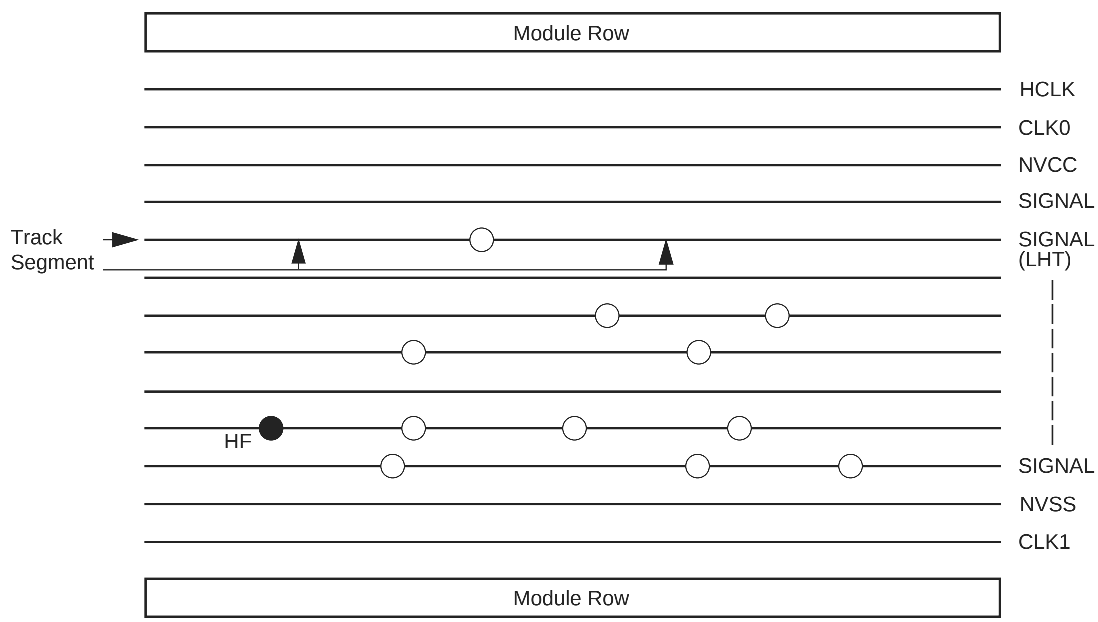



***Figure 2-7 •*** **Horizontal Routing Tracks and Segments**

## Vertical Routing

Other tracks run vertically through the modules. Vertical tracks are of three types: input, output, and long. Vertical tracks are also divided into one or more segments. Each segment in an input track is dedicated to the input of a particular module. Each segment in an output track is dedicated to the output of a particular module. Long segments are uncommitted and can be assigned during routing. Each output segment spans four channels (two above and two below), except near the top and bottom of the array where edge effects occur. LVTs contain either one or two segments. An example of vertical routing tracks and segments is shown in Figure 2-8.

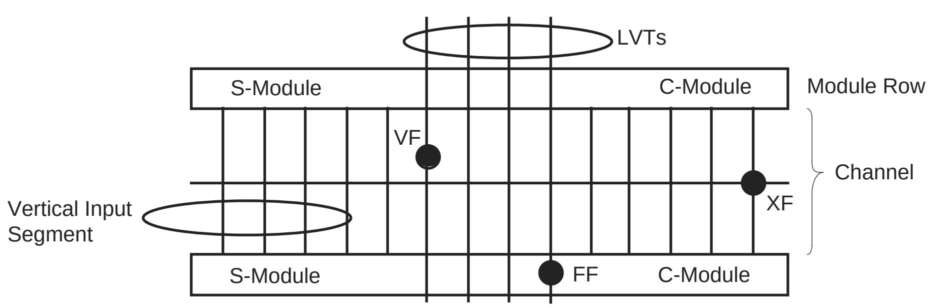



***Figure 2-8 •*** **Vertical Routing Tracks and Segments**

## Antifuse Connections

An antifuse is a “normally open” structure as opposed to the normally closed fuse structure used in PROMs or PALs. The use of antifuses to implement a programmable logic device results in highly testable structures as well as an efficient programming architecture. The structure is highly testable because there are no preexisting connections; temporary connections can be made using pass transistors. These temporary connections can isolate individual antifuses to be programmed as well as isolate individual circuit structures to be tested. This can be done both before and after programming. For example, all metal tracks can be tested for continuity and shorts between adjacent tracks, and the functionality of all logic modules can be verified.

Four types of antifuse connections are used in the routing structure of the ACT 3 array. (The physical structure of the antifuse is identical in each case; only the usage differs.)

Table 2-1 shows four types of antifuses.

***Table 2-1 •*** **Antifuse Types**

| Type | Description |
|---|---|
| XF | Horizontal-to-vertical connection |
| HF | Horizontal-to-horizontal connection |
| VF | Vertical-to-vertical connection |
| FF | "Fast" vertical connection |

Examples of all four types of connections are shown in Figure 2-7 on page 2-6 and Figure 2-8 on page 2-6.

## Module Interface

Connections to Logic and I/O modules are made through vertical segments that connect to the module inputs and outputs. These vertical segments lie on vertical tracks that span the entire height of the array.

### *Module Input Connections*

The tracks dedicated to module inputs are segmented by pass transistors in each module row. During normal user operation, the pass transistors are inactive, which isolates the inputs of a module from the inputs of the module directly above or below it. During certain test modes, the pass transistors are active to verify the continuity of the metal tracks. Vertical input segments span only the channel above or the channel below. The logic modules are arranged such that half of the inputs are connected to the channel above and half of the inputs to segments in the channel below, as shown in Figure 2-9.

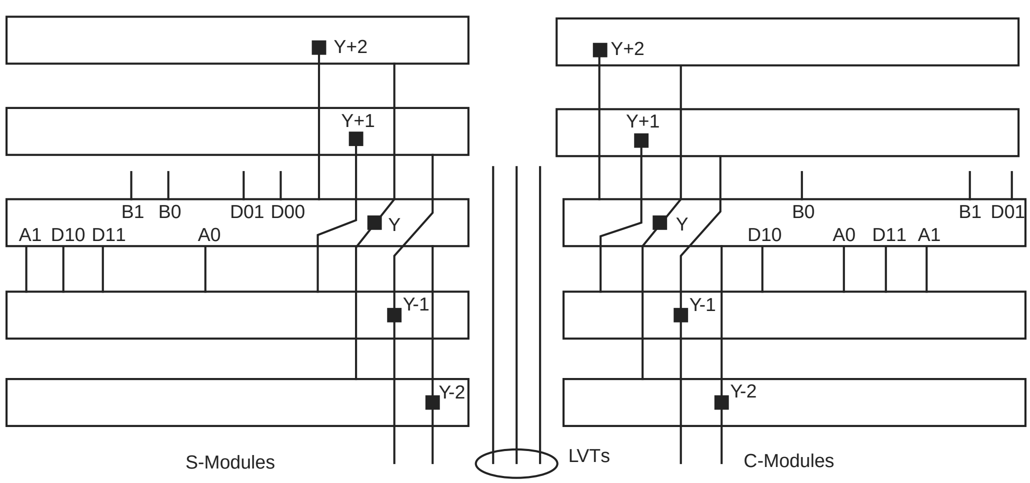



***Figure 2-9 •*** **Logic Module Routing Interface**

### Module Output Connections

Module outputs have dedicated output segments. Output segments extend vertically two channels above and two channels below, except at the top or bottom of the array. Output segments twist, as shown in Figure 10, so that only four vertical tracks are required.

### LVT Connections

Outputs may also connect to nondedicated segments called Long Vertical Tracks (LVTs). Each module pair in the array shares four LVTs that span the length of the column. Any module in the column pair can connect to one of the LVTs in the column using an FF connection. The FF connection uses antifuses connected directly to the driver stage of the module output, bypassing the isolation transistor. FF antifuses are programmed at a higher current level than HF, VF, or XF antifuses to produce a lower resistance value.

### Antifuse Connections

In general every intersection of a vertical segment and a horizontal segment contains an unprogrammed antifuse (XF-type). One exception is in the case of the clock networks.

### Clock Connections

To minimize loading on the clock networks, a subset of inputs has antifuses on the clock tracks. Only a few of the C-module and S-module inputs can be connected to the clock networks. To further reduce loading on the clock network, only a subset of the horizontal routing tracks can connect to the clock inputs of the S-module.

## Programming and Test Circuits

The array of logic and I/O modules is surrounded by test and programming circuits controlled by the temporary special I/O pins MODE, SDI, and DCLK. The function of these pins is similar to all ACT family devices. The ACT 3 family also includes support for two Actionprobe® circuits, allowing complete observability of any logic or I/O module in the array using the temporary special I/O pins, PRA and PRB.

# Package Thermal Characteristics

The device junction to case thermal characteristic is θjc, and the junction to ambient air characteristic is θja. The thermal characteristics for θja are shown with two different air flow rates.

Maximum junction temperature is 150°C.

A sample calculation of the absolute maximum power dissipation allowed for a CPGA 175-pin package at commercial temperature and still air is as follows:

$$\frac{\text{Max. junction temp. (°C)} - \text{Max. ambient temp. (°C)}}{\theta_{ja}\text{°C/W}} = \frac{150\text{°C} - 70\text{°C}}{25\text{°C/W}} = 3.2\text{ W}$$

*EQ 2*

***Table 2-8*** **• Package Thermal Characteristics**

| Package Type* | Pin Count | $\theta_{jc}$ | $\theta_{ja}$ Still Air | $\theta_{ja}$ 300 ft./min. | Units |
|---|---|---|---|---|---|
| Ceramic Pin Grid Array | 100 | 20 | 35 | 17 | °C/W |
| | 133 | 20 | 30 | 15 | °C/W |
| | 175 | 20 | 25 | 14 | °C/W |
| | 207 | 20 | 22 | 13 | °C/W |
| | 257 | 20 | 15 | 8 | °C/W |
| Ceramic Quad Flatpack | 132 | 13 | 55 | 30 | °C/W |
| | 196 | 13 | 36 | 24 | °C/W |
| | 256 | 13 | 30 | 18 | °C/W |
| Plastic Quad Flatpack | 100 | 13 | 51 | 40 | °C/W |
| | 160 | 10 | 33 | 26 | °C/W |
| | 208 | 10 | 33 | 26 | °C/W |
| Very Thin Quad Flatpack | 100 | 12 | 43 | 35 | °C/W |
| Thin Quad Flatpack | 176 | 11 | 32 | 25 | °C/W |
| Power Quad Flatpack | 208 | 0.4 | 17 | 13 | °C/W |
| Plastic Leaded Chip Carrier | 84 | 12 | 37 | 28 | °C/W |
| Plastic Ball Grid Array | 225 | 10 | 25 | 19 | °C/W |
| | 313 | 10 | 23 | 17 | °C/W |

*Note: Maximum power dissipation in still air:*
*PQ160 = 2.4 W*
*PQ208 = 2.4 W*
*PQ100 = 1.6 W*
*VQ100 = 1.9 W*
*TQ176 = 2.5 W*
*PL84 = 2.2 W*
*RQ208 = 4.7 W*
*BG225 = 3.2 W*
*BG313 = 3.5 W*

## A1425A, A14V25A Timing Characteristics (continued)

***Table 2-25*** **• A1425A, A14V25A Worst-Case Commercial Conditions, VCC = 4.75 V, $T_J$ = 70°C**

| Dedicated (hardwired) I/O Clock Network | | –3 Speed[1] | | –2 Speed[1] | | –1 Speed | | Std. Speed | | 3.3 V Speed[1] | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **Parameter/Description** | | **Min.** | **Max.** | **Min.** | **Max.** | **Min.** | **Max.** | **Min.** | **Max.** | **Min.** | **Max.** | |
| $t_{IOCKH}$ | Input Low to High (pad to I/O module input) | | 2.0 | | 2.3 | | 2.6 | | 3.0 | | 3.5 | ns |
| $t_{IOPWH}$ | Minimum Pulse Width High | 1.9 | | 2.4 | | 3.3 | | 3.8 | | 4.8 | | ns |
| $t_{IPOWL}$ | Minimum Pulse Width Low | 1.9 | | 2.4 | | 3.3 | | 3.8 | | 4.8 | | ns |
| $t_{IOSAPW}$ | Minimum Asynchronous Pulse Width | 1.9 | | 2.4 | | 3.3 | | 3.8 | | 4.8 | | ns |
| $t_{IOCKSW}$ | Maximum Skew | | 0.4 | | 0.4 | | 0.4 | | 0.4 | | 0.4 | ns |
| $t_{IOP}$ | Minimum Period | 4.0 | | 5.0 | | 6.8 | | 8.0 | | 10.0 | | ns |
| $f_{IOMAX}$ | Maximum Frequency | | 250 | | 200 | | 150 | | 125 | | 100 | MHz |
| **Dedicated (hardwired) Array Clock** | | | | | | | | | | | | |
| $t_{HCKH}$ | Input Low to High (pad to S-module input) | | 3.0 | | 3.4 | | 3.9 | | 4.5 | | 5.5 | ns |
| $t_{HCKL}$ | Input High to Low (pad to S-module input) | | 3.0 | | 3.4 | | 3.9 | | 4.5 | | 5.5 | ns |
| $t_{HPWH}$ | Minimum Pulse Width High | 1.9 | | 2.4 | | 3.3 | | 3.8 | | 4.8 | | ns |
| $t_{HPWL}$ | Minimum Pulse Width Low | 1.9 | | 2.4 | | 3.3 | | 3.8 | | 4.8 | | ns |
| $t_{HCKSW}$ | Delta High to Low, Low Slew | | 0.3 | | 0.3 | | 0.3 | | 0.3 | | 0.3 | ns |
| $t_{HP}$ | Minimum Period | 4.0 | | 5.0 | | 6.8 | | 8.0 | | 10.0 | | ns |
| $f_{HMAX}$ | Maximum Frequency | | 250 | | 200 | | 150 | | 125 | | 100 | MHz |
| **Routed Array Clock Networks** | | | | | | | | | | | | |
| $t_{RCKH}$ | Input Low to High (FO = 64) | | 3.7 | | 4.1 | | 4.7 | | 5.5 | | 9.0 | ns |
| $t_{RCKL}$ | Input High to Low (FO = 64) | | 4.0 | | 4.5 | | 5.1 | | 6.0 | | 9.0 | ns |
| $t_{RPWH}$ | Min. Pulse Width High (FO = 64) | 3.3 | | 3.8 | | 4.2 | | 4.9 | | 6.5 | | ns |
| $t_{RPWL}$ | Min. Pulse Width Low (FO = 64) | 3.3 | | 3.8 | | 4.2 | | 4.9 | | 6.5 | | ns |
| $t_{RCKSW}$ | Maximum Skew (FO = 128) | | 0.7 | | 0.8 | | 0.9 | | 1.0 | | 1.0 | ns |
| $t_{RP}$ | Minimum Period (FO = 64) | 6.8 | | 8.0 | | 8.7 | | 10.0 | | 13.4 | | ns |
| $f_{RMAX}$ | Maximum Frequency (FO = 64) | | 150 | | 125 | | 115 | | 100 | | 75 | MHz |
| **Clock-to-Clock Skews** | | | | | | | | | | | | |
| $t_{IOHCKSW}$ | I/O Clock to H-Clock Skew | 0.0 | 1.7 | 0.0 | 1.8 | 0.0 | 2.0 | 0.0 | 2.2 | 0.0 | 3.0 | ns |
| $t_{IORCKSW}$ | I/O Clock to R-Clock Skew (FO = 64)<br>(FO = 80) | 0.0<br>0.0 | 1.0<br>3.0 | 0.0<br>0.0 | 1.0<br>3.0 | 0.0<br>0.0 | 1.0<br>3.0 | 0.0<br>0.0 | 1.0<br>3.0 | 0.0<br>0.0 | 3.0<br>3.0 | ns |
| $t_{HRCKSW}$ | H-Clock to R-Clock Skew (FO = 64)<br>(FO = 80) | 0.0<br>0.0 | 1.0<br>3.0 | 0.0<br>0.0 | 1.0<br>3.0 | 0.0<br>0.0 | 1.0<br>3.0 | 0.0<br>0.0 | 1.0<br>3.0 | 0.0<br>0.0 | 1.0<br>3.0 | ns |

*Notes:*

1. *The –2 and –3 speed grades have been discontinued. Refer to PDN 0104, PDN 0203, PDN 0604, and PDN 1004 at http://www.microsemi.com/soc/support/notifications/default.aspx#pdn.*
2. *Delays based on 35 pF loading.*

## A1460A, A14V60A Timing Characteristics (continued)

***Table 2-31*** **• A1460A, A14V60A Worst-Case Commercial Conditions, VCC = 4.75 V, $T_J$ = 70°C**

| I/O Module Input Propagation Delays | | –3 Speed[1] | | –2 Speed[1] | | –1 Speed | | Std. Speed | | 3.3 V Speed[1] | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **Parameter/Description** | | **Min.** | **Max.** | **Min.** | **Max.** | **Min.** | **Max.** | **Min.** | **Max.** | **Min.** | **Max.** | |
| $t_{INY}$ | Input Data Pad to Y | | 2.8 | | 3.2 | | 3.6 | | 4.2 | | 5.5 | ns |
| $t_{ICKY}$ | Input Reg IOCLK Pad to Y | | 4.7 | | 5.3 | | 6.0 | | 7.0 | | 9.2 | ns |
| $t_{OCKY}$ | Output Reg IOCLK Pad to Y | | 4.7 | | 5.3 | | 6.0 | | 7.0 | | 9.2 | ns |
| $t_{ICLRY}$ | Input Asynchronous Clear to Y | | 4.7 | | 5.3 | | 6.0 | | 7.0 | | 9.2 | ns |
| $t_{OCLRY}$ | Output Asynchronous Clear to Y | | 4.7 | | 5.3 | | 6.0 | | 7.0 | | 9.2 | ns |
| **Predicted Input Routing Delays[2]** | | | | | | | | | | | | |
| $t_{RD1}$ | FO = 1 Routing Delay | | 0.9 | | 1.0 | | 1.1 | | 1.3 | | 1.7 | ns |
| $t_{RD2}$ | FO = 2 Routing Delay | | 1.2 | | 1.4 | | 1.6 | | 1.8 | | 2.4 | ns |
| $t_{RD3}$ | FO = 3 Routing Delay | | 1.4 | | 1.6 | | 1.8 | | 2.1 | | 2.8 | ns |
| $t_{RD4}$ | FO = 4 Routing Delay | | 1.7 | | 1.9 | | 2.2 | | 2.5 | | 3.3 | ns |
| $t_{RD8}$ | FO = 8 Routing Delay | | 2.8 | | 3.2 | | 3.6 | | 4.2 | | 5.5 | ns |
| **I/O Module Sequential Timing (wrt IOCLK pad)** | | | | | | | | | | | | |
| $t_{INH}$ | Input F-F Data Hold | 0.0 | | 0.0 | | 0.0 | | 0.0 | | 0.0 | | ns |
| $t_{INSU}$ | Input F-F Data Setup | 1.3 | | 1.5 | | 1.8 | | 2.0 | | 2.0 | | ns |
| $t_{IDEH}$ | Input Data Enable Hold | 0.0 | | 0.0 | | 0.0 | | 0.0 | | 0.0 | | ns |
| $t_{IDESU}$ | Input Data Enable Setup | 5.8 | | 6.5 | | 7.5 | | 8.6 | | 8.6 | | ns |
| $t_{OUTH}$ | Output F-F Data hold | 0.7 | | 0.8 | | 0.9 | | 1.0 | | 1.0 | | ns |
| $t_{OUTSU}$ | Output F-F Data Setup | 0.7 | | 0.8 | | 0.9 | | 1.0 | | 1.0 | | ns |
| $t_{ODEH}$ | Output Data Enable Hold | 0.3 | | 0.4 | | 0.4 | | 0.5 | | 0.5 | | ns |
| $f_{ODESU}$ | Output Data Enable Setup | 1.3 | | 1.5 | | 1.7 | | 2.0 | | 2.0 | | ns |

*Notes:*

5. *The –2 and –3 speed grades have been discontinued. Refer to PDN 0104, PDN 0203, PDN 0604, and PDN 1004 at http://www.microsemi.com/soc/support/notifications/default.aspx#pdn.*
6. *Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual worst-case performance. Post-route timing is based on actual routing delay measurements performed on the device prior to shipment.*

## A1460A, A14V60A Timing Characteristics (continued)

***Table 2-33* • A1460A, A14V60A Worst-Case Commercial Conditions, VCC = 4.75 V, $T_J$ = 70°C**

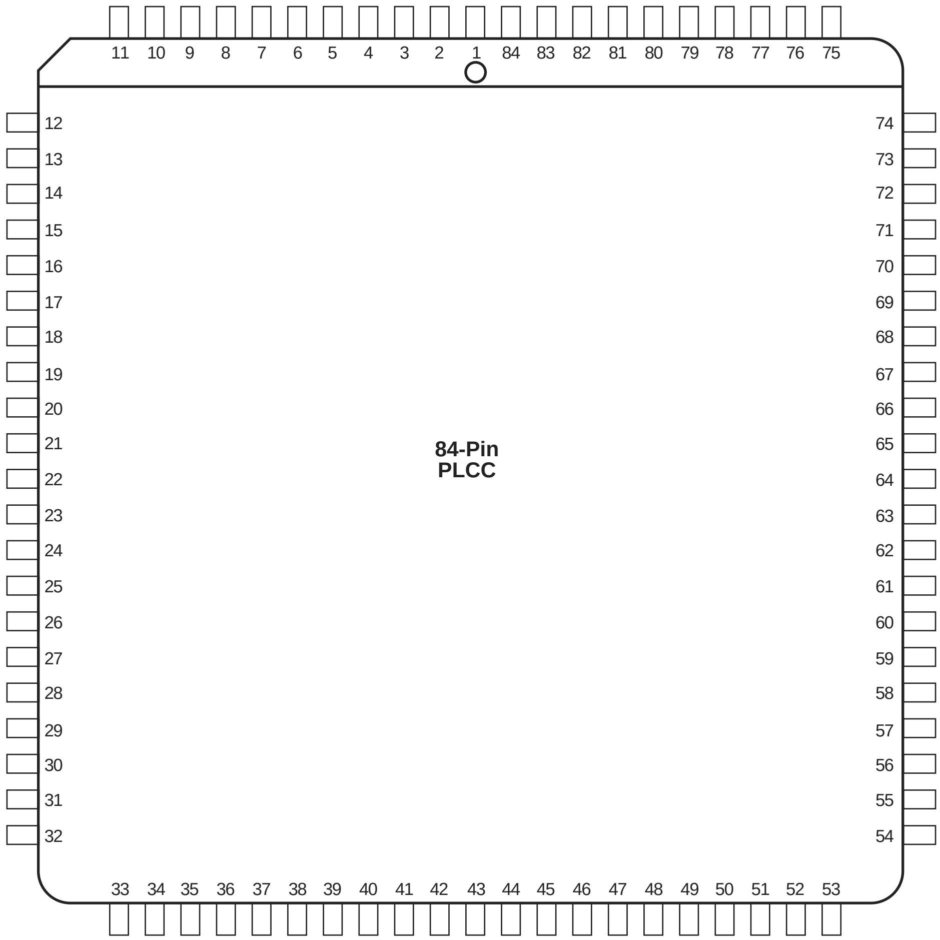
| Dedicated (hardwired) I/O Clock Network | | –3 Speed[1] | | –2 Speed[1] | | –1 Speed | | Std. Speed | | 3.3 V Speed[1] | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **Parameter/Description** | | **Min.** | **Max.** | **Min.** | **Max.** | **Min.** | **Max.** | **Min.** | **Max.** | **Min.** | **Max.** | |
| $t_{IOCKH}$ | Input Low to High (pad to I/O module input) | | 2.3 | | 2.6 | | 3.0 | | 3.5 | | 4.5 | ns |
| $t_{IOPWH}$ | Minimum Pulse Width High | 2.4 | | 3.2 | | 3.8 | | 4.8 | | 6.5 | | ns |
| $t_{IPOWL}$ | Minimum Pulse Width Low | 2.4 | | 3.2 | | 3.8 | | 4.8 | | 6.5 | | ns |
| $t_{IOSAPW}$ | Minimum Asynchronous Pulse Width | 2.4 | | 3.2 | | 3.8 | | 4.8 | | 6.5 | | ns |
| $t_{IOCKSW}$ | Maximum Skew | | 0.6 | | 0.6 | | 0.6 | | 0.6 | | 0.6 | ns |
| $t_{IOP}$ | Minimum Period | 5.0 | | 6.8 | | 8.0 | | 10.0 | | 13.4 | | ns |
| $f_{IOMAX}$ | Maximum Frequency | | 200 | | 150 | | 125 | | 100 | | 75 | MHz |
| **Dedicated (hardwired) Array Clock** | | | | | | | | | | | | |
| $t_{HCKH}$ | Input Low to High (pad to S-module input) | | 3.7 | | 4.1 | | 4.7 | | 5.5 | | 7.0 | ns |
| $t_{HCKL}$ | Input High to Low (pad to S-module input) | | 3.7 | | 4.1 | | 4.7 | | 5.5 | | 7.0 | ns |
| $t_{HPWH}$ | Minimum Pulse Width High | 2.4 | | 3.2 | | 3.8 | | 4.8 | | 6.5 | | ns |
| $t_{HPWL}$ | Minimum Pulse Width Low | 2.4 | | 3.2 | | 3.8 | | 4.8 | | 6.5 | | ns |
| $t_{HCKSW}$ | Delta High to Low, Low Slew | | 0.6 | | 0.6 | | 0.6 | | 0.6 | | 0.6 | ns |
| $t_{HP}$ | Minimum Period | 5.0 | | 6.8 | | 8.0 | | 10.0 | | 13.4 | | ns |
| $f_{HMAX}$ | Maximum Frequency | | 200 | | 150 | | 125 | | 100 | | 75 | MHz |
| **Routed Array Clock Networks** | | | | | | | | | | | | |
| $t_{RCKH}$ | Input Low to High (FO = 64) | | 6.0 | | 6.8 | | 7.7 | | 9.0 | | 11.8 | ns |
| $t_{RCKL}$ | Input High to Low (FO = 64) | | 6.0 | | 6.8 | | 7.7 | | 9.0 | | 11.8 | ns |
| $t_{RPWH}$ | Min. Pulse Width High (FO = 64) | 4.1 | | 4.5 | | 5.4 | | 6.1 | | 8.2 | | ns |
| $t_{RPWL}$ | Min. Pulse Width Low (FO = 64) | 4.1 | | 4.5 | | 5.4 | | 6.1 | | 8.2 | | ns |
| $t_{RCKSW}$ | Maximum Skew (FO = 128) | | 1.2 | | 1.4 | | 1.6 | | 1.8 | | 1.8 | ns |
| $t_{RP}$ | Minimum Period (FO = 64) | 8.3 | | 9.3 | | 11.1 | | 12.5 | | 16.7 | | ns |
| $f_{RMAX}$ | Maximum Frequency (FO = 64) | | 120 | | 105 | | 90 | | 80 | | 60 | MHz |
| **Clock-to-Clock Skews** | | | | | | | | | | | | |
| $t_{IOHCKSW}$ | I/O Clock to H-Clock Skew | 0.0 | 2.6 | 0.0 | 2.7 | 0.0 | 2.9 | 0.0 | 3.0 | 0.0 | 3.0 | ns |
| $t_{IORCKSW}$ | I/O Clock to R-Clock Skew (FO = 64)<br>(FO = 216) | 0.0<br>0.0 | 1.7<br>5.0 | 0.0<br>0.0 | 1.7<br>5.0 | 0.0<br>0.0 | 1.7<br>5.0 | 0.0<br>0.0 | 1.7<br>5.0 | 0.0<br>0.0 | 5.0<br>5.0 | ns |
| $t_{HRCKSW}$ | H-Clock to R-Clock Skew (FO = 64)<br>(FO = 216) | 0.0<br>0.0 | 1.3<br>3.0 | 0.0<br>0.0 | 1.0<br>3.0 | 0.0<br>0.0 | 1.0<br>3.0 | 0.0<br>0.0 | 1.0<br>3.0 | 0.0<br>0.0 | 1.0<br>3.0 | ns |

*Notes:*

1. *The –2 and –3 speed grades have been discontinued. Refer to PDN 0104, PDN 0203, PDN 0604, and PDN 1004 at http://www.microsemi.com/soc/support/notifications/default.aspx#pdn.*
2. *Delays based on 35 pF loading.*

# 3 – Package Pin Assignments

## PL84




*Note: This is the top view of the package.*

### *Note*

For Package Manufacturing and Environmental information, visit the Resource Center at http://www.microsemi.com/soc/products/solutions/package/docs.aspx.

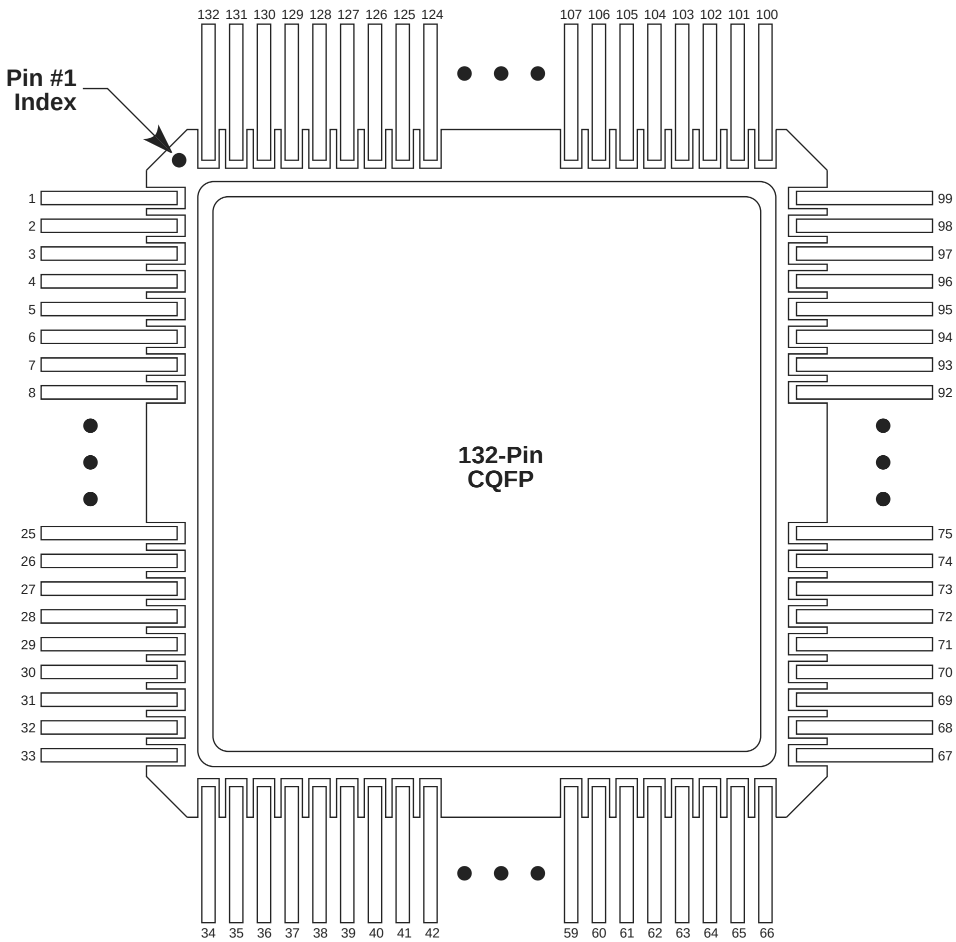
| PQ160 | | | |
|---|---|---|---|
| **Pin Number** | **A1425, A14V25 Function** | **A1440, A14V40 Function** | **A1460, A14V60 Function** |
| 1 | GND | GND | GND |
| 2 | SDI, I/O | SDI, I/O | SDI, I/O |
| 5 | NC | I/O | I/O |
| 9 | MODE | MODE | MODE |
| 10 | VCC | VCC | VCC |
| 14 | NC | I/O | I/O |
| 15 | GND | GND | GND |
| 18 | VCC | VCC | VCC |
| 19 | GND | GND | GND |
| 20 | NC | I/O | I/O |
| 24 | NC | I/O | I/O |
| 27 | NC | I/O | I/O |
| 28 | VCC | VCC | VCC |
| 29 | VCC | VCC | VCC |
| 40 | GND | GND | GND |
| 41 | NC | I/O | I/O |
| 43 | NC | I/O | I/O |
| 45 | NC | I/O | I/O |
| 46 | VCC | VCC | VCC |
| 47 | NC | I/O | I/O |
| 49 | NC | I/O | I/O |
| 51 | NC | I/O | I/O |
| 53 | NC | I/O | I/O |
| 58 | PRB, I/O | PRB, I/O | PRB, I/O |
| 59 | GND | GND | GND |
| 60 | VCC | VCC | VCC |
| 62 | HCLK, I/O | HCLK, I/O | HCLK, I/O |
| 63 | GND | GND | GND |
| 74 | NC | I/O | I/O |
| 75 | VCC | VCC | VCC |
| 76 | NC | I/O | I/O |
| 77 | NC | I/O | I/O |
| 78 | NC | I/O | I/O |
| 79 | SDO | SDO | SDO |
| 80 | IOPCL, I/O | IOPCL, I/O | IOPCL, I/O |
| 81 | GND | GND | GND |
| 90 | VCC | VCC | VCC |
| 91 | VCC | VCC | VCC |

| PQ160 | | | |
|---|---|---|---|
| **Pin Number** | **A1425, A14V25 Function** | **A1440, A14V40 Function** | **A1460, A14V60 Function** |
| 92 | NC | I/O | I/O |
| 93 | NC | I/O | I/O |
| 98 | GND | GND | GND |
| 99 | VCC | VCC | VCC |
| 100 | NC | I/O | I/O |
| 103 | GND | GND | GND |
| 107 | NC | I/O | I/O |
| 109 | NC | I/O | I/O |
| 110 | VCC | VCC | VCC |
| 111 | GND | GND | GND |
| 112 | VCC | VCC | VCC |
| 113 | NC | I/O | I/O |
| 119 | NC | I/O | I/O |
| 120 | IOCLK, I/O | IOCLK, I/O | IOCLK, I/O |
| 121 | GND | GND | GND |
| 124 | NC | I/O | I/O |
| 127 | NC | I/O | I/O |
| 136 | CLKA, I/O | CLKA, I/O | CLKA, I/O |
| 137 | CLKB, I/O | CLKB, I/O | CLKB, I/O |
| 138 | VCC | VCC | VCC |
| 139 | GND | GND | GND |
| 140 | VCC | VCC | VCC |
| 141 | GND | GND | GND |
| 142 | PRA, I/O | PRA, I/O | PRA, I/O |
| 143 | NC | I/O | I/O |
| 145 | NC | I/O | I/O |
| 147 | NC | I/O | I/O |
| 149 | NC | I/O | I/O |
| 151 | NC | I/O | I/O |
| 153 | NC | I/O | I/O |
| 154 | VCC | VCC | VCC |
| 160 | DCLK, I/O | DCLK, I/O | DCLK, I/O |

*Notes:*

1. All unlisted pin numbers are user I/Os.
2. NC denotes no connection.
3. MODE should be terminated to GND through a 10K resistor to enable Actionprobe usage; otherwise it can be terminated directly to GND.

# CQ132




*Note: This is the top view*

## *Note*

For Package Manufacturing and Environmental information, visit the Resource Center at http://www.microsemi.com/soc/products/solutions/package/docs.aspx

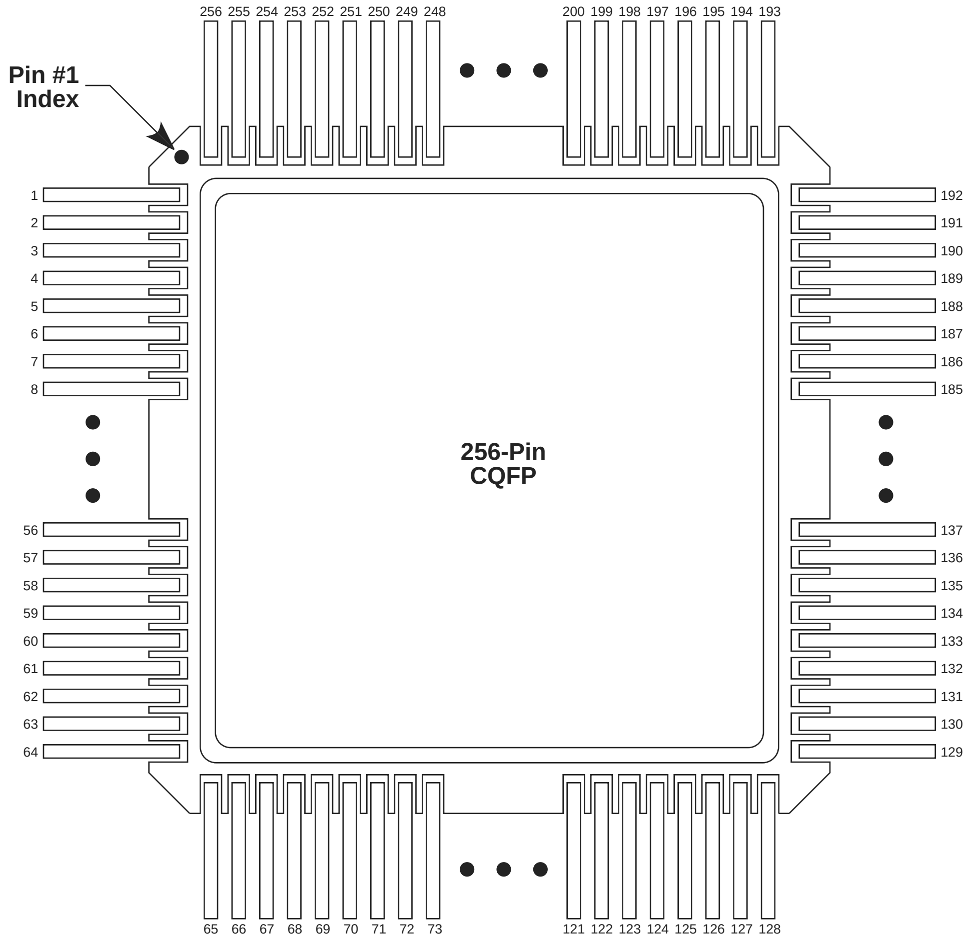
| CQ196 | |
|---|---|
| **Pin Number** | **A1460 Function** |
| 1 | GND |
| 2 | SDI, I/O |
| 11 | MODE |
| 12 | VCC |
| 13 | GND |
| 37 | GND |
| 38 | VCC |
| 39 | VCC |
| 51 | GND |
| 52 | GND |
| 59 | VCC |
| 64 | GND |
| 77 | HCLK, I/O |
| 79 | PRB, I/O |
| 86 | GND |
| 94 | VCC |
| 98 | GND |
| 99 | SDO |
| 100 | IOPCL, I/O |

| CQ196 | |
|---|---|
| **Pin Number** | **A1460 Function** |
| 101 | GND |
| 110 | VCC |
| 111 | VCC |
| 112 | GND |
| 137 | VCC |
| 138 | GND |
| 139 | GND |
| 140 | VCC |
| 148 | IOCLK, I/O |
| 149 | GND |
| 155 | VCC |
| 162 | GND |
| 172 | CLKA, I/O |
| 173 | CLKB, I/O |
| 174 | PRA, I/O |
| 183 | GND |
| 189 | VCC |
| 193 | GND |
| 196 | DCLK, I/O |

*Notes:*

1. All unlisted pin numbers are user I/Os.
2. NC denotes no connection.
3. MODE should be terminated to GND through a 10K resistor to enable Actionprobe usage; otherwise it can be terminated directly to GND.

# CQ256

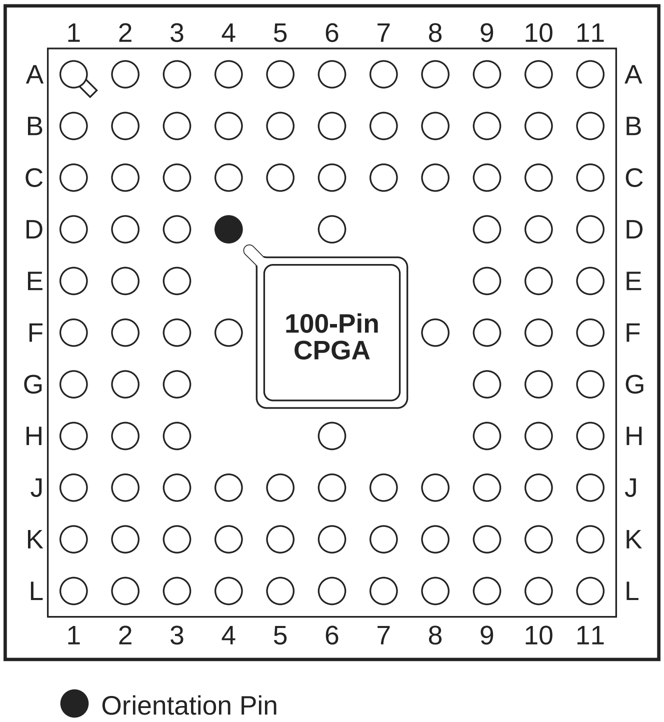



*Note: This is the top view.*

## *Note*

For Package Manufacturing and Environmental information, visit the Resource Center at http://www.microsemi.com/soc/products/solutions/package/docs.aspx

# PG100




*Note: This is the top view.*

## *Note*

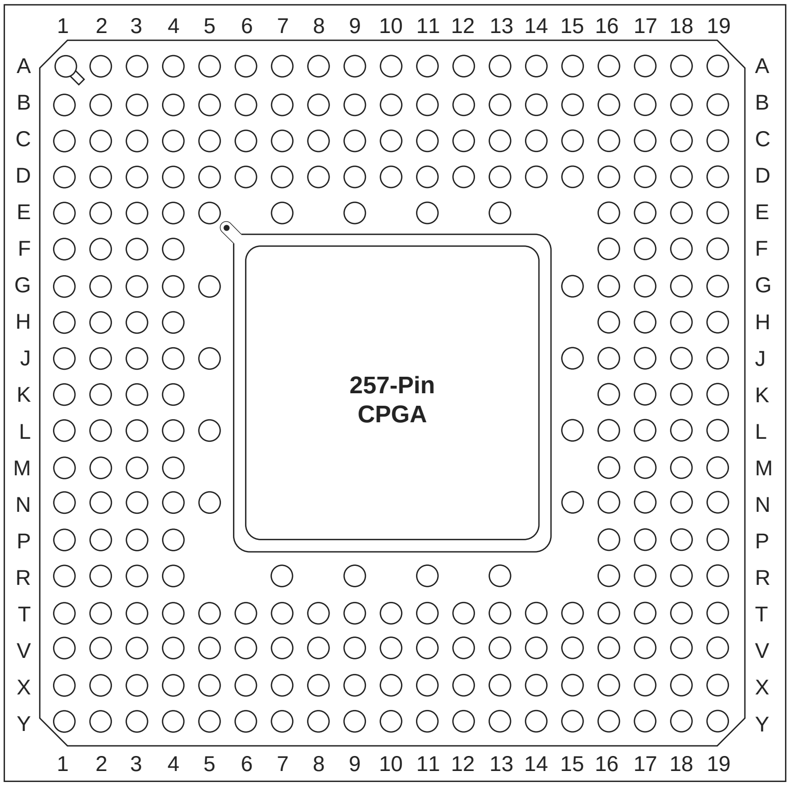
For Package Manufacturing and Environmental information, visit the Resource Center at http://www.microsemi.com/soc/products/solutions/package/docs.aspx

| PG100 | |
|---|---|
| **A1415 Function** | **Location** |
| CLKA or I/O | C7 |
| CLKB or I/O | D6 |
| DCLK or I/O | C4 |
| GND | C3, C6, C9, E9, F3, F9, J3, J6, J8, J9 |
| HCLK or I/O | H6 |
| IOCLK or I/O | C10 |
| IOPCL or I/O | K9 |
| MODE | C2 |
| PRA or I/O | A6 |
| PRB or I/O | L3 |
| SDI or I/O | B3 |
| SDO | L9 |
| VCC | B6, B10, E11, F2, F10, G2, K2, K6, K10 |

*Notes:*

1. All unlisted pin numbers are user I/Os.
2. NC denotes no connection.
3. MODE should be terminated to GND through a 10K resistor to enable Actionprobe usage; otherwise it can be terminated directly to GND.
4. The PG100 package has been discontinued.

# PG257




*Note: This is the top view.*

## *Note*

For Package Manufacturing and Environmental information, visit the Resource Center at http://www.microsemi.com/soc/products/solutions/package/docs.aspx