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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	200
Number of Logic Elements/Cells	-
Total RAM Bits	-
Number of I/O	80
Number of Gates	1500
Voltage - Supply	4.5V ~ 5.5V
Mounting Type	Surface Mount
Operating Temperature	-55°C ~ 125°C (TC)
Package / Case	100-BQFP
Supplier Device Package	100-PQFP (20x14)
Purchase URL	https://www.e-xfl.com/product-detail/microsemi/a1415a-pqg100m

Device/Package	Speed Grade[1]				Application[1]			
	Std.	–1	–2	–3	C	I	M	B
A14V40A Device								
84-Pin Plastic Leaded Chip Carrier (PLCC)	✓	–	–	–	✓	–	–	–
100-Pin Very Thin Quad Flatpack (VQFP)	✓	–	–	–	✓	–	–	–
160-Pin Plastic Quad Flatpack (PQFP)	✓	–	–	–	✓	–	–	–
176-Pin Thin Quad Flatpack (TQFP)	✓	–	–	–	✓	–	–	–
A1460A Device								
160-Pin Plastic Quad Flatpack (PQFP)	✓	✓	D	D	✓	✓	–	–
176-Pin Thin Quad Flatpack (TQFP)	✓	✓	D	D	✓	✓	–	–
196-Pin Ceramic Quad Flatpack (CQFP)	✓	✓	–	–	✓	–	✓	✓
207-Pin Ceramic Pin Grid Array (CPGA)	✓	✓	D	D	✓	–	✓	✓
208-Pin Plastic Quad Flatpack (PQFP)	✓	✓	D	D	✓	✓	–	–
225-Pin Plastic Ball Grid Array (BGA)	D	D	D	D	D	–	–	–
A14V60A Device								
160-Pin Plastic Quad Flatpack (PQFP)	✓	–	–	–	✓	–	–	–
176-Pin Thin Quad Flatpack (TQFP)	✓	–	–	–	✓	–	–	–
208-Pin Plastic Quad Flatpack (PQFP)	✓	–	–	–	✓	–	–	–
A14100A Device								
208-Pin Power Quad Flatpack (RQFP)	✓	✓	D	D	✓	✓	–	–
257-Pin Ceramic Pin Grid Array (CPGA)	✓	✓	D	D	✓	–	✓	✓
313-Pin Plastic Ball Grid Array (BGA)	✓	✓	D	D	✓	–	–	–
256-Pin Ceramic Quad Flatpack (CQFP)	✓	✓	–	–	✓	–	✓	✓
A14V100A Device								
208-Pin Power Quad Flatpack (RQFP)	✓	–	–	–	✓	–	–	–
313-Pin Plastic Ball Grid Array (BGA)	✓	–	–	–	✓	–	–	–

Notes:
1. *Applications:*
   C = Commercial
   I = Industrial
   M = Military
2. *Commercial only*

Availability:
✓ = Available
P = Planned
– = Not planned
D = Discontinued

Speed Grade:
–1 = Approx. 15% faster than Std.
–2 = Approx. 25% faster than Std.
–3 = Approx. 35% faster than Std.
(–2 and –3 speed grades have been discontinued.)

***Table 1-1* • Chip-to-Chip Performance (worst-case commercial)**

Device and Speed Grade	t_{CKHS} (ns)	t_{TRACE} (ns)	t_{INSU} (ns)	Total (ns)	MHz
A1425A -3	7.5	1.0	1.8	10.3	97
A1460A -3	9.0	1.0	1.3	11.3	88
A1425A -2	7.5	1.0	2.0	10.5	95
A1460A -2	9.0	1.0	1.5	11.5	87
A1425A -1	9.0	1.0	2.3	12.3	81
A1460A -1	10.0	1.0	1.8	12.8	78
A1425A STD	10.0	1.0	2.7	13.7	73
A1460A STD	11.5	1.0	2.0	14.5	69

Note: The –2 and –3 speed grades have been discontinued. Refer to PDN 0104, PDN 0203, PDN 0604, and PDN 1004 at http://www.microsemi.com/soc/support/notifications/default.aspx#pdn.

The I/O module output Y is used to bring Pad signals into the array or to feed the output register back into the array. This allows the output register to be used in high-speed state machine applications. Side I/O modules have a dedicated output segment for Y extending into the routing channels above and below (similar to logic modules). Top/Bottom I/O modules have no dedicated output segment. Signals coming into the chip from the top or bottom are routed using F-fuses and LVTs (F-fuses and LVTs are explained in detail in the routing section).

I/O Pad Drivers

All pad drivers are capable of being tristate. Each buffer connects to an associated I/O module with four signals: OE (Output Enable), IE (Input Enable), DataOut, and DataIn. Certain special signals used only during programming and test also connect to the pad drivers: OUTEN (global output enable), INEN (global input enable), and SLEW (individual slew selection). See Figure 2-5.

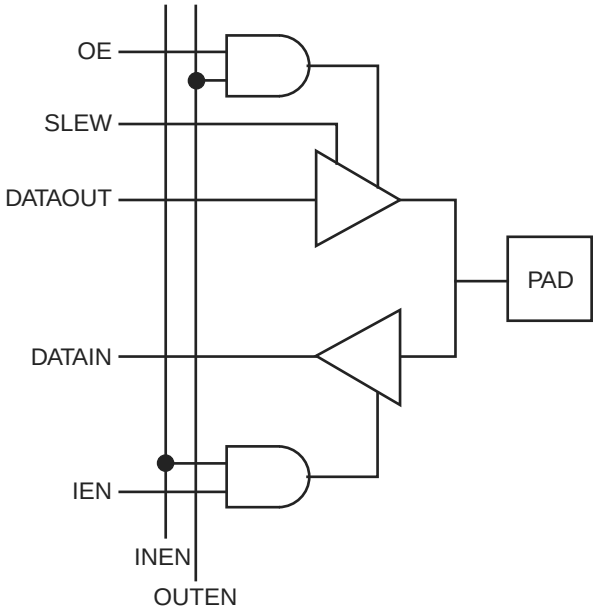


Figure 2-5 • **Function Diagram for I/O Pad Driver**

Special I/Os

The special I/Os are of two types: temporary and permanent. Temporary special I/Os are used during programming and testing. They function as normal I/Os when the MODE pin is inactive. Permanent special I/Os are user programmed as either normal I/Os or special I/Os. Their function does not change once the device has been programmed. The permanent special I/Os consist of the array clock input buffers (CLKA and CLKB), the hard-wired array clock input buffer (HCLK), the hard-wired I/O clock input buffer (IOCLK), and the hard-wired I/O register preset/clear input buffer (IOPCL). Their function is determined by the I/O macros selected.

Clock Networks

The ACT 3 architecture contains four clock networks: two high-performance dedicated clock networks and two general purpose routed networks. The high-performance networks function up to 200 MHz, while the general purpose routed networks function up to 150 MHz.

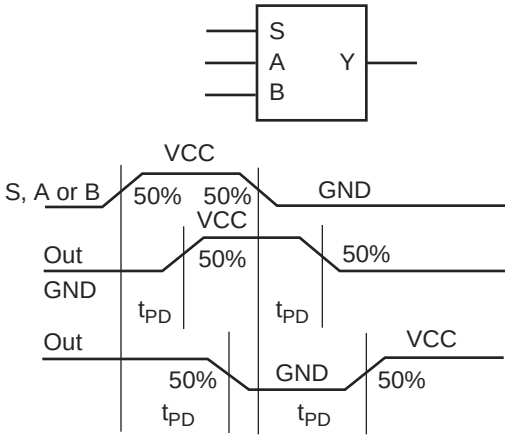


Figure 2-14 • **Module Delays**

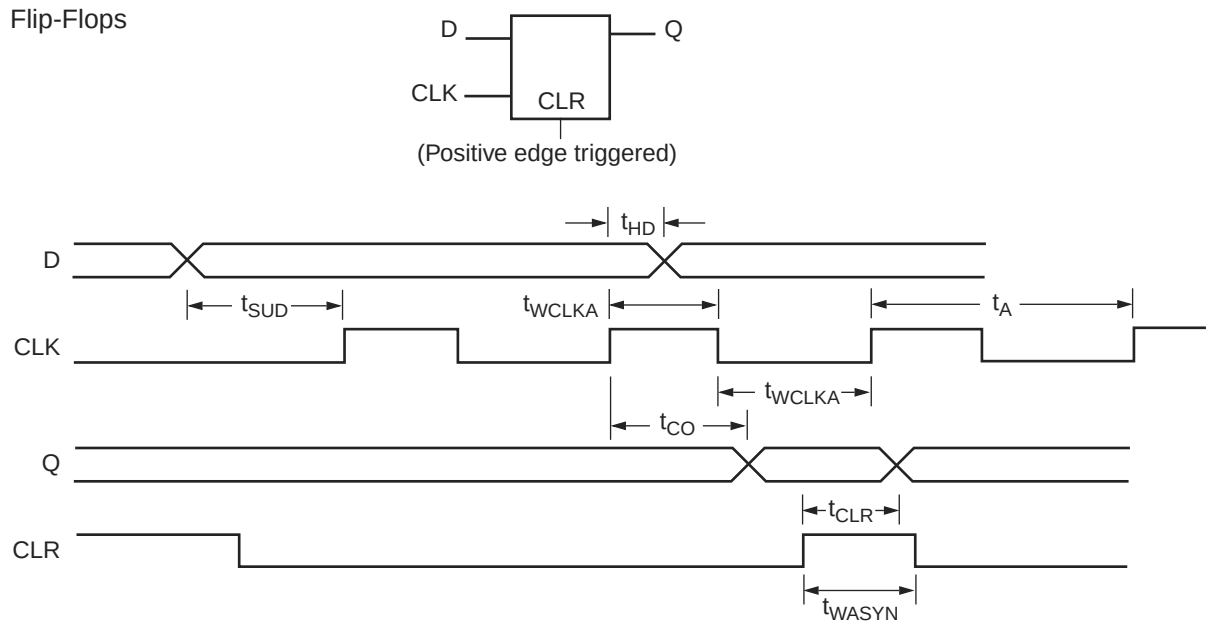


Figure 2-15 • **Sequential Module Timing Characteristics**

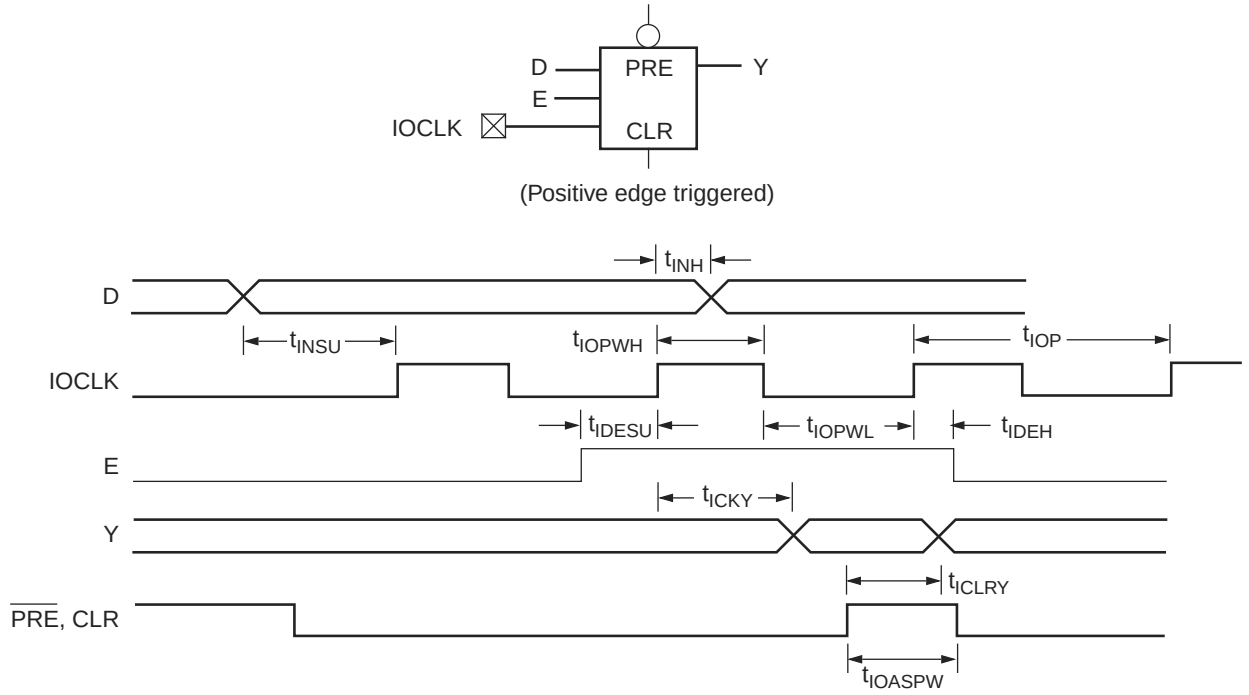


Figure 2-16 • **I/O Module: Sequential Input Timing Characteristics**

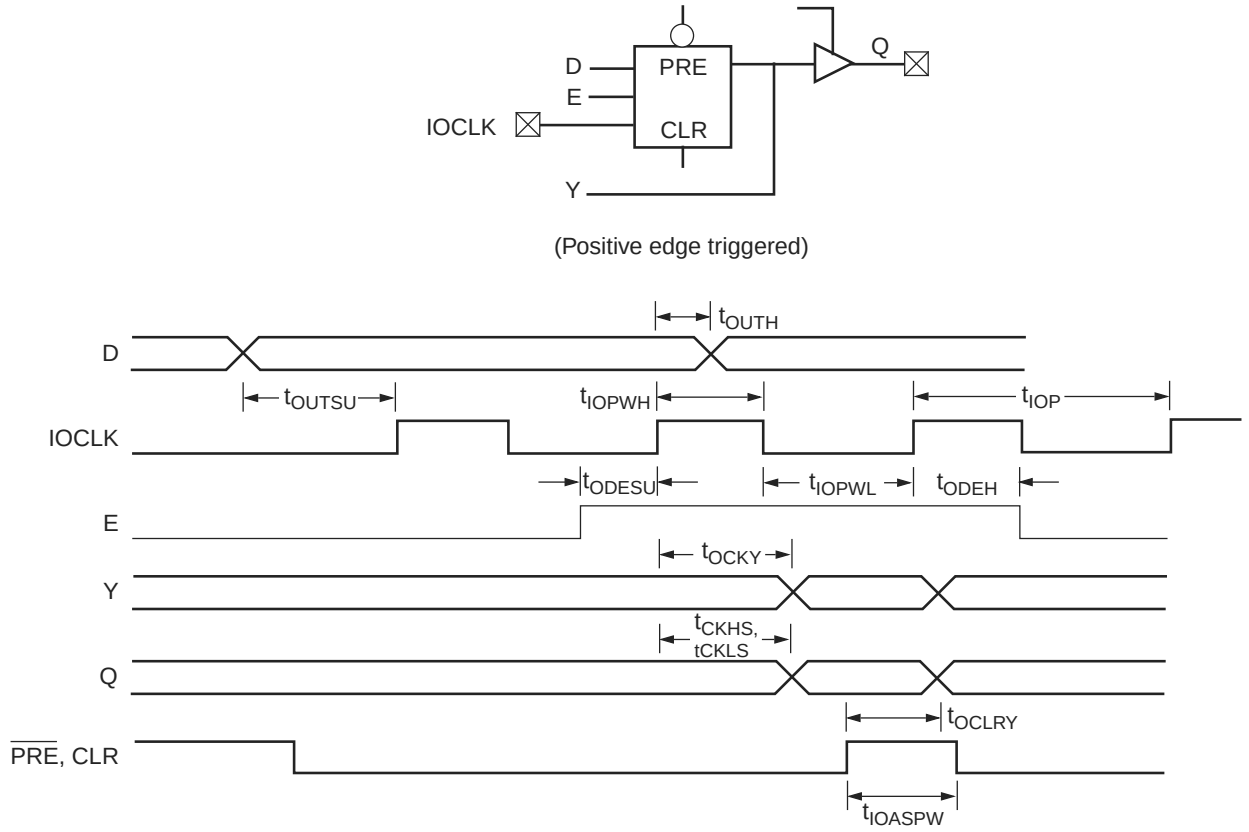


Figure 2-17 • **I/O Module: Sequential Output Timing Characteristics**

A1415A, A14V15A Timing Characteristics (continued)

Table 2-20 • A1415A, A14V15A Worst-Case Commercial Conditions, VCC = 4.75 V, T_J = 70°C

I/O Module – TTL Output Timing[1]		–3 Speed[2]		–2 Speed[2]		–1 Speed		Std. Speed		3.3 V Speed[1]		Units
Parameter/Description		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t_{DHS}	Data to Pad, High Slew		5.0		5.6		6.4		7.5		9.8	ns
t_{DLS}	Data to Pad, Low Slew		8.0		9.0		10.2		12.0		15.6	ns
t_{ENZHS}	Enable to Pad, Z to H/L, High Slew		4.0		4.5		5.1		6.0		7.8	ns
t_{ENZLS}	Enable to Pad, Z to H/L, Low Slew		7.4		8.3		9.4		11.0		14.3	ns
t_{ENHSZ}	Enable to Pad, H/L to Z, High Slew		6.5		7.5		8.5		10.0		13.0	ns
t_{ENLSZ}	Enable to Pad, H/L to Z, Low Slew		6.5		7.5		8.5		10.0		13.0	ns
t_{CKHS}	IOCLK Pad to Pad H/L, High Slew		7.5		7.5		9.0		10.0		13.0	ns
t_{CKLS}	IOCLK Pad to Pad H/L, Low Slew		11.3		11.3		13.5		15.0		19.5	ns
d_{TLHHS}	Delta Low to High, High Slew		0.02		0.02		0.03		0.03		0.04	ns/pF
d_{TLHLS}	Delta Low to High, Low Slew		0.05		0.05		0.06		0.07		0.09	ns/pF
d_{THLHS}	Delta High to Low, High Slew		0.04		0.04		0.04		0.05		0.07	ns/pF
d_{THLLS}	Delta High to Low, Low Slew		0.05		0.05		0.06		0.07		0.09	ns/pF
I/O Module – CMOS Output Timing[1]												
t_{DHS}	Data to Pad, High Slew		6.2		7.0		7.9		9.3		12.1	ns
t_{DLS}	Data to Pad, Low Slew		11.7		13.1		14.9		17.5		22.8	ns
t_{ENZHS}	Enable to Pad, Z to H/L, High Slew		5.2		5.9		6.6		7.8		10.1	ns
t_{ENZLS}	Enable to Pad, Z to H/L, Low Slew		8.9		10.0		11.3		13.3		17.3	ns
t_{ENHSZ}	Enable to Pad, H/L to Z, High Slew		6.7		7.5		8.5		10.0		13.0	ns
t_{ENLSZ}	Enable to Pad, H/L to Z, Low Slew		6.7		7.5		9.0		10.0		13.0	ns
t_{CKHS}	IOCLK Pad to Pad H/L, High Slew		8.9		8.9		10.7		11.8		15.3	ns
t_{CKLS}	IOCLK Pad to Pad H/L, Low Slew		13.0		13.0		15.6		17.3		22.5	ns
d_{TLHHS}	Delta Low to High, High Slew		0.04		0.04		0.05		0.06		0.08	ns/pF
d_{TLHLS}	Delta Low to High, Low Slew		0.07		0.08		0.09		0.11		0.14	ns/pF
d_{THLHS}	Delta High to Low, High Slew		0.03		0.03		0.03		0.04		0.05	ns/pF
d_{THLLS}	Delta High to Low, Low Slew		0.04		0.04		0.04		0.05		0.07	ns/pF

Notes:

1. *Delays based on 35 pF loading.*
2. *The –2 and –3 speed grades have been discontinued. Please refer to the Product Discontinuation Notices (PDNs) listed below:*

   PDN March 2001
   PDN 0104
   PDN 0203
   PDN 0604
   PDN 1004

A1425A, A14V25A Timing Characteristics (continued)

***Table 2-23* • A1425A, A14V25A Worst-Case Commercial Conditions, VCC = 4.75 V, T_J = 70°C**

I/O Module Input Propagation Delays		–3 Speed[1]		–2 Speed[1]		–1 Speed		Std. Speed		3.3 V Speed[1]		Units
Parameter/Description		**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	
t_{INY}	Input Data Pad to Y		2.8		3.2		3.6		4.2		5.5	ns
t_{ICKY}	Input Reg IOCLK Pad to Y		4.7		5.3		6.0		7.0		9.2	ns
t_{OCKY}	Output Reg IOCLK Pad to Y		4.7		5.3		6.0		7.0		9.2	ns
t_{ICLRY}	Input Asynchronous Clear to Y		4.7		5.3		6.0		7.0		9.2	ns
t_{OCLRY}	Output Asynchronous Clear to Y		4.7		5.3		6.0		7.0		9.2	ns
Predicted Input Routing Delays[2]												
t_{RD1}	FO = 1 Routing Delay		0.9		1.0		1.1		1.3		1.7	ns
t_{RD2}	FO = 2 Routing Delay		1.2		1.4		1.6		1.8		2.4	ns
t_{RD3}	FO = 3 Routing Delay		1.4		1.6		1.8		2.1		2.8	ns
t_{RD4}	FO = 4 Routing Delay		1.7		1.9		2.2		2.5		3.3	ns
t_{RD8}	FO = 8 Routing Delay		2.8		3.2		3.6		4.2		5.5	ns
I/O Module Sequential Timing (wrt IOCLK pad)												
t_{INH}	Input F-F Data Hold	0.0		0.0		0.0		0.0		0.0		ns
t_{INSU}	Input F-F Data Setup	1.8		2.0		2.3		2.7		3.0		ns
t_{IDEH}	Input Data Enable Hold	0.0		0.0		0.0		0.0		0.0		ns
t_{IDESU}	Input Data Enable Setup	5.8		6.5		7.5		8.6		8.6		ns
t_{OUTH}	Output F-F Data hold	0.7		0.8		0.9		1.0		1.0		ns
t_{OUTSU}	Output F-F Data Setup	0.7		0.8		0.9		1.0		1.0		ns
t_{ODEH}	Output Data Enable Hold	0.3		0.4		0.4		0.5		0.5		ns
f_{ODESU}	Output Data Enable Setup	1.3		1.5		1.7		2.0		2.0		ns

*Notes: **

1. *The –2 and –3 speed grades have been discontinued. Refer to PDN 0104, PDN 0203, PDN 0604, and PDN 1004 at http://www.microsemi.com/soc/support/notifications/default.aspx#pdn.*
2. *Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual worst-case performance. Post-route timing is based on actual routing delay measurements performed on the device prior to shipment.*

A1440A, A14V40A Timing Characteristics (continued)

Table 2-29 • **A1440A, A14V40A Worst-Case Commercial Conditions, VCC = 4.75 V, T_J = 70°C**

Dedicated (hardwired) I/O Clock Network		–3 Speed[1]		–2 Speed[1]		–1 Speed		Std. Speed		3.3 V Speed[1]		Units
Parameter/Description		**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	
t_{IOCKH}	Input Low to High (pad to I/O module input)		2.0		2.3		2.6		3.0		3.5	ns
t_{IOPWH}	Minimum Pulse Width High	1.9		2.4		3.3		3.8		4.8		ns
t_{IPOWL}	Minimum Pulse Width Low	1.9		2.4		3.3		3.8		4.8		ns
t_{IOSAPW}	Minimum Asynchronous Pulse Width	1.9		2.4		3.3		3.8		4.8		ns
t_{IOCKSW}	Maximum Skew		0.4		0.4		0.4		0.4		0.4	ns
t_{IOP}	Minimum Period	4.0		5.0		6.8		8.0		10.0		ns
f_{IOMAX}	Maximum Frequency		250		200		150		125		100	MHz
Dedicated (hardwired) Array Clock												
t_{HCKH}	Input Low to High (pad to S-module input)		3.0		3.4		3.9		4.5		5.5	ns
t_{HCKL}	Input High to Low (pad to S-module input)		3.0		3.4		3.9		4.5		5.5	ns
t_{HPWH}	Minimum Pulse Width High	1.9		2.4		3.3		3.8		4.8		ns
t_{HPWL}	Minimum Pulse Width Low	1.9		2.4		3.3		3.8		4.8		ns
t_{HCKSW}	Delta High to Low, Low Slew		0.3		0.3		0.3		0.3		0.3	ns
t_{HP}	Minimum Period	4.0		5.0		6.8		8.0		10.0		ns
f_{HMAX}	Maximum Frequency		250		200		150		125		100	MHz
Routed Array Clock Networks												
t_{RCKH}	Input Low to High (FO = 64)		3.7		4.1		4.7		5.5		9.0	ns
t_{RCKL}	Input High to Low (FO = 64)		4.0		4.5		5.1		6.0		9.0	ns
t_{RPWH}	Min. Pulse Width High (FO = 64)	3.3		3.8		4.2		4.9		6.5		ns
t_{RPWL}	Min. Pulse Width Low (FO = 64)	3.3		3.8		4.2		4.9		6.5		ns
t_{RCKSW}	Maximum Skew (FO = 128)		0.7		0.8		0.9		1.0		1.0	ns
t_{RP}	Minimum Period (FO = 64)	6.8		8.0		8.7		10.0		13.4		ns
f_{RMAX}	Maximum Frequency (FO = 64)		150		125		115		100		75	MHz
Clock-to-Clock Skews												
$t_{IOHCKSW}$	I/O Clock to H-Clock Skew	0.0	1.7	0.0	1.8	0.0	2.0	0.0	2.2	0.0	3.0	ns
$t_{IORCKSW}$	I/O Clock to R-Clock Skew (FO = 64) (FO = 144)	0.0 0.0	1.0 3.0	0.0 0.0	1.0 3.0	0.0 0.0	1.0 3.0	0.0 0.0	1.0 3.0	0.0 0.0	3.0 3.0	ns
t_{HRCKSW}	H-Clock to R-Clock Skew (FO = 64) (FO = 144)	0.0 0.0	1.0 3.0	0.0 0.0	1.0 3.0	0.0 0.0	1.0 3.0	0.0 0.0	1.0 3.0	0.0 0.0	1.0 3.0	ns

Notes:

1. *The –2 and –3 speed grades have been discontinued. Refer to PDN 0104, PDN 0203, PDN 0604, and PDN 1004 at http://www.microsemi.com/soc/support/notifications/default.aspx#pdn.*
2. *Delays based on 35 pF loading.*

A1460A, A14V60A Timing Characteristics (continued)

***Table 2-31* • A1460A, A14V60A Worst-Case Commercial Conditions, VCC = 4.75 V, T_J = 70°C**

I/O Module Input Propagation Delays		–3 Speed[1]		–2 Speed[1]		–1 Speed		Std. Speed		3.3 V Speed[1]		Units
Parameter/Description		**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	
t_{INY}	Input Data Pad to Y		2.8		3.2		3.6		4.2		5.5	ns
t_{ICKY}	Input Reg IOCLK Pad to Y		4.7		5.3		6.0		7.0		9.2	ns
t_{OCKY}	Output Reg IOCLK Pad to Y		4.7		5.3		6.0		7.0		9.2	ns
t_{ICLRY}	Input Asynchronous Clear to Y		4.7		5.3		6.0		7.0		9.2	ns
t_{OCLRY}	Output Asynchronous Clear to Y		4.7		5.3		6.0		7.0		9.2	ns
Predicted Input Routing Delays[2]												
t_{RD1}	FO = 1 Routing Delay		0.9		1.0		1.1		1.3		1.7	ns
t_{RD2}	FO = 2 Routing Delay		1.2		1.4		1.6		1.8		2.4	ns
t_{RD3}	FO = 3 Routing Delay		1.4		1.6		1.8		2.1		2.8	ns
t_{RD4}	FO = 4 Routing Delay		1.7		1.9		2.2		2.5		3.3	ns
t_{RD8}	FO = 8 Routing Delay		2.8		3.2		3.6		4.2		5.5	ns
I/O Module Sequential Timing (wrt IOCLK pad)												
t_{INH}	Input F-F Data Hold	0.0		0.0		0.0		0.0		0.0		ns
t_{INSU}	Input F-F Data Setup	1.3		1.5		1.8		2.0		2.0		ns
t_{IDEH}	Input Data Enable Hold	0.0		0.0		0.0		0.0		0.0		ns
t_{IDESU}	Input Data Enable Setup	5.8		6.5		7.5		8.6		8.6		ns
t_{OUTH}	Output F-F Data hold	0.7		0.8		0.9		1.0		1.0		ns
t_{OUTSU}	Output F-F Data Setup	0.7		0.8		0.9		1.0		1.0		ns
t_{ODEH}	Output Data Enable Hold	0.3		0.4		0.4		0.5		0.5		ns
f_{ODESU}	Output Data Enable Setup	1.3		1.5		1.7		2.0		2.0		ns

Notes:

5. *The –2 and –3 speed grades have been discontinued. Refer to PDN 0104, PDN 0203, PDN 0604, and PDN 1004 at http://www.microsemi.com/soc/support/notifications/default.aspx#pdn.*
6. *Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual worst-case performance. Post-route timing is based on actual routing delay measurements performed on the device prior to shipment.*

A14100A, A14V100A Timing Characteristics (continued)

Table 2-36 • A14100A, A14V100A Worst-Case Commercial Conditions, VCC = 4.75 V, T_J = 70°C

I/O Module – TTL Output Timing[1]		–3 Speed[2]		–2 Speed[2]		–1 Speed		Std. Speed		3.3 V Speed[1]		Units
Parameter/Description		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t_{DHS}	Data to Pad, High Slew		5.0		5.6		6.4		7.5		9.8	ns
t_{DLS}	Data to Pad, Low Slew		8.0		9.0		10.2		12.0		15.6	ns
t_{ENZHS}	Enable to Pad, Z to H/L, High Slew		4.0		4.5		5.1		6.0		7.8	ns
t_{ENZLS}	Enable to Pad, Z to H/L, Low Slew		7.4		8.3		9.4		11.0		14.3	ns
t_{ENHSZ}	Enable to Pad, H/L to Z, High Slew		8.0		9.0		10.2		12.0		15.6	ns
t_{ENLSZ}	Enable to Pad, H/L to Z, Low Slew		7.4		8.3		9.4		11.0		14.3	ns
t_{CKHS}	IOCLK Pad to Pad H/L, High Slew		9.5		9.5		10.5		12.0		15.6	ns
t_{CKLS}	IOCLK Pad to Pad H/L, Low Slew		12.8		12.8		15.3		17.0		22.1	ns
d_{TLHHS}	Delta Low to High, High Slew		0.02		0.02		0.03		0.03		0.04	ns/pF
d_{TLHLS}	Delta Low to High, Low Slew		0.05		0.05		0.06		0.07		0.09	ns/pF
d_{THLHS}	Delta High to Low, High Slew		0.04		0.04		0.04		0.05		0.07	ns/pF
d_{THLLS}	Delta High to Low, Low Slew		0.05		0.05		0.06		0.07		0.09	ns/pF
I/O Module – CMOS Output Timing[1]												
t_{DHS}	Data to Pad, High Slew		6.2		7.0		7.9		9.3		12.1	ns
t_{DLS}	Data to Pad, Low Slew		11.7		13.1		14.9		17.5		22.8	ns
t_{ENZHS}	Enable to Pad, Z to H/L, High Slew		5.2		5.9		6.6		7.8		10.1	ns
t_{ENZLS}	Enable to Pad, Z to H/L, Low Slew		8.9		10.0		11.3		13.3		17.3	ns
t_{ENHSZ}	Enable to Pad, H/L to Z, High Slew		8.0		9.0		10.0		12.0		15.6	ns
t_{ENLSZ}	Enable to Pad, H/L to Z, Low Slew		7.4		8.3		9.4		11.0		14.3	ns
t_{CKHS}	IOCLK Pad to Pad H/L, High Slew		10.4		10.4		12.4		13.8		17.9	ns
t_{CKLS}	IOCLK Pad to Pad H/L, Low Slew		14.5		14.5		17.4		19.3		25.1	ns
d_{TLHHS}	Delta Low to High, High Slew		0.04		0.04		0.05		0.06		0.08	ns/pF
d_{TLHLS}	Delta Low to High, Low Slew		0.07		0.08		0.09		0.11		0.14	ns/pF
d_{THLHS}	Delta High to Low, High Slew		0.03		0.03		0.03		0.04		0.05	ns/pF
d_{THLLS}	Delta High to Low, Low Slew		0.04		0.04		0.04		0.05		0.07	ns/pF

*Notes: **

1. *Delays based on 35 pF loading.*
2. *The –2 and –3 speed grades have been discontinued. Refer to PDN 0104, PDN 0203, PDN 0604, and PDN 1004 at http://www.microsemi.com/soc/support/notifications/default.aspx#pdn.*

A14100A, A14V100A Timing Characteristics (continued)

Table 2-37 • **A14100A, A14V100A Worst-Case Commercial Conditions, VCC = 4.75 V, T_J = 70°C**

Dedicated (hardwired) I/O Clock Network		–3 Speed[1]		–2 Speed[1]		–1 Speed		Std. Speed		3.3 V Speed[1]		Units
Parameter/Description		**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	
t_{IOCKH}	Input Low to High (pad to I/O module input)		2.3		2.6		3.0		3.5		4.5	ns
t_{IOPWH}	Minimum Pulse Width High	2.4		3.3		3.8		4.8		6.5		ns
t_{IPOWL}	Minimum Pulse Width Low	2.4		3.3		3.8		4.8		6.5		ns
t_{IOSAPW}	Minimum Asynchronous Pulse Width	2.4		3.3		3.8		4.8		6.5		ns
t_{IOCKSW}	Maximum Skew		0.6		0.6		0.7		0.8		0.6	ns
t_{IOP}	Minimum Period	5.0		6.8		8.0		10.0		13.4		ns
f_{IOMAX}	Maximum Frequency		200		150		125		100		75	MHz
Dedicated (hardwired) Array Clock												
t_{HCKH}	Input Low to High (pad to S-module input)		3.7		4.1		4.7		5.5		7.0	ns
t_{HCKL}	Input High to Low (pad to S-module input)		3.7		4.1		4.7		5.5		7.0	ns
t_{HPWH}	Minimum Pulse Width High	2.4		3.3		3.8		4.8		6.5		ns
t_{HPWL}	Minimum Pulse Width Low	2.4		3.3		3.8		4.8		6.5		ns
t_{HCKSW}	Delta High to Low, Low Slew		0.6		0.6		0.7		0.8		0.6	ns
t_{HP}	Minimum Period	5.0		6.8		8.0		10.0		13.4		ns
f_{HMAX}	Maximum Frequency		200		150		125		100		75	MHz
Routed Array Clock Networks												
t_{RCKH}	Input Low to High (FO = 64)		6.0		6.8		7.7		9.0		11.8	ns
t_{RCKL}	Input High to Low (FO = 64)		6.0		6.8		7.7		9.0		11.8	ns
t_{RPWH}	Min. Pulse Width High (FO = 64)	4.1		4.5		5.4		6.1		8.2		ns
t_{RPWL}	Min. Pulse Width Low (FO = 64)	4.1		4.5		5.4		6.1		8.2		ns
t_{RCKSW}	Maximum Skew (FO = 128)		1.2		1.4		1.6		1.8		1.8	ns
t_{RP}	Minimum Period (FO = 64)	8.3		9.3		11.1		12.5		16.7		ns
f_{RMAX}	Maximum Frequency (FO = 64)		120		105		90		80		60	MHz
Clock-to-Clock Skews												
$t_{IOHCKSW}$	I/O Clock to H-Clock Skew	0.0	2.6	0.0	2.7	0.0	2.9	0.0	3.0	0.0	3.0	ns
$t_{IORCKSW}$	I/O Clock to R-Clock Skew (FO = 64) (FO = 350)	0.0 0.0	1.7 5.0	0.0 0.0	1.7 5.0	0.0 0.0	1.7 5.0	0.0 0.0	1.7 5.0	0.0 0.0	5.0 5.0	ns
t_{HRCKSW}	H-Clock to R-Clock Skew (FO = 64) (FO = 350)	0.0 0.0	1.3 3.0	0.0 0.0	1.0 3.0	0.0 0.0	1.0 3.0	0.0 0.0	1.0 3.0	0.0 0.0	1.0 3.0	ns

*Notes: **

1. *The –2 and –3 speed grades have been discontinued. Refer to PDN 0104, PDN 0203, PDN 0604, and PDN 1004 at http://www.microsemi.com/soc/support/notifications/default.aspx#pdn.*
2. *Delays based on 35 pF loading.*

Pin Descriptions

CLKA Clock A (Input)

Clock input for clock distribution networks. The Clock input is buffered prior to clocking the logic modules. This pin can also be used as an I/O.

CLKB Clock B (Input)

Clock input for clock distribution networks. The Clock input is buffered prior to clocking the logic modules. This pin can also be used as an I/O.

GND Ground

LOW supply voltage.

HCLK Dedicated (Hard-wired) Array Clock (Input)

Clock input for sequential modules. This input is directly wired to each S-Module and offers clock speeds independent of the number of S-Modules being driven. This pin can also be used as an I/O.

I/O Input/Output (Input, Output)

The I/O pin functions as an input, output, three-state, or bidirectional buffer. Input and output levels are compatible with standard TTL and CMOS specifications. Unused I/O pins are tristated by the Designer Series software.

IOCLK Dedicated (Hard-wired) I/O Clock (Input)

Clock input for I/O modules. This input is directly wired to each I/O module and offers clock speeds independent of the number of I/O modules being driven. This pin can also be used as an I/O.

IOPCL Dedicated (Hard-wired) I/O Preset/Clear (Input)

Input for I/O preset or clear. This global input is directly wired to the preset and clear inputs of all I/O registers. This pin functions as an I/O when no I/O preset or clear macros are used.

MODE Mode (Input)

The MODE pin controls the use of diagnostic pins (DCLK, PRA, PRB, SDI). When the MODE pin is HIGH, the special functions are active. When the MODE pin is LOW, the pins function as I/Os. To provide Actionprobe capability, the MODE pin should be terminated to GND through a 10K resistor so that the MODE pin can be pulled high when required.

NC No Connection

This pin is not connected to circuitry within the device.

PRA Probe A (Output)

The Probe A pin is used to output data from any user-defined design node within the device. This independent diagnostic pin can be used in conjunction with the Probe B pin to allow real-time diagnostic output of any signal path within the device. The Probe A pin can be used as a user-defined I/O when debugging has been completed. The pin's probe capabilities can be permanently disabled to protect programmed design confidentiality. PRA is accessible when the MODE pin is HIGH. This pin functions as an I/O when the MODE pin is LOW.

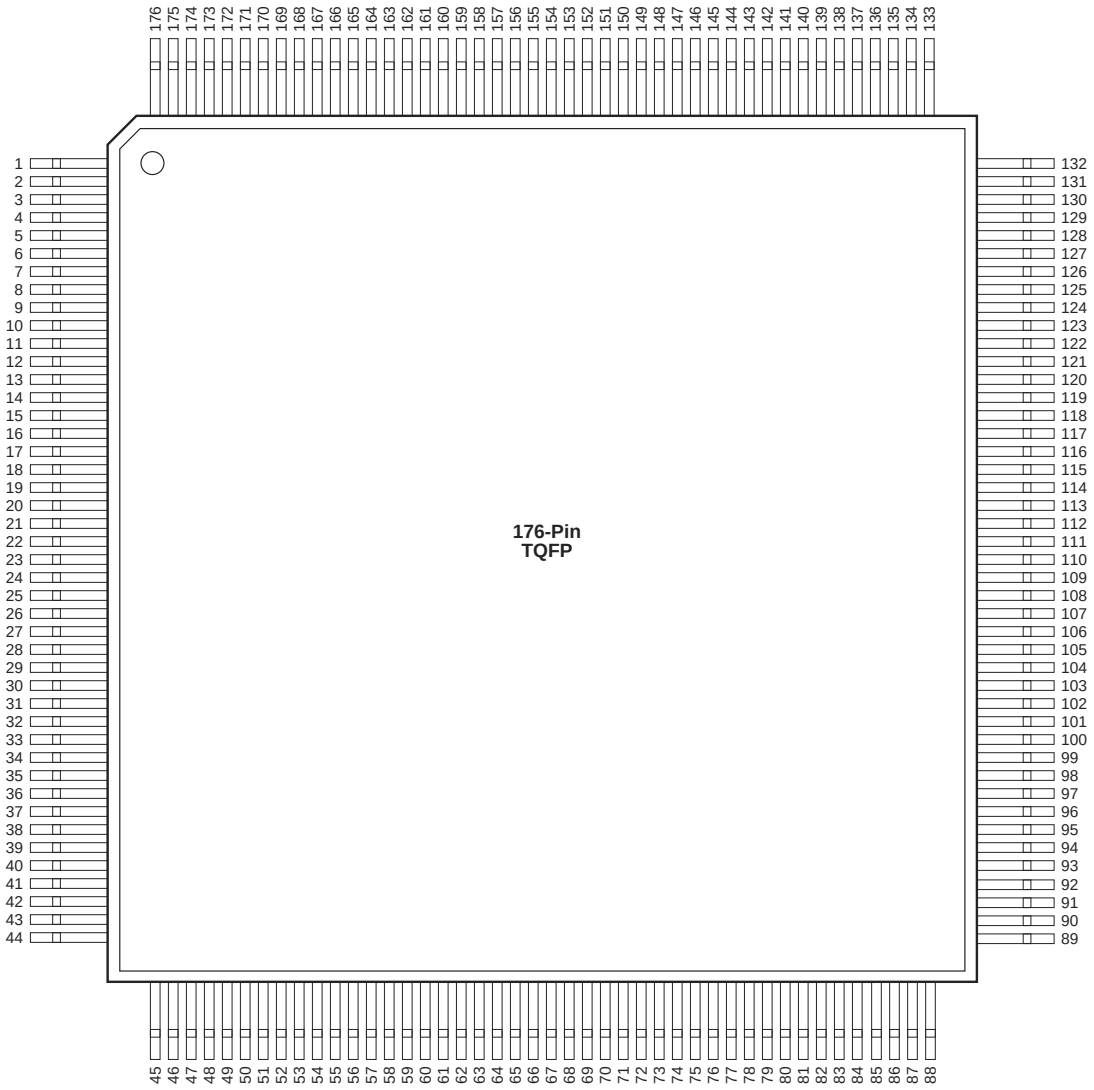
PRB Probe B (Output)

The Probe B pin is used to output data from any user-defined design node within the device. This independent diagnostic pin can be used in conjunction with the Probe A pin to allow real-time diagnostic output of any signal path within the device. The Probe B pin can be used as a user-defined I/O when debugging has been completed. The pin's probe capabilities can be permanently disabled to protect programmed design confidentiality. PRB is accessible when the MODE pin is HIGH. This pin functions as an I/O when the MODE pin is LOW.

SDI Serial Data Input (Input)

Serial data input for diagnostic probe and device programming. SDI is active when the MODE pin is HIGH. This pin functions as an I/O when the MODE pin is LOW.

TQ176



Note: This is the top view.

Note

For Package Manufacturing and Environmental information, visit the Resource Center at http://www.microsemi.com/soc/products/solutions/package/docs.aspx

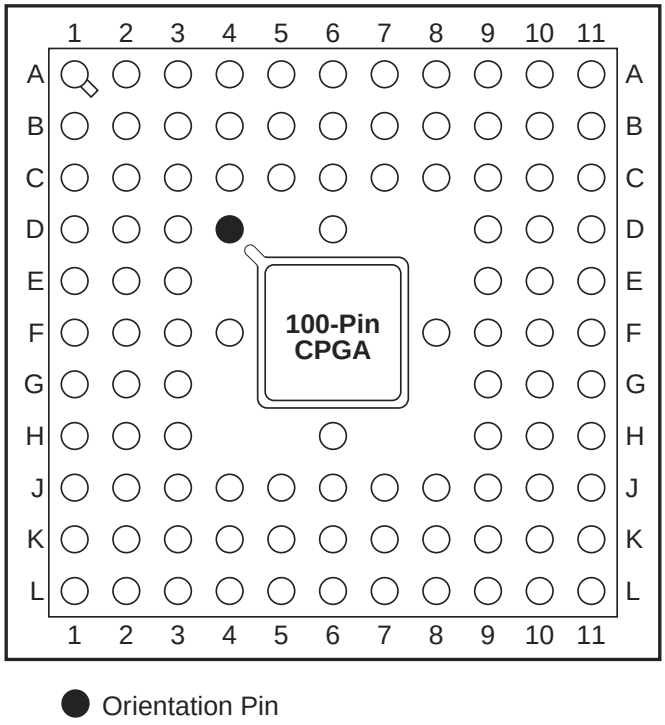
CQ196	
Pin Number	**A1460 Function**
1	GND
2	SDI, I/O
11	MODE
12	VCC
13	GND
37	GND
38	VCC
39	VCC
51	GND
52	GND
59	VCC
64	GND
77	HCLK, I/O
79	PRB, I/O
86	GND
94	VCC
98	GND
99	SDO
100	IOPCL, I/O

CQ196	
Pin Number	**A1460 Function**
101	GND
110	VCC
111	VCC
112	GND
137	VCC
138	GND
139	GND
140	VCC
148	IOCLK, I/O
149	GND
155	VCC
162	GND
172	CLKA, I/O
173	CLKB, I/O
174	PRA, I/O
183	GND
189	VCC
193	GND
196	DCLK, I/O

Notes:

1. All unlisted pin numbers are user I/Os.
2. NC denotes no connection.
3. MODE should be terminated to GND through a 10K resistor to enable Actionprobe usage; otherwise it can be terminated directly to GND.

PG100



Note: This is the top view.

Note

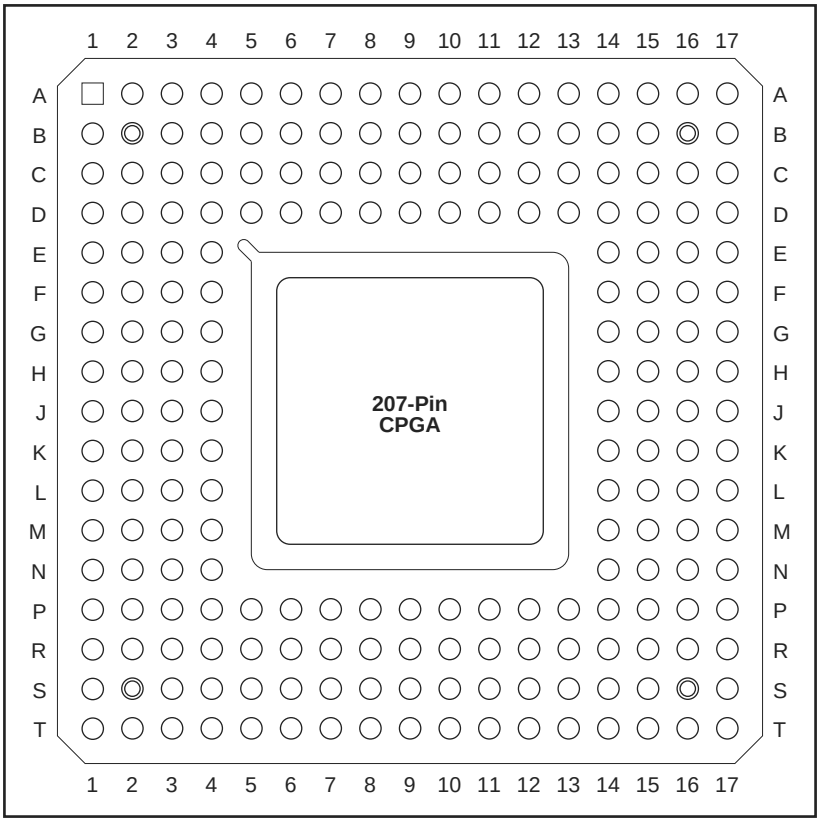
For Package Manufacturing and Environmental information, visit the Resource Center at http://www.microsemi.com/soc/products/solutions/package/docs.aspx

PG175	
A1440 Function	**Location**
CLKA or I/O	C9
CLKB or I/O	A9
DCLK or I/O	D5
GND	D4, D8, D11, D12, E4, E14, H4, H12, L4, L12, M4, M8, M12
HCLK or I/O	R8
IOCLK or I/O	E12
IOPCL or I/O	P13
MODE	F3
NC	A1, A2, A15, B2, B3, P2, P14, R1, R2, R14, R15
PRA or I/O	B8
PRB or I/O	R7
SDI or I/O	D3
SDO	N12
VCC	C3, C8, C13, E15, H3, H13, L1, L14, N3, N8, N13

Notes:

1. All unlisted pin numbers are user I/Os.
2. NC denotes no connection.
3. MODE should be terminated to GND through a 10K resistor to enable Actionprobe usage; otherwise it can be terminated directly to GND.
4. The PG175 package has been discontinued.

PG207



Note: This is the top view.

Note

For Package Manufacturing and Environmental information, visit the Resource Center at http://www.microsemi.com/soc/products/solutions/package/docs.aspx

PG207	
A1460 Function	**Location**
CLKA or I/O	K1
CLKB or I/O	J3
DCLK or I/O	E4
GND	C14, D4, D5, D9, D14, J4, J14, P3, P4, P7, P9, P14, R15
HCLK or I/O	J15
IOCLK or I/O	P5
IOPCL or I/O	N14
MODE	D7
NC	A1, A2, A16, A17, B1, B17, C1, C2, S1, S3, S17, T1, T2, T16, T17
PRA or I/O	H1
PRB or I/O	K16
SDI or I/O	C3
SDO	P15
VCC	B2, B9, B16, D11, J2, J16, P12, S2, S9, S16, T5

Notes:

1. All unlisted pin numbers are user I/Os.
2. NC denotes no connection.
3. MODE should be terminated to GND through a 10K resistor to enable Actionprobe usage; otherwise it can be terminated directly to GND.

Revision	Changes	Page
Revision 2 (continued)	In the "Package Pin Assignments" section, notes were added to the pin tables for the following packages, stating that they are discontinued: "BG225" "PG100" "PG133" "PG175"	 3-20 3-24 3-26 3-28
Revision 1 (June 2006)	RoHS compliant information was added to the "Ordering Information" section.	II