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### Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

### Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

#### Details

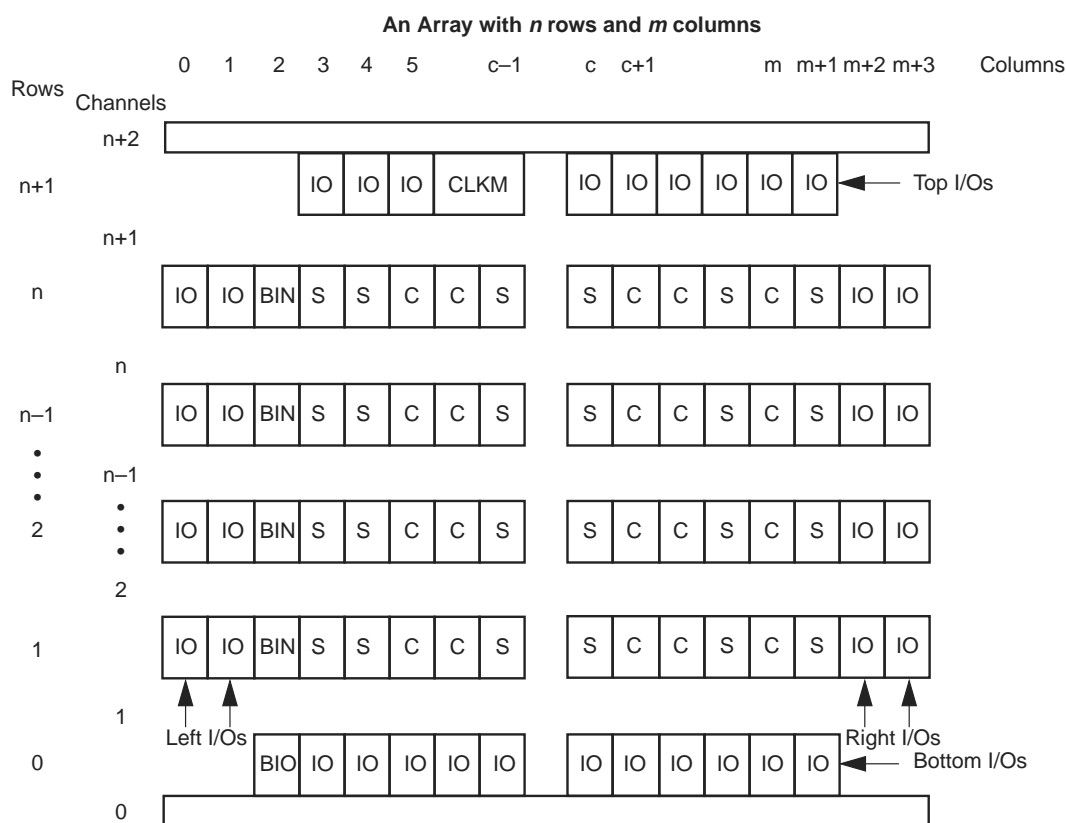
Product Status	Obsolete
Number of LABs/CLBs	200
Number of Logic Elements/Cells	-
Total RAM Bits	-
Number of I/O	80
Number of Gates	1500
Voltage - Supply	4.5V ~ 5.5V
Mounting Type	Surface Mount
Operating Temperature	-55°C ~ 125°C (TC)
Package / Case	100-TQFP
Supplier Device Package	100-VQFP (14x14)
Purchase URL	<a href="https://www.e-xfl.com/product-detail/microsemi/a1415a-vq100m">https://www.e-xfl.com/product-detail/microsemi/a1415a-vq100m</a>

## 2 – Detailed Specifications

This section of the datasheet is meant to familiarize the user with the architecture of the ACT 3 family of FPGA devices. A generic description of the family will be presented first, followed by a detailed description of the logic blocks, the routing structure, the antifuses, and the special function circuits. The on-chip circuitry required to program the devices is not covered.

### Topology

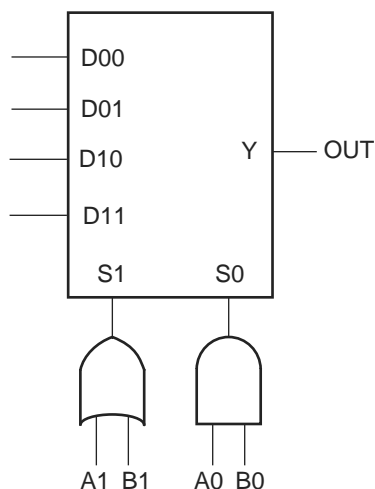
The ACT 3 family architecture is composed of six key elements: Logic modules, I/O modules, I/O Pad Drivers, Routing Tracks, Clock Networks, and Programming and Test Circuits. The basic structure is similar for all devices in the family, differing only in the number of rows, columns, and I/Os. The array itself consists of alternating rows of modules and channels. The logic modules and channels are in the center of the array; the I/O modules are located along the array periphery. A simplified floor plan is depicted in Figure 2-1.



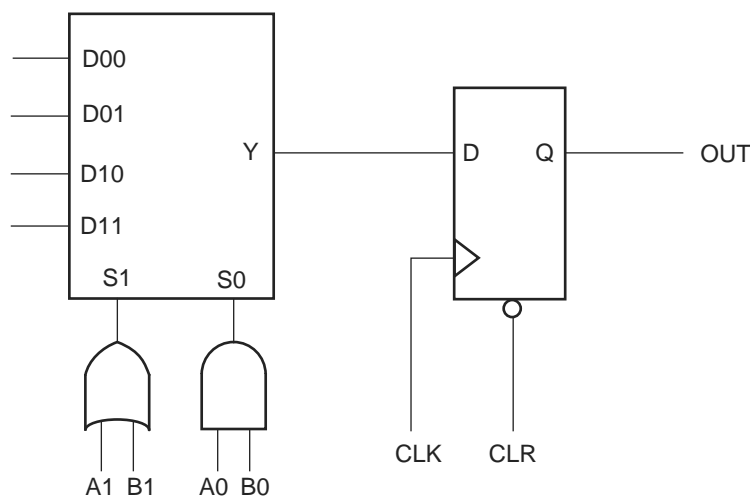
**Figure 2-1 • Generalized Floor Plan of ACT 3 Device**

## Logic Modules

ACT 3 logic modules are enhanced versions of the 1200XL family logic modules. As in the 1200XL family, there are two types of modules: C-modules and S-modules (Figure 2-2 and Figure 2-3). The C-module is functionally equivalent to the 1200XL C-module and implements high fanin combinatorial macros, such as 5-input AND, 5-input OR, and so on. It is available for use as the CM8 hard macro. The S-module is designed to implement high-speed sequential functions within a single module.



**Figure 2-2 • C-Module Diagram**



**Figure 2-3 • S-Module Diagram**

S-modules consist of a full C-module driving a flip-flop, which allows an additional level of logic to be implemented without additional propagation delay. It is available for use as the DFM8A/B and DLM8A/B hard macros. C-modules and S-modules are arranged in pairs called module-pairs. Module-pairs are arranged in alternating patterns and make up the bulk of the array. This arrangement allows the placement software to support two-module macros of four types (CC, CS, SC, and SS). The C-module implements the following function:

$$Y = !S1 * !S0 * D00 + !S1 * S0 * D01 + S1 * !S0 * D10 + S1 * S0 * D11$$

*EQ 1*

where:  $S0 = A0 * B0$  and  $S1 = A1 + B1$

## Package Thermal Characteristics

The device junction to case thermal characteristic is  $\theta_{jc}$ , and the junction to ambient air characteristic is  $\theta_{ja}$ . The thermal characteristics for  $\theta_{ja}$  are shown with two different air flow rates.

Maximum junction temperature is 150°C.

A sample calculation of the absolute maximum power dissipation allowed for a CPGA 175-pin package at commercial temperature and still air is as follows:

$$\frac{\text{Max. junction temp. (°C)} - \text{Max. ambient temp. (°C)}}{\theta_{ja} \text{ °C/W}} = \frac{150^{\circ}\text{C} - 70^{\circ}\text{C}}{25^{\circ}\text{C/W}} = 3.2 \text{ W}$$

EQ 2

**Table 2-8 • Package Thermal Characteristics**

Package Type*	Pin Count	$\theta_{jc}$	$\theta_{ja}$ Still Air	$\theta_{ja}$ 300 ft./min.	Units
Ceramic Pin Grid Array	100	20	35	17	°C/W
	133	20	30	15	°C/W
	175	20	25	14	°C/W
	207	20	22	13	°C/W
	257	20	15	8	°C/W
Ceramic Quad Flatpack	132	13	55	30	°C/W
	196	13	36	24	°C/W
	256	13	30	18	°C/W
Plastic Quad Flatpack	100	13	51	40	°C/W
	160	10	33	26	°C/W
	208	10	33	26	°C/W
Very Thin Quad Flatpack	100	12	43	35	°C/W
Thin Quad Flatpack	176	11	32	25	°C/W
Power Quad Flatpack	208	0.4	17	13	°C/W
Plastic Leaded Chip Carrier	84	12	37	28	°C/W
Plastic Ball Grid Array	225	10	25	19	°C/W
	313	10	23	17	°C/W

Note: Maximum power dissipation in still air:

PQ160 = 2.4 W

PQ208 = 2.4 W

PQ100 = 1.6 W

VQ100 = 1.9 W

TQ176 = 2.5 W

PL84 = 2.2 W

RQ208 = 4.7 W

BG225 = 3.2 W

BG313 = 3.5 W

## Power Dissipation

$$P = [ICC_{\text{standby}} + I_{\text{active}}] * VCC * IOL * VOL * N + IOH * (VCC - VOH) * M$$

EQ 3

where:

ICC standby is the current flowing when no inputs or outputs are changing

Iactive is the current flowing due to CMOS switching.

IOL and IOH are TTL sink/source current.

VOL and VOH are TTL level output voltages.

N is the number of outputs driving TTL loads to VOL.

M equals the number of outputs driving TTL loads to VOH.

An accurate determination of N and M is problematical because their values depend on the design and on the system I/O. The power can be divided into two components: static and active.

## Static Power Component

Microsemi FPGAs have small static power components that result in lower power dissipation than PALs or PLDs. By integrating multiple PALs/PLDs into one FPGA, an even greater reduction in board-level power dissipation can be achieved.

The power due to standby current is typically a small component of the overall power. Standby power is calculated in Table 2-9 for commercial, worst case conditions.

**Table 2-9 • Standby Power Calculation**

ICC	VCC	Power
2 mA	5.25 V	10.5 mW

The static power dissipated by TTL loads depends on the number of outputs driving high or low and the DC load current. Again, this value is typically small. For instance, a 32-bit bus sinking 4 mA at 0.33 V will generate 42 mW with all outputs driving low, and 140 mW with all outputs driving high. The actual dissipation will average somewhere between as I/Os switch states with time.

## Active Power Component

Power dissipation in CMOS devices is usually dominated by the active (dynamic) power dissipation. This component is frequency dependent, a function of the logic and the external I/O. Active power dissipation results from charging internal chip capacitances of the interconnect, unprogrammed antifuses, module inputs, and module outputs, plus external capacitance due to PC board traces and load device inputs.

An additional component of the active power dissipation is the totem-pole current in CMOS transistor pairs. The net effect can be associated with an equivalent capacitance that can be combined with frequency and voltage to represent active power dissipation.

## Equivalent Capacitance

The power dissipated by a CMOS circuit can be expressed by EQ 4.

$$\text{Power } (\mu\text{W}) = C_{\text{EQ}} * VCC^2 * F$$

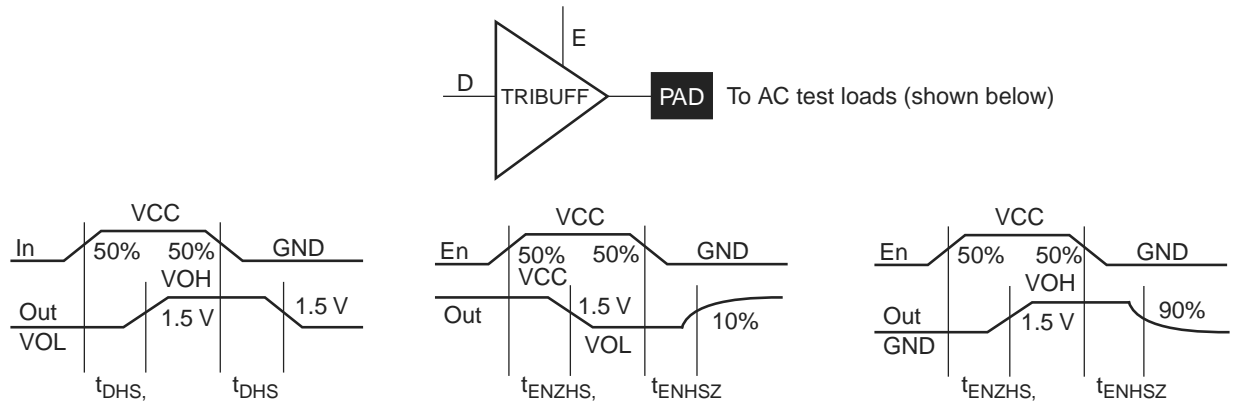
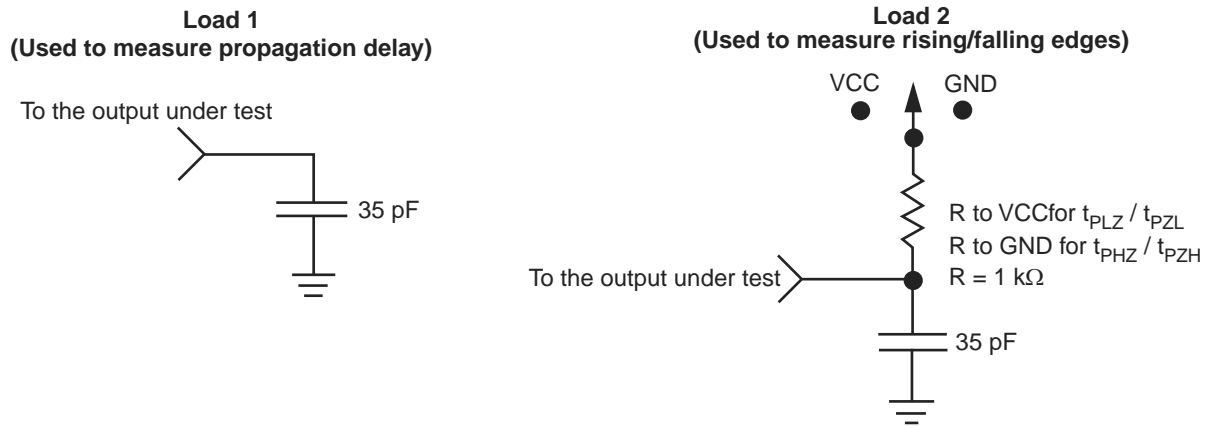
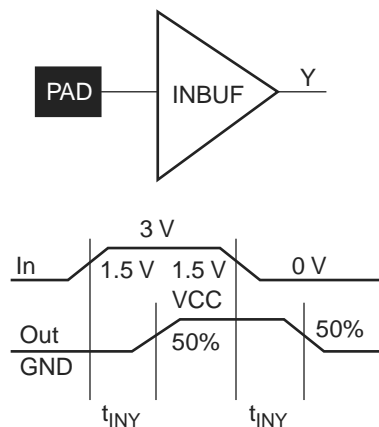
EQ 4

Where:

C<sub>EQ</sub> is the equivalent capacitance expressed in pF.

VCC is the power supply in volts.

F is the switching frequency in MHz.


**Figure 2-11 • Output Buffers**

**Figure 2-12 • AC Test Loads**

**Figure 2-13 • Input Buffer Delays**

## Timing Derating

ACT 3 devices are manufactured in a CMOS process. Therefore, device performance varies according to temperature, voltage, and process variations. Minimum timing parameters reflect maximum operating voltage, minimum operating temperature, and best-case processing. Maximum timing parameters reflect minimum operating voltage, maximum operating temperature, and worst-case processing.

**Table 2-15 • Timing Derating Factor (Temperature and Voltage)**

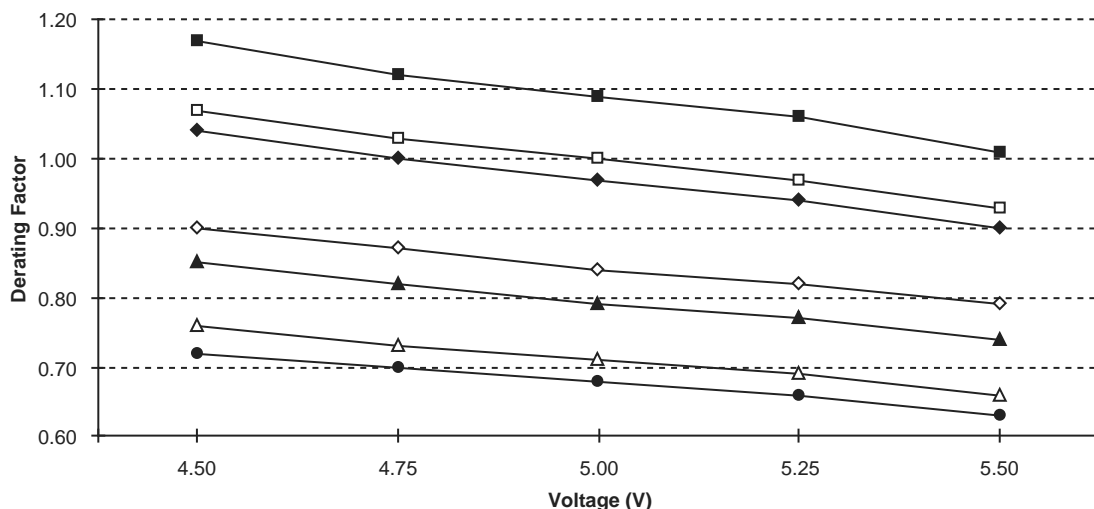
(Commercial Minimum/Maximum Specification) x	Industrial		Military	
	Min.	Max.	Min.	Max.
	0.66	1.07	0.63	1.17

**Table 2-16 • Timing Derating Factor for Designs at Typical Temperature ( $T_J = 25^\circ\text{C}$ ) and Voltage (5.0 V)**

(Commercial Maximum Specification) x	0.85
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**Table 2-17 • Temperature and Voltage Derating Factors (normalized to Worst-Case Commercial,  $T_J = 4.75\text{ V}$ ,  $70^\circ\text{C}$ )**

	-55	-40	0	25	70	85	125
<b>4.50</b>	0.72	0.76	0.85	0.90	1.04	1.07	1.117
<b>4.75</b>	0.70	0.73	0.82	0.87	1.00	1.03	1.12
<b>5.00</b>	0.68	0.71	0.79	0.84	0.97	1.00	1.09
<b>5.25</b>	0.66	0.69	0.77	0.82	0.94	0.97	1.06
<b>5.50</b>	0.63	0.66	0.74	0.79	0.90	0.93	1.01



Note: This derating factor applies to all routing and propagation delays.

**Figure 2-18 • Junction Temperature and Voltage Derating Curves (normalized to Worst-Case Commercial,  $T_J = 4.75\text{ V}$ ,  $70^\circ\text{C}$ )**

## A1415A, A14V15A Timing Characteristics (continued)

Table 2-20 • A1415A, A14V15A Worst-Case Commercial Conditions, VCC = 4.75 V, T<sub>J</sub> = 70°C

I/O Module – TTL Output Timing <sup>1</sup>		–3 Speed <sup>2</sup>		–2 Speed <sup>2</sup>		–1 Speed		Std. Speed		3.3 V Speed <sup>1</sup>		Units
Parameter/Description		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t <sub>DHS</sub>	Data to Pad, High Slew		5.0		5.6		6.4		7.5		9.8	ns
t <sub>DLS</sub>	Data to Pad, Low Slew		8.0		9.0		10.2		12.0		15.6	ns
t <sub>ENZHS</sub>	Enable to Pad, Z to H/L, High Slew		4.0		4.5		5.1		6.0		7.8	ns
t <sub>ENZLS</sub>	Enable to Pad, Z to H/L, Low Slew		7.4		8.3		9.4		11.0		14.3	ns
t <sub>ENHSZ</sub>	Enable to Pad, H/L to Z, High Slew		6.5		7.5		8.5		10.0		13.0	ns
t <sub>ENLSZ</sub>	Enable to Pad, H/L to Z, Low Slew		6.5		7.5		8.5		10.0		13.0	ns
t <sub>CKHS</sub>	IOCLK Pad to Pad H/L, High Slew		7.5		7.5		9.0		10.0		13.0	ns
t <sub>CKLS</sub>	IOCLK Pad to Pad H/L, Low Slew		11.3		11.3		13.5		15.0		19.5	ns
d <sub>TLHHS</sub>	Delta Low to High, High Slew		0.02		0.02		0.03		0.03		0.04	ns/pF
d <sub>TLHLS</sub>	Delta Low to High, Low Slew		0.05		0.05		0.06		0.07		0.09	ns/pF
d <sub>THLHS</sub>	Delta High to Low, High Slew		0.04		0.04		0.04		0.05		0.07	ns/pF
d <sub>THLLS</sub>	Delta High to Low, Low Slew		0.05		0.05		0.06		0.07		0.09	ns/pF
I/O Module – CMOS Output Timing <sup>1</sup>												
t <sub>DHS</sub>	Data to Pad, High Slew		6.2		7.0		7.9		9.3		12.1	ns
t <sub>DLS</sub>	Data to Pad, Low Slew		11.7		13.1		14.9		17.5		22.8	ns
t <sub>ENZHS</sub>	Enable to Pad, Z to H/L, High Slew		5.2		5.9		6.6		7.8		10.1	ns
t <sub>ENZLS</sub>	Enable to Pad, Z to H/L, Low Slew		8.9		10.0		11.3		13.3		17.3	ns
t <sub>ENHSZ</sub>	Enable to Pad, H/L to Z, High Slew		6.7		7.5		8.5		10.0		13.0	ns
t <sub>ENLSZ</sub>	Enable to Pad, H/L to Z, Low Slew		6.7		7.5		9.0		10.0		13.0	ns
t <sub>CKHS</sub>	IOCLK Pad to Pad H/L, High Slew		8.9		8.9		10.7		11.8		15.3	ns
t <sub>CKLS</sub>	IOCLK Pad to Pad H/L, Low Slew		13.0		13.0		15.6		17.3		22.5	ns
d <sub>TLHHS</sub>	Delta Low to High, High Slew		0.04		0.04		0.05		0.06		0.08	ns/pF
d <sub>TLHLS</sub>	Delta Low to High, Low Slew		0.07		0.08		0.09		0.11		0.14	ns/pF
d <sub>THLHS</sub>	Delta High to Low, High Slew		0.03		0.03		0.03		0.04		0.05	ns/pF
d <sub>THLLS</sub>	Delta High to Low, Low Slew		0.04		0.04		0.04		0.05		0.07	ns/pF

**Notes:**

- Delays based on 35 pF loading.
- The –2 and –3 speed grades have been discontinued. Please refer to the Product Discontinuation Notices (PDNs) listed below:

PDN March 2001  
PDN 0104  
PDN 0203  
PDN 0604  
PDN 1004



## A1425A, A14V25A Timing Characteristics (continued)

**Table 2-25 • A1425A, A14V25A Worst-Case Commercial Conditions, VCC = 4.75 V, T<sub>J</sub> = 70°C**

Dedicated (hardwired) I/O Clock Network		–3 Speed <sup>1</sup>		–2 Speed <sup>1</sup>		–1 Speed		Std. Speed		3.3 V Speed <sup>1</sup>		Units
Parameter/Description		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t <sub>IOCKH</sub>	Input Low to High (pad to I/O module input)		2.0		2.3		2.6		3.0		3.5	ns
t <sub>IOPWH</sub>	Minimum Pulse Width High	1.9		2.4		3.3		3.8		4.8		ns
t <sub>IPOWL</sub>	Minimum Pulse Width Low	1.9		2.4		3.3		3.8		4.8		ns
t <sub>IOSAPW</sub>	Minimum Asynchronous Pulse Width	1.9		2.4		3.3		3.8		4.8		ns
t <sub>IOCKSW</sub>	Maximum Skew		0.4		0.4		0.4		0.4		0.4	ns
t <sub>IOP</sub>	Minimum Period	4.0		5.0		6.8		8.0		10.0		ns
f <sub>IOMAX</sub>	Maximum Frequency		250		200		150		125		100	MHz
<b>Dedicated (hardwired) Array Clock</b>												
t <sub>HCKH</sub>	Input Low to High (pad to S-module input)		3.0		3.4		3.9		4.5		5.5	ns
t <sub>HCKL</sub>	Input High to Low (pad to S-module input)		3.0		3.4		3.9		4.5		5.5	ns
t <sub>HPWH</sub>	Minimum Pulse Width High	1.9		2.4		3.3		3.8		4.8		ns
t <sub>HPWL</sub>	Minimum Pulse Width Low	1.9		2.4		3.3		3.8		4.8		ns
t <sub>HCKSW</sub>	Delta High to Low, Low Slew		0.3		0.3		0.3		0.3		0.3	ns
t <sub>HP</sub>	Minimum Period	4.0		5.0		6.8		8.0		10.0		ns
f <sub>HMAX</sub>	Maximum Frequency		250		200		150		125		100	MHz
<b>Routed Array Clock Networks</b>												
t <sub>RCKH</sub>	Input Low to High (FO = 64)		3.7		4.1		4.7		5.5		9.0	ns
t <sub>RCKL</sub>	Input High to Low (FO = 64)		4.0		4.5		5.1		6.0		9.0	ns
t <sub>RPWH</sub>	Min. Pulse Width High (FO = 64)	3.3		3.8		4.2		4.9		6.5		ns
t <sub>RPWL</sub>	Min. Pulse Width Low (FO = 64)	3.3		3.8		4.2		4.9		6.5		ns
t <sub>RCKSW</sub>	Maximum Skew (FO = 128)		0.7		0.8		0.9		1.0		1.0	ns
t <sub>RP</sub>	Minimum Period (FO = 64)	6.8		8.0		8.7		10.0		13.4		ns
f <sub>RMAX</sub>	Maximum Frequency (FO = 64)		150		125		115		100		75	MHz
<b>Clock-to-Clock Skews</b>												
t <sub>IOHCKSW</sub>	I/O Clock to H-Clock Skew	0.0	1.7	0.0	1.8	0.0	2.0	0.0	2.2	0.0	3.0	ns
t <sub>IORCKSW</sub>	I/O Clock to R-Clock Skew (FO = 64) (FO = 80)	0.0	1.0	0.0	1.0	0.0	1.0	0.0	1.0	0.0	3.0	ns
		0.0	3.0	0.0	3.0	0.0	3.0	0.0	3.0	0.0	3.0	
t <sub>HRCKSW</sub>	H-Clock to R-Clock Skew (FO = 64) (FO = 80)	0.0	1.0	0.0	1.0	0.0	1.0	0.0	1.0	0.0	1.0	ns
		0.0	3.0	0.0	3.0	0.0	3.0	0.0	3.0	0.0	3.0	

**Notes:**

1. The –2 and –3 speed grades have been discontinued. Refer to PDN 0104, PDN 0203, PDN 0604, and PDN 1004 at <http://www.microsemi.com/soc/support/notifications/default.aspx#pdn>.
2. Delays based on 35 pF loading.

## A1460A, A14V60A Timing Characteristics

**Table 2-30 • A1460A, A14V60A Worst-Case Commercial Conditions, VCC = 4.75 V, T<sub>J</sub> = 70°C<sup>1</sup>**

Logic Module Propagation Delays <sup>2</sup>		–3 Speed <sup>3</sup>		–2 Speed <sup>3</sup>		–1 Speed		Std. Speed		3.3 V Speed <sup>1</sup>		Units
Parameter/Description		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t <sub>PD</sub>	Internal Array Module		2.0		2.3		2.6		3.0		3.9	ns
t <sub>CO</sub>	Sequential Clock to Q		2.0		2.3		2.6		3.0		3.9	ns
t <sub>CLR</sub>	Asynchronous Clear to Q		2.0		2.3		2.6		3.0		3.9	ns
<b>Predicted Routing Delays<sup>4</sup></b>												
t <sub>RD1</sub>	FO = 1 Routing Delay		0.9		1.0		1.1		1.3		1.7	ns
t <sub>RD2</sub>	FO = 2 Routing Delay		1.2		1.4		1.6		1.8		2.4	ns
t <sub>RD3</sub>	FO = 3 Routing Delay		1.4		1.6		1.8		2.1		2.8	ns
t <sub>RD4</sub>	FO = 4 Routing Delay		1.7		1.9		2.2		2.5		3.3	ns
t <sub>RD8</sub>	FO = 8 Routing Delay		2.8		3.2		3.6		4.2		5.5	ns
<b>Logic Module Sequential Timing</b>												
t <sub>SUD</sub>	Flip-Flop Data Input Setup	0.5		0.6		0.7		0.8		0.8		ns
t <sub>HD</sub>	Flip-Flop Data Input Hold	0.0		0.0		0.0		0.0		0.0		ns
t <sub>SUD</sub>	Latch Data Input Setup	0.5		0.6		0.7		0.8		0.8		ns
t <sub>HD</sub>	Latch Data Input Hold	0.0		0.0		0.0		0.0		0.0		ns
t <sub>WASYN</sub>	Asynchronous Pulse Width	2.4		3.2		3.8		4.8		6.5		ns
t <sub>WCLKA</sub>	Flip-Flop Clock Pulse Width	2.4		3.2		3.8		4.8		6.5		ns
t <sub>A</sub>	Flip-Flop Clock Input Period	5.0		6.8		8.0		10.0		13.4		ns
f <sub>MAX</sub>	Flip-Flop Clock Frequency		200		150		125		100		75	MHz

**Notes:**

1. VCC = 3.0 V for 3.3 V specifications.
2. For dual-module macros, use t<sub>PD</sub> + t<sub>RD1</sub> + t<sub>PDn</sub> + t<sub>CO</sub> + t<sub>RD1</sub> + t<sub>PDn</sub> or t<sub>PD1</sub> + t<sub>RD1</sub> + t<sub>SUD</sub>, whichever is appropriate.
3. The –2 and –3 speed grades have been discontinued. Refer to PDN 0104, PDN 0203, PDN 0604, and PDN 1004 at <http://www.microsemi.com/soc/support/notifications/default.aspx#pdn>.
4. Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual worst-case performance. Post-route timing is based on actual routing delay measurements performed on the device prior to shipment.

## A14100A, A14V100A Timing Characteristics (continued)

**Table 2-35 • A14100A, A14V100A Worst-Case Commercial Conditions, VCC = 4.75 V, T<sub>J</sub> = 70°C**

I/O Module Input Propagation Delays		–3 Speed <sup>1</sup>		–2 Speed <sup>1</sup>		–1 Speed		Std. Speed		3.3 V Speed <sup>1</sup>		Units
Parameter/Description		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t <sub>INY</sub>	Input Data Pad to Y		2.8		3.2		3.6		4.2		5.5	ns
t <sub>ICKY</sub>	Input Reg IOCLK Pad to Y		4.7		5.3		6.0		7.0		9.2	ns
t <sub>OCKY</sub>	Output Reg IOCLK Pad to Y		4.7		5.3		6.0		7.0		9.2	ns
t <sub>ICLRY</sub>	Input Asynchronous Clear to Y		4.7		5.3		6.0		7.0		9.2	ns
t <sub>OCLRY</sub>	Output Asynchronous Clear to Y		4.7		5.3		6.0		7.0		9.2	ns
<b>Predicted Input Routing Delays<sup>2</sup></b>												
t <sub>RD1</sub>	FO = 1 Routing Delay		0.9		1.0		1.1		1.3		1.7	ns
t <sub>RD2</sub>	FO = 2 Routing Delay		1.2		1.4		1.6		1.8		2.4	ns
t <sub>RD3</sub>	FO = 3 Routing Delay		1.4		1.6		1.8		2.1		2.8	ns
t <sub>RD4</sub>	FO = 4 Routing Delay		1.7		1.9		2.2		2.5		3.3	ns
t <sub>RD8</sub>	FO = 8 Routing Delay		2.8		3.2		3.6		4.2		5.5	ns
<b>I/O Module Sequential Timing (wrt IOCLK pad)</b>												
t <sub>INH</sub>	Input F-F Data Hold	0.0		0.0		0.0		0.0		0.0		ns
t <sub>INSU</sub>	Input F-F Data Setup	1.2		1.4		1.5		1.8		1.8		ns
t <sub>IDEH</sub>	Input Data Enable Hold	0.0		0.0		0.0		0.0		0.0		ns
t <sub>IDESU</sub>	Input Data Enable Setup	5.8		6.5		7.5		8.6		8.6		ns
t <sub>OUTH</sub>	Output F-F Data hold	0.7		0.8		1.0		1.0		1.0		ns
t <sub>OUTSU</sub>	Output F-F Data Setup	0.7		0.8		1.0		1.0		1.0		ns
t <sub>ODEH</sub>	Output Data Enable Hold	0.3		0.4		0.5		0.5		0.5		ns
f <sub>ODESU</sub>	Output Data Enable Setup	1.3		1.5		2.0		2.0		2.0		ns

Notes: \*

1. The –2 and –3 speed grades have been discontinued. Refer to PDN 0104, PDN 0203, PDN 0604, and PDN 1004 at <http://www.microsemi.com/soc/support/notifications/default.aspx#pdn>.
2. Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual worst-case performance. Post-route timing is based on actual routing delay measurements performed on the device prior to shipment.

## A14100A, A14V100A Timing Characteristics (continued)

Table 2-36 • A14100A, A14V100A Worst-Case Commercial Conditions, VCC = 4.75 V, T<sub>J</sub> = 70°C

I/O Module – TTL Output Timing <sup>1</sup>		–3 Speed <sup>2</sup>		–2 Speed <sup>2</sup>		–1 Speed		Std. Speed		3.3 V Speed <sup>1</sup>		Units
Parameter/Description		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t <sub>DHS</sub>	Data to Pad, High Slew		5.0		5.6		6.4		7.5		9.8	ns
t <sub>DLS</sub>	Data to Pad, Low Slew		8.0		9.0		10.2		12.0		15.6	ns
t <sub>ENZHS</sub>	Enable to Pad, Z to H/L, High Slew		4.0		4.5		5.1		6.0		7.8	ns
t <sub>ENZLS</sub>	Enable to Pad, Z to H/L, Low Slew		7.4		8.3		9.4		11.0		14.3	ns
t <sub>ENHSZ</sub>	Enable to Pad, H/L to Z, High Slew		8.0		9.0		10.2		12.0		15.6	ns
t <sub>ENLSZ</sub>	Enable to Pad, H/L to Z, Low Slew		7.4		8.3		9.4		11.0		14.3	ns
t <sub>CKHS</sub>	IOCLK Pad to Pad H/L, High Slew		9.5		9.5		10.5		12.0		15.6	ns
t <sub>CKLS</sub>	IOCLK Pad to Pad H/L, Low Slew		12.8		12.8		15.3		17.0		22.1	ns
d <sub>TLHHS</sub>	Delta Low to High, High Slew		0.02		0.02		0.03		0.03		0.04	ns/pF
d <sub>TLHLS</sub>	Delta Low to High, Low Slew		0.05		0.05		0.06		0.07		0.09	ns/pF
d <sub>THLHS</sub>	Delta High to Low, High Slew		0.04		0.04		0.04		0.05		0.07	ns/pF
d <sub>THLLS</sub>	Delta High to Low, Low Slew		0.05		0.05		0.06		0.07		0.09	ns/pF
I/O Module – CMOS Output Timing <sup>1</sup>												
t <sub>DHS</sub>	Data to Pad, High Slew		6.2		7.0		7.9		9.3		12.1	ns
t <sub>DLS</sub>	Data to Pad, Low Slew		11.7		13.1		14.9		17.5		22.8	ns
t <sub>ENZHS</sub>	Enable to Pad, Z to H/L, High Slew		5.2		5.9		6.6		7.8		10.1	ns
t <sub>ENZLS</sub>	Enable to Pad, Z to H/L, Low Slew		8.9		10.0		11.3		13.3		17.3	ns
t <sub>ENHSZ</sub>	Enable to Pad, H/L to Z, High Slew		8.0		9.0		10.0		12.0		15.6	ns
t <sub>ENLSZ</sub>	Enable to Pad, H/L to Z, Low Slew		7.4		8.3		9.4		11.0		14.3	ns
t <sub>CKHS</sub>	IOCLK Pad to Pad H/L, High Slew		10.4		10.4		12.4		13.8		17.9	ns
t <sub>CKLS</sub>	IOCLK Pad to Pad H/L, Low Slew		14.5		14.5		17.4		19.3		25.1	ns
d <sub>TLHHS</sub>	Delta Low to High, High Slew		0.04		0.04		0.05		0.06		0.08	ns/pF
d <sub>TLHLS</sub>	Delta Low to High, Low Slew		0.07		0.08		0.09		0.11		0.14	ns/pF
d <sub>THLHS</sub>	Delta High to Low, High Slew		0.03		0.03		0.03		0.04		0.05	ns/pF
d <sub>THLLS</sub>	Delta High to Low, Low Slew		0.04		0.04		0.04		0.05		0.07	ns/pF

Notes: \*

1. Delays based on 35 pF loading.
2. The –2 and –3 speed grades have been discontinued. Refer to PDN 0104, PDN 0203, PDN 0604, and PDN 1004 at <http://www.microsemi.com/soc/support/notifications/default.aspx#pdn>.

## Pin Descriptions

### **CLKA**                      **Clock A (Input)**

Clock input for clock distribution networks. The Clock input is buffered prior to clocking the logic modules. This pin can also be used as an I/O.

### **CLKB**                      **Clock B (Input)**

Clock input for clock distribution networks. The Clock input is buffered prior to clocking the logic modules. This pin can also be used as an I/O.

### **GND**                      **Ground**

LOW supply voltage.

### **HCLK**                      **Dedicated (Hard-wired) Array Clock (Input)**

Clock input for sequential modules. This input is directly wired to each S-Module and offers clock speeds independent of the number of S-Modules being driven. This pin can also be used as an I/O.

### **I/O**                      **Input/Output (Input, Output)**

The I/O pin functions as an input, output, three-state, or bidirectional buffer. Input and output levels are compatible with standard TTL and CMOS specifications. Unused I/O pins are tristated by the Designer Series software.

### **IOCLK**                      **Dedicated (Hard-wired) I/O Clock (Input)**

Clock input for I/O modules. This input is directly wired to each I/O module and offers clock speeds independent of the number of I/O modules being driven. This pin can also be used as an I/O.

### **IOPCL**                      **Dedicated (Hard-wired) I/O Preset/Clear (Input)**

Input for I/O preset or clear. This global input is directly wired to the preset and clear inputs of all I/O registers. This pin functions as an I/O when no I/O preset or clear macros are used.

### **MODE**                      **Mode (Input)**

The MODE pin controls the use of diagnostic pins (DCLK, PRA, PRB, SDI). When the MODE pin is HIGH, the special functions are active. When the MODE pin is LOW, the pins function as I/Os. To provide Actionprobe capability, the MODE pin should be terminated to GND through a 10K resistor so that the MODE pin can be pulled high when required.

### **NC**                      **No Connection**

This pin is not connected to circuitry within the device.

### **PRA**                      **Probe A (Output)**

The Probe A pin is used to output data from any user-defined design node within the device. This independent diagnostic pin can be used in conjunction with the Probe B pin to allow real-time diagnostic output of any signal path within the device. The Probe A pin can be used as a user-defined I/O when debugging has been completed. The pin's probe capabilities can be permanently disabled to protect programmed design confidentiality. PRA is accessible when the MODE pin is HIGH. This pin functions as an I/O when the MODE pin is LOW.

### **PRB**                      **Probe B (Output)**

The Probe B pin is used to output data from any user-defined design node within the device. This independent diagnostic pin can be used in conjunction with the Probe A pin to allow real-time diagnostic output of any signal path within the device. The Probe B pin can be used as a user-defined I/O when debugging has been completed. The pin's probe capabilities can be permanently disabled to protect programmed design confidentiality. PRB is accessible when the MODE pin is HIGH. This pin functions as an I/O when the MODE pin is LOW.

### **SDI**                      **Serial Data Input (Input)**

Serial data input for diagnostic probe and device programming. SDI is active when the MODE pin is HIGH. This pin functions as an I/O when the MODE pin is LOW.

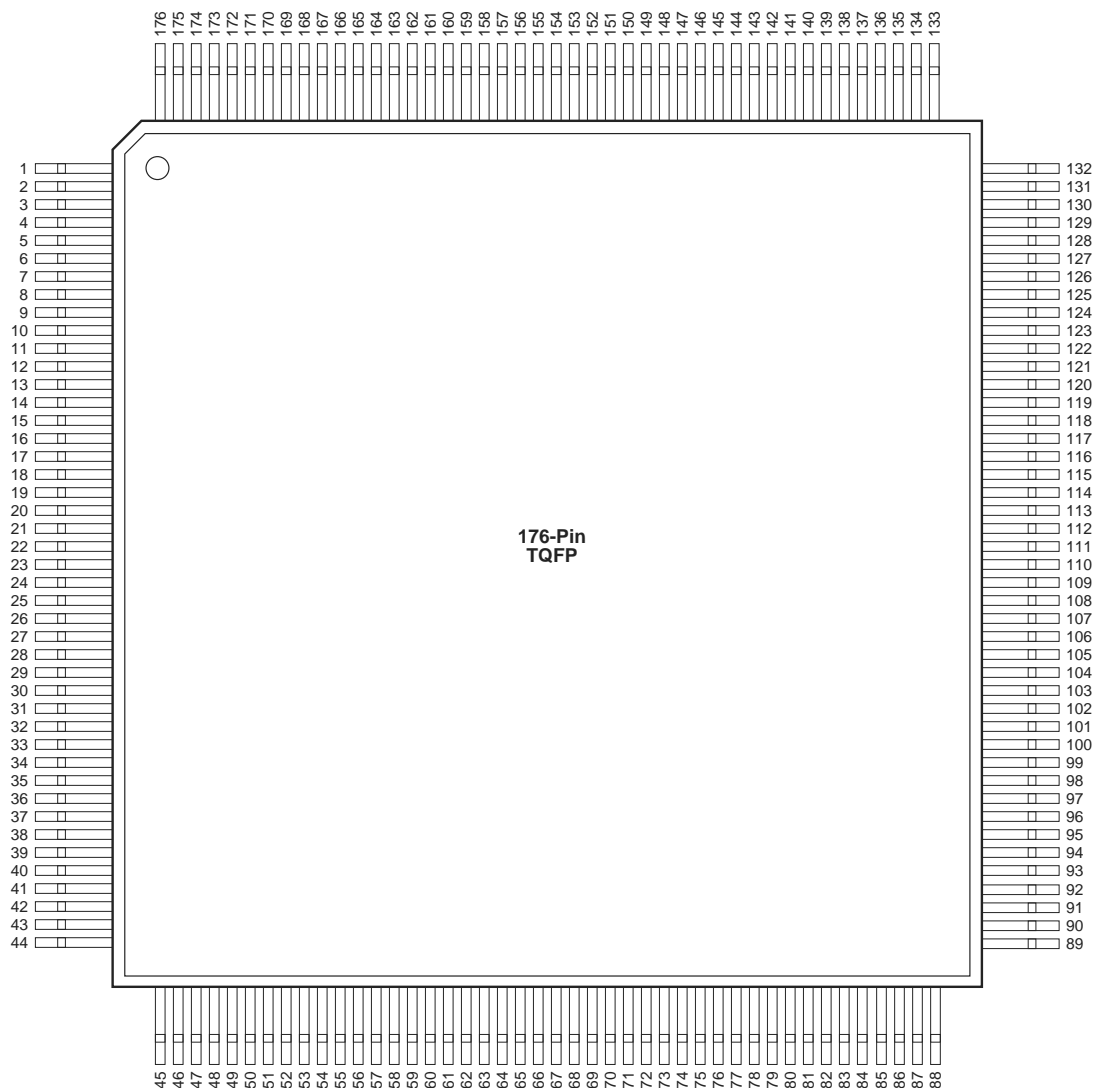


PQ160			
Pin Number	A1425, A14V25 Function	A1440, A14V40 Function	A1460, A14V60 Function
92	NC	I/O	I/O
93	NC	I/O	I/O
98	GND	GND	GND
99	VCC	VCC	VCC
100	NC	I/O	I/O
103	GND	GND	GND
107	NC	I/O	I/O
109	NC	I/O	I/O
110	VCC	VCC	VCC
111	GND	GND	GND
112	VCC	VCC	VCC
113	NC	I/O	I/O
119	NC	I/O	I/O
120	IOCLK, I/O	IOCLK, I/O	IOCLK, I/O
121	GND	GND	GND
124	NC	I/O	I/O
127	NC	I/O	I/O
136	CLKA, I/O	CLKA, I/O	CLKA, I/O
137	CLKB, I/O	CLKB, I/O	CLKB, I/O
138	VCC	VCC	VCC
139	GND	GND	GND
140	VCC	VCC	VCC
141	GND	GND	GND
142	PRA, I/O	PRA, I/O	PRA, I/O
143	NC	I/O	I/O
145	NC	I/O	I/O
147	NC	I/O	I/O
149	NC	I/O	I/O
151	NC	I/O	I/O
153	NC	I/O	I/O
154	VCC	VCC	VCC
160	DCLK, I/O	DCLK, I/O	DCLK, I/O

**Notes:**

1. All unlisted pin numbers are user I/Os.
2. NC denotes no connection.
3. MODE should be terminated to GND through a 10K resistor to enable Actionprobe usage; otherwise it can be terminated directly to GND.

## TQ176



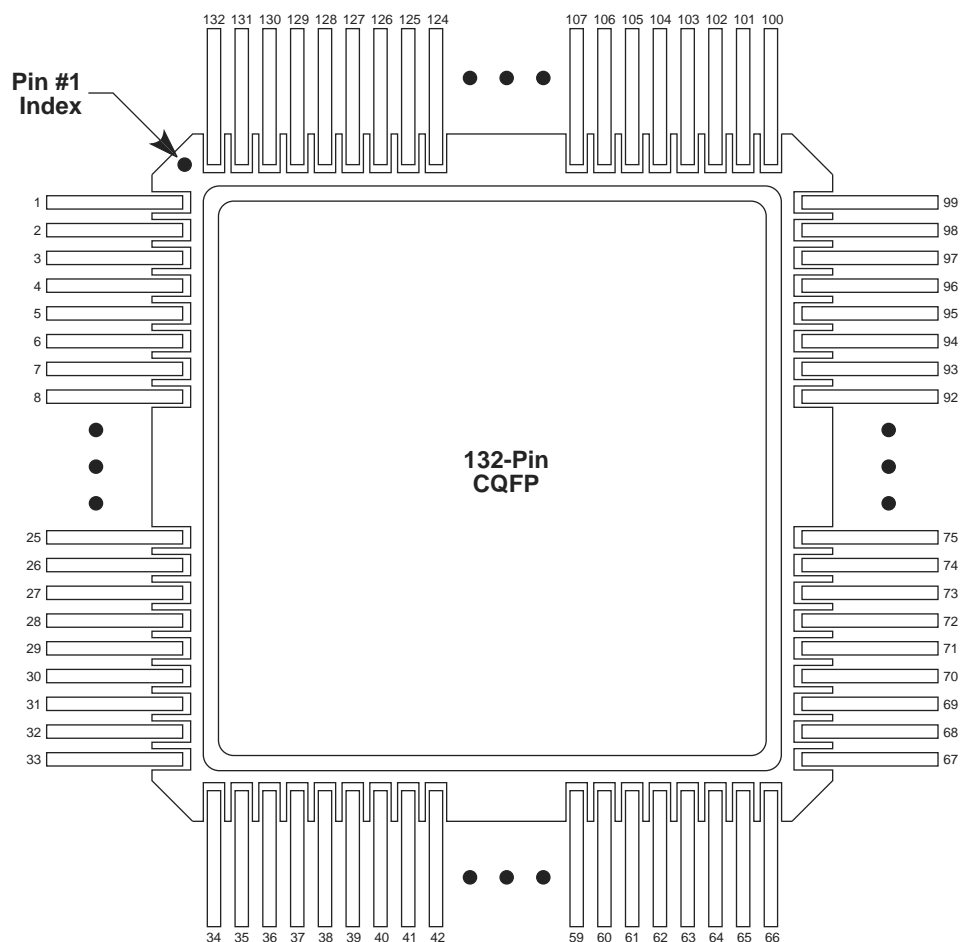
*Note: This is the top view.*

### Note

For Package Manufacturing and Environmental information, visit the Resource Center at <http://www.microsemi.com/soc/products/solutions/package/docs.aspx>



## CQ132



*Note:* This is the top view

### Note

For Package Manufacturing and Environmental information, visit the Resource Center at <http://www.microsemi.com/soc/products/solutions/package/docs.aspx>

CQ132		CQ132	
Pin Number	A1425 Function	Pin Number	A1425 Function
1	NC	67	NC
2	GND	74	GND
3	SDI, I/O	75	VCC
9	MODE	78	VCC
10	GND	89	VCC
11	VCC	90	GND
22	VCC	91	VCC
26	GND	92	GND
27	VCC	98	IOCLK, I/O
34	NC	99	NC
36	GND	100	NC
42	GND	101	GND
43	VCC	106	GND
48	PRB, I/O	107	VCC
50	HCLK, I/O	116	CLKA, I/O
58	GND	117	CLKB, I/O
59	VCC	118	PRA, I/O
63	SDO	122	GND
64	IOPCL, I/O	123	VCC
65	GND	131	DCLK, I/O
66	NC	132	NC

*Notes:*

1. All unlisted pin numbers are user I/Os.
2. NC denotes no connection.
3. MODE should be terminated to GND through a 10K resistor to enable Actionprobe usage; otherwise it can be terminated directly to GND.

CQ256	
Pin Number	A14100 Function
1	GND
2	SDI, I/O
11	MODE
28	VCC
29	GND
30	VCC
31	GND
46	VCC
59	GND
90	PRB, I/O
91	GND
92	VCC
93	GND
94	VCC
96	HCLK, I/O
110	GND
126	SDO
127	IOPCL, I/O
128	GND

CQ256	
Pin Number	A14100 Function
141	VCC
158	GND
159	VCC
160	GND
161	VCC
174	VCC
175	GND
176	GND
188	IOCLK, I/O
189	GND
219	CLKA, I/O
220	CLKB, I/O
221	VCC
222	GND
223	VCC
224	GND
225	PRA, I/O
240	GND
256	DCLK, I/O

**Notes:**

1. All unlisted pin numbers are user I/Os.
2. NC denotes no connection.
3. MODE should be terminated to GND through a 10K resistor to enable Actionprobe usage; otherwise it can be terminated directly to GND.

BG225	
A1460 Function	Location
CLKA or I/O	C8
CLKB or I/O	B8
DCLK or I/O	B2
GND	A1, A15, D15, F8, G7, G8, G9, H6, H7, H8, H9, H10, J7, J8, J9, K8, P2, R15
HCLK or I/O	P9
IOCLK or I/O	B14
IOPCL or I/O	P14
MODE	D1
NC	A11, B5, B7, D8, D12, F6, F11, H1, H12, H14, K11, L1, L13, N8, P5, R1, R8, R11, R14
PRA or I/O	A7
PRB or I/O	L7
SDI or I/O	D4
SDO	N13
VCC	A8, B12, D5, D14, E3, E8, E13, H2, H3, H11, H15, K4, L2, L12, M8, M15, P4, P8, R13

*Notes:*

1. All unlisted pin numbers are user I/Os.
2. NC denotes no connection.
3. MODE should be terminated to GND through a 10K resistor to enable Actionprobe usage; otherwise it can be terminated directly to GND.
4. The BG225 package has been discontinued.

## 4 – Datasheet Information

### List of Changes

The following table lists critical changes that were made in each version of the datasheet.

Revision	Changes	Page
Revision 3 (January 2012)	The description for SDO pins had earlier been removed from the datasheet and has now been included again, in the "Pin Descriptions" section (SAR 35820).	2-21
	SDO pin numbers had earlier been removed from package pin assignment tables in the datasheet, and have now been restored to the pin tables (SAR 35820).	3-1
Revision 2 (September 2011)	The ACT 3 datasheet was formatted newly in the style used for current datasheets. The same information is present (other than noted in the list of changes for this revision) but divided into chapters.	N/A
	The datasheet was revised to note in multiple places that speed grades –2 and –3 have been discontinued. The following device/package combinations have been discontinued for all speed grades and temperatures (SAR 33872): A1415 PG100 A1425 PG133 A1440 PG175 A1460 BG225 Refer to PDN 0104, PDN 0203, PDN 0604, and PDN 1004.	I and others
	The "Features" section was revised to state the clock-to-output time and on-chip performance for –1 speed grade as 9.0 ns and 186 MHz. The "General Description" section was revised in accordance (SAR 33872).	I
	The maximum performance values were updated in Table 1 • ACT 3 Family Product Information, and now reflect worst-case commercial for the –1 speed grade (SAR 33872).	I
	The "Product Plan" table was updated as follows to conform to current offerings (SAR 33872): The A1415A device is offered in PL84, PG100, and VQ100 packages for Military application. The A1440A device is offered in TQ176 and VQ100 packages for Industrial application.	III
	Table 1-1 • Chip-to-Chip Performance (worst-case commercial) was updated to include data for all speed grades instead of only –3 (SAR 33872).	1-2
	Figure 1-1 • Predictable Performance (worst-case commercial, –1 speed grade) was revised to reflect values for the –1 speed grade (SAR 33872).	1-1
	Figure 2-10 • Timing Model was updated to show data for the –1 speed grade instead of –3 (SAR 33872).	2-16
	Table 2-14 • Logic Module and Routing Delay by Fanout (ns); Worst-Case Commercial Conditions was updated to include data for all speed grades instead of only –3 (SAR 33872).	2-20
	Package names used in the "Package Pin Assignments" section and throughout the document were revised to match standards given in <i>Package Mechanical Drawings</i> (SAR 27395).	3-1