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## Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

## Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

| Details | |
|---|---|
| Product Status | Obsolete |
| Number of LABs/CLBs | 310 |
| Number of Logic Elements/Cells | - |
| Total RAM Bits | - |
| Number of I/O | 100 |
| Number of Gates | 2500 |
| Voltage - Supply | 4.5V ~ 5.5V |
| Mounting Type | Surface Mount |
| Operating Temperature | 0°C ~ 70°C (TA) |
| Package / Case | 132-BCQFP with Tie Bar |
| Supplier Device Package | 132-CQFP (63.5x63.5) |
| Purchase URL | https://www.e-xfl.com/product-detail/microsemi/a1425a-1cq132c |

## Dedicated Clocks

Dedicated clock networks support high performance by providing sub-nanosecond skew and guaranteed performance. Dedicated clock networks contain no programming elements in the path from the I/O Pad Driver to the input of S-modules or I/O modules. There are two dedicated clock networks: one for the array registers (HCLK), and one for the I/O registers (IOCLK). The clock networks are accessed by special I/Os.

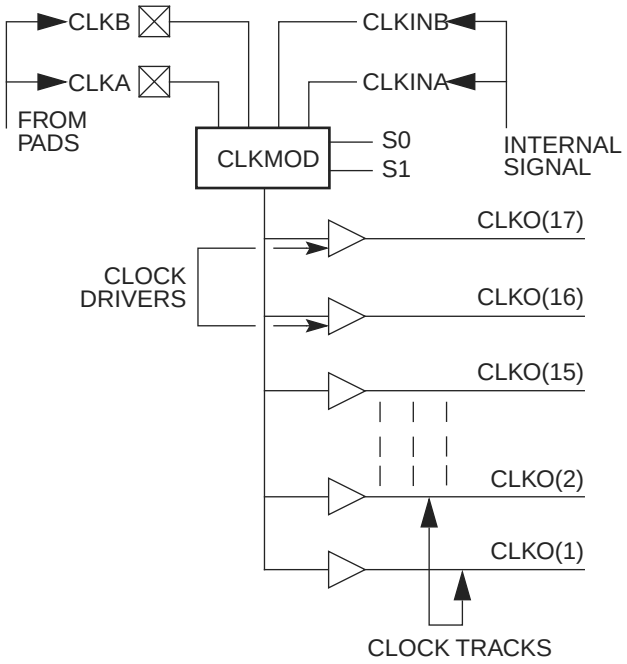



***Figure 2-6 •*** **Clock Networks**

The routed clock networks are referred to as CLK0 and CLK1. Each network is connected to a clock module (CLKMOD) that selects the source of the clock signal and may be driven as follows (Figure 2-6):

- Externally from the CLKA pad
- Externally from the CLKB pad
- Internally from the CLKINA input
- Internally from the CLKINB input

The clock modules are located in the top row of I/O modules. Clock drivers and a dedicated horizontal clock track are located in each horizontal routing channel. The function of the clock module is determined by the selection of clock macros from the macro library. The macro CLKBUF is used to connect one of the two external clock pins to a clock network, and the macro CLKINT is used to connect an internally generated clock signal to a clock network. Since both clock networks are identical, the user does not care whether CLK0 or CLK1 is being used. Routed clocks can also be used to drive high fanout nets like resets, output enables, or data enables. This saves logic modules and results in performance increases in some cases.

# Routing Structure

The ACT 3 architecture uses vertical and horizontal routing tracks to connect the various logic and I/O modules. These routing tracks are metal interconnects that may either be of continuous length or broken into segments. Segments can be joined together at the ends using antifuses to increase their lengths up to the full length of the track.

### Module Output Connections

Module outputs have dedicated output segments. Output segments extend vertically two channels above and two channels below, except at the top or bottom of the array. Output segments twist, as shown in Figure 10, so that only four vertical tracks are required.

### LVT Connections

Outputs may also connect to nondedicated segments called Long Vertical Tracks (LVTs). Each module pair in the array shares four LVTs that span the length of the column. Any module in the column pair can connect to one of the LVTs in the column using an FF connection. The FF connection uses antifuses connected directly to the driver stage of the module output, bypassing the isolation transistor. FF antifuses are programmed at a higher current level than HF, VF, or XF antifuses to produce a lower resistance value.

### Antifuse Connections

In general every intersection of a vertical segment and a horizontal segment contains an unprogrammed antifuse (XF-type). One exception is in the case of the clock networks.

### Clock Connections

To minimize loading on the clock networks, a subset of inputs has antifuses on the clock tracks. Only a few of the C-module and S-module inputs can be connected to the clock networks. To further reduce loading on the clock network, only a subset of the horizontal routing tracks can connect to the clock inputs of the S-module.

## Programming and Test Circuits

The array of logic and I/O modules is surrounded by test and programming circuits controlled by the temporary special I/O pins MODE, SDI, and DCLK. The function of these pins is similar to all ACT family devices. The ACT 3 family also includes support for two Actionprobe® circuits, allowing complete observability of any logic or I/O module in the array using the temporary special I/O pins, PRA and PRB.

Equivalent capacitance is calculated by measuring ICC active at a specified frequency and voltage for each circuit component of interest. Measurements have been made over a range of frequencies at a fixed value of VCC. Equivalent capacitance is frequency independent so that the results may be used over a wide range of operating conditions. Equivalent capacitance values are shown in Figure 2-10.

***Table 2-10* • CEQ Values for Microsemi FPGAs**

| Item | CEQ Value |
|---|---|
| Modules ($C_{EQM}$) | 6.7 |
| Input Buffers ($C_{EQI}$) | 7.2 |
| Output Buffers ($C_{EQO}$) | 10.4 |
| Routed Array Clock Buffer Loads ($C_{EQCR}$) | 1.6 |
| Dedicated Clock Buffer Loads ($C_{EQCD}$) | 0.7 |
| I/O Clock Buffer Loads ($C_{EQCI)}$ | 0.9 |

To calculate the active power dissipated from the complete design, the switching frequency of each part of the logic must be known. EQ 5 shows a piece-wise linear summation over all components.

$$\text{Power} = VCC^2 * [(m * C_{EQM} * f_m)_{modules} + (n * C_{EQI} * f_n)_{inputs} + (p * (C_{EQO} + C_L) * fp)_{outputs} + 0.5 * (q1 * C_{EQCR} * f_{q1})_{routed\_Clk1} + (r1 * fq1)_{routed\_Clk1} + 0.5 * (q2 * C_{EQCR} * fq2)_{routed\_Clk2} + (r_2 * f_{q2})_{routed\_Clk2} + 0.5 * (s_1 * C_{EQCD} * f_{s1})_{dedicated\_Clk} + (s_2 * C_{EQCI} * f_{s2})_{IO\_Clk}]$$

*EQ 5*

Where:

$m$ = Number of logic modules switching at $f_m$
$n$ = Number of input buffers switching at $f_n$
$p$ = Number of output buffers switching at $f_p$
q1 = Number of clock loads on the first routed array clock
q2 = Number of clock loads on the second routed array clock
$r_1$ = Fixed capacitance due to first routed array clock
$r_2$ = Fixed capacitance due to second routed array clock
$s_1$ = Fixed number of clock loads on the dedicated array clock
$s_2$ = Fixed number of clock loads on the dedicated I/O clock
$C_{EQM}$ = Equivalent capacitance of logic modules in pF
$C_{EQI}$ = Equivalent capacitance of input buffers in pF
$C_{EQO}$ = Equivalent capacitance of output buffers in pF
$C_{EQCR}$ = Equivalent capacitance of routed array clock in pF
$C_{EQCD}$ = Equivalent capacitance of dedicated array clock in pF
$C_{EQCI}$ = Equivalent capacitance of dedicated I/O clock in pF
$C_L$ = Output lead capacitance in pF
$f_m$ = Average logic module switching rate in MHz
$f_n$ = Average input buffer switching rate in MHz
$f_p$ = Average output buffer switching rate in MHz
$f_{q1}$ = Average first routed array clock rate in MHz
$f_{q2}$ = Average second routed array clock rate in MHz
$f_{s1}$ = Average dedicated array clock rate in MHz
$f_{s2}$ = Average dedicated I/O clock rate in MHz

***Table 2-11* • Fixed Capacitance Values for Microsemi FPGAs**

| Device Type | r1, routed_Clk1 | r2, routed_Clk2 |
|---|---|---|
| A1415A | 60 | 60 |
| A14V15A | 57 | 57 |
| A1425A | 75 | 75 |
| A14V25A | 72 | 72 |
| A1440A | 105 | 105 |
| A14V40A | 100 | 100 |
| A1440B | 105 | 105 |
| A1460A | 165 | 165 |
| A14V60A | 157 | 157 |
| A1460B | 165 | 165 |
| A14100A | 195 | 195 |
| A14V100A | 185 | 185 |
| A14100B | 195 | 195 |

***Table 2-12* • Fixed Clock Loads (s1/s2)**

| Device Type | s1, Clock Loads on Dedicated Array Clock | s2, Clock Loads on Dedicated I/O Clock |
|---|---|---|
| A1415A | 104 | 80 |
| A14V15A | 104 | 80 |
| A1425A | 160 | 100 |
| A14V25A | 160 | 100 |
| A1440A | 288 | 140 |
| A14V40A | 288 | 140 |
| A1440B | 288 | 140 |
| A1460A | 432 | 168 |
| A14V60A | 432 | 168 |
| A1460B | 432 | 168 |
| A14100A | 697 | 228 |
| A14V100A | 697 | 228 |
| A14100B | 697 | 228 |

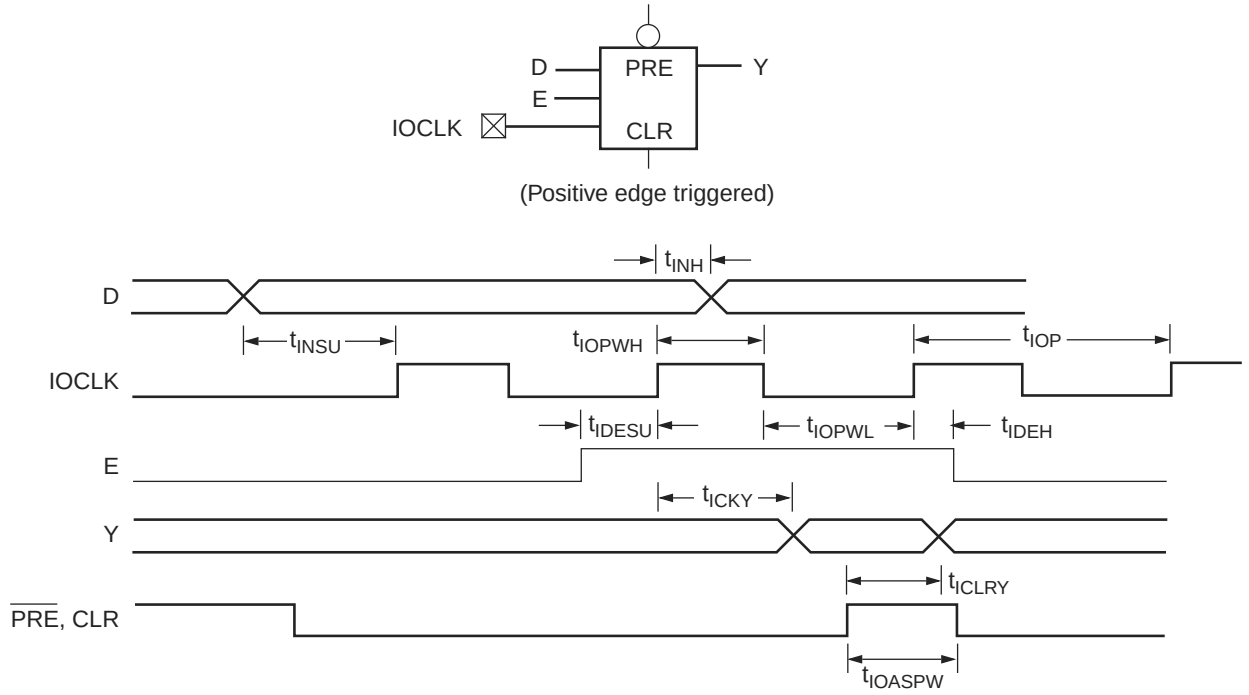



***Figure 2-16 •*** **I/O Module: Sequential Input Timing Characteristics**

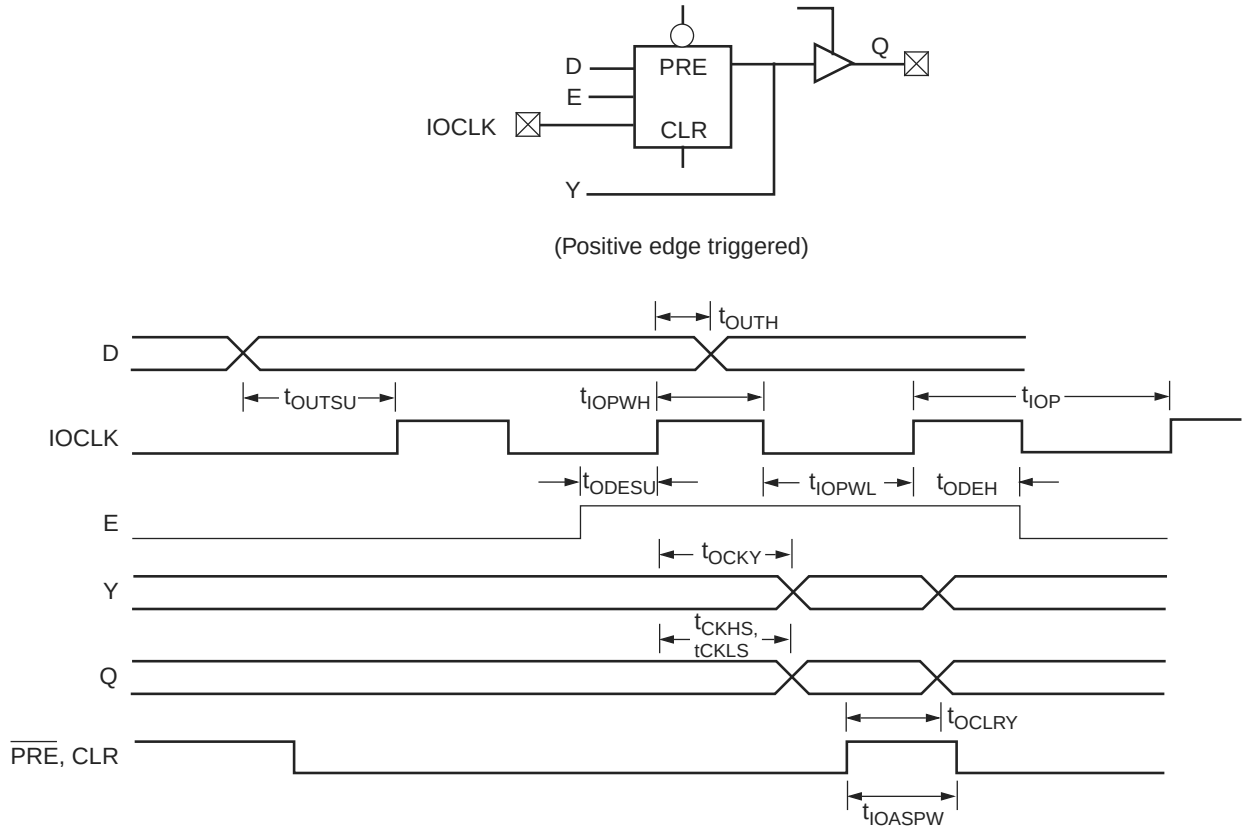



***Figure 2-17 •*** **I/O Module: Sequential Output Timing Characteristics**

## A1415A, A14V15A Timing Characteristics (continued)

***Table 2-19* • A1415A, A14V15A Worst-Case Commercial Conditions, VCC = 4.75 V, $T_J$ = 70°C**

| I/O Module Input Propagation Delays | | –3 Speed[1] | | –2 Speed[1] | | –1 Speed | | Std. Speed | | 3.3 V Speed[2] | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **Parameter/Description** | | **Min.** | **Max.** | **Min.** | **Max.** | **Min.** | **Max.** | **Min.** | **Max.** | **Min.** | **Max.** | |
| $t_{INY}$ | Input Data Pad to Y | | 2.8 | | 3.2 | | 3.6 | | 4.2 | | 5.5 | ns |
| $t_{ICKY}$ | Input Reg IOCLK Pad to Y | | 4.7 | | 5.3 | | 6.0 | | 7.0 | | 9.2 | ns |
| $t_{OCKY}$ | Output Reg IOCLK Pad to Y | | 4.7 | | 5.3 | | 6.0 | | 7.0 | | 9.2 | ns |
| $t_{ICLRY}$ | Input Asynchronous Clear to Y | | 4.7 | | 5.3 | | 6.0 | | 7.0 | | 9.2 | ns |
| $t_{OCLRY}$ | Output Asynchronous Clear to Y | | 4.7 | | 5.3 | | 6.0 | | 7.0 | | 9.2 | ns |
| **Predicted Input Routing Delays[2]** | | | | | | | | | | | | |
| $t_{RD1}$ | FO = 1 Routing Delay | | 0.9 | | 1.0 | | 1.1 | | 1.3 | | 1.7 | ns |
| $t_{RD2}$ | FO = 2 Routing Delay | | 1.2 | | 1.4 | | 1.6 | | 1.8 | | 2.4 | ns |
| $t_{RD3}$ | FO = 3 Routing Delay | | 1.4 | | 1.6 | | 1.8 | | 2.1 | | 2.8 | ns |
| $t_{RD4}$ | FO = 4 Routing Delay | | 1.7 | | 1.9 | | 2.2 | | 2.5 | | 3.3 | ns |
| $t_{RD8}$ | FO = 8 Routing Delay | | 2.8 | | 3.2 | | 3.6 | | 4.2 | | 5.5 | ns |
| **I/O Module Sequential Timing (wrt IOCLK pad)** | | | | | | | | | | | | |
| $t_{INH}$ | Input F-F Data Hold | 0.0 | | 0.0 | | 0.0 | | 0.0 | | 0.0 | | ns |
| $t_{INSU}$ | Input F-F Data Setup | 2.0 | | 2.3 | | 2.5 | | 3.0 | | 3.0 | | ns |
| $t_{IDEH}$ | Input Data Enable Hold | 0.0 | | 0.0 | | 0.0 | | 0.0 | | 0.0 | | ns |
| $t_{IDESU}$ | Input Data Enable Setup | 5.8 | | 6.5 | | 7.5 | | 8.6 | | 8.6 | | ns |
| $t_{OUTH}$ | Output F-F Data hold | 0.7 | | 0.8 | | 0.9 | | 1.0 | | 1.0 | | ns |
| $t_{OUTSU}$ | Output F-F Data Setup | 0.7 | | 0.8 | | 0.9 | | 1.0 | | 1.0 | | ns |
| $t_{ODEH}$ | Output Data Enable Hold | 0.3 | | 0.4 | | 0.4 | | 0.5 | | 0.5 | | ns |
| $f_{ODESU}$ | Output Data Enable Setup | 1.3 | | 1.5 | | 1.7 | | 2.0 | | 2.0 | | ns |

*Notes:*

1. *The –2 and –3 speed grades have been discontinued. Please refer to the Product Discontinuation Notices (PDNs) listed below:*

   *PDN March 2001*
   *PDN 0104*
   *PDN 0203*
   *PDN 0604*
   *PDN 1004*

2. *Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual worst-case performance. Post-route timing is based on actual routing delay measurements performed on the device prior to shipment.*

## A1425A, A14V25A Timing Characteristics (continued)

***Table 2-25* • A1425A, A14V25A Worst-Case Commercial Conditions, VCC = 4.75 V, $T_J$ = 70°C**

| Dedicated (hardwired) I/O Clock Network | | –3 Speed[1] | | –2 Speed[1] | | –1 Speed | | Std. Speed | | 3.3 V Speed[1] | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **Parameter/Description** | | **Min.** | **Max.** | **Min.** | **Max.** | **Min.** | **Max.** | **Min.** | **Max.** | **Min.** | **Max.** | |
| $t_{IOCKH}$ | Input Low to High (pad to I/O module input) | | 2.0 | | 2.3 | | 2.6 | | 3.0 | | 3.5 | ns |
| $t_{IOPWH}$ | Minimum Pulse Width High | 1.9 | | 2.4 | | 3.3 | | 3.8 | | 4.8 | | ns |
| $t_{IPOWL}$ | Minimum Pulse Width Low | 1.9 | | 2.4 | | 3.3 | | 3.8 | | 4.8 | | ns |
| $t_{IOSAPW}$ | Minimum Asynchronous Pulse Width | 1.9 | | 2.4 | | 3.3 | | 3.8 | | 4.8 | | ns |
| $t_{IOCKSW}$ | Maximum Skew | | 0.4 | | 0.4 | | 0.4 | | 0.4 | | 0.4 | ns |
| $t_{IOP}$ | Minimum Period | 4.0 | | 5.0 | | 6.8 | | 8.0 | | 10.0 | | ns |
| $f_{IOMAX}$ | Maximum Frequency | | 250 | | 200 | | 150 | | 125 | | 100 | MHz |
| **Dedicated (hardwired) Array Clock** | | | | | | | | | | | | |
| $t_{HCKH}$ | Input Low to High (pad to S-module input) | | 3.0 | | 3.4 | | 3.9 | | 4.5 | | 5.5 | ns |
| $t_{HCKL}$ | Input High to Low (pad to S-module input) | | 3.0 | | 3.4 | | 3.9 | | 4.5 | | 5.5 | ns |
| $t_{HPWH}$ | Minimum Pulse Width High | 1.9 | | 2.4 | | 3.3 | | 3.8 | | 4.8 | | ns |
| $t_{HPWL}$ | Minimum Pulse Width Low | 1.9 | | 2.4 | | 3.3 | | 3.8 | | 4.8 | | ns |
| $t_{HCKSW}$ | Delta High to Low, Low Slew | | 0.3 | | 0.3 | | 0.3 | | 0.3 | | 0.3 | ns |
| $t_{HP}$ | Minimum Period | 4.0 | | 5.0 | | 6.8 | | 8.0 | | 10.0 | | ns |
| $f_{HMAX}$ | Maximum Frequency | | 250 | | 200 | | 150 | | 125 | | 100 | MHz |
| **Routed Array Clock Networks** | | | | | | | | | | | | |
| $t_{RCKH}$ | Input Low to High (FO = 64) | | 3.7 | | 4.1 | | 4.7 | | 5.5 | | 9.0 | ns |
| $t_{RCKL}$ | Input High to Low (FO = 64) | | 4.0 | | 4.5 | | 5.1 | | 6.0 | | 9.0 | ns |
| $t_{RPWH}$ | Min. Pulse Width High (FO = 64) | 3.3 | | 3.8 | | 4.2 | | 4.9 | | 6.5 | | ns |
| $t_{RPWL}$ | Min. Pulse Width Low (FO = 64) | 3.3 | | 3.8 | | 4.2 | | 4.9 | | 6.5 | | ns |
| $t_{RCKSW}$ | Maximum Skew (FO = 128) | | 0.7 | | 0.8 | | 0.9 | | 1.0 | | 1.0 | ns |
| $t_{RP}$ | Minimum Period (FO = 64) | 6.8 | | 8.0 | | 8.7 | | 10.0 | | 13.4 | | ns |
| $f_{RMAX}$ | Maximum Frequency (FO = 64) | | 150 | | 125 | | 115 | | 100 | | 75 | MHz |
| **Clock-to-Clock Skews** | | | | | | | | | | | | |
| $t_{IOHCKSW}$ | I/O Clock to H-Clock Skew | 0.0 | 1.7 | 0.0 | 1.8 | 0.0 | 2.0 | 0.0 | 2.2 | 0.0 | 3.0 | ns |
| $t_{IORCKSW}$ | I/O Clock to R-Clock Skew (FO = 64)<br>(FO = 80) | 0.0<br>0.0 | 1.0<br>3.0 | 0.0<br>0.0 | 1.0<br>3.0 | 0.0<br>0.0 | 1.0<br>3.0 | 0.0<br>0.0 | 1.0<br>3.0 | 0.0<br>0.0 | 3.0<br>3.0 | ns |
| $t_{HRCKSW}$ | H-Clock to R-Clock Skew (FO = 64)<br>(FO = 80) | 0.0<br>0.0 | 1.0<br>3.0 | 0.0<br>0.0 | 1.0<br>3.0 | 0.0<br>0.0 | 1.0<br>3.0 | 0.0<br>0.0 | 1.0<br>3.0 | 0.0<br>0.0 | 1.0<br>3.0 | ns |

*Notes:*

1. *The –2 and –3 speed grades have been discontinued. Refer to PDN 0104, PDN 0203, PDN 0604, and PDN 1004 at http://www.microsemi.com/soc/support/notifications/default.aspx#pdn.*
2. *Delays based on 35 pF loading.*

## A1460A, A14V60A Timing Characteristics (continued)

***Table 2-31* • A1460A, A14V60A Worst-Case Commercial Conditions, VCC = 4.75 V, $T_J$ = 70°C**

| I/O Module Input Propagation Delays | | –3 Speed[1] | | –2 Speed[1] | | –1 Speed | | Std. Speed | | 3.3 V Speed[1] | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **Parameter/Description** | | **Min.** | **Max.** | **Min.** | **Max.** | **Min.** | **Max.** | **Min.** | **Max.** | **Min.** | **Max.** | |
| $t_{INY}$ | Input Data Pad to Y | | 2.8 | | 3.2 | | 3.6 | | 4.2 | | 5.5 | ns |
| $t_{ICKY}$ | Input Reg IOCLK Pad to Y | | 4.7 | | 5.3 | | 6.0 | | 7.0 | | 9.2 | ns |
| $t_{OCKY}$ | Output Reg IOCLK Pad to Y | | 4.7 | | 5.3 | | 6.0 | | 7.0 | | 9.2 | ns |
| $t_{ICLRY}$ | Input Asynchronous Clear to Y | | 4.7 | | 5.3 | | 6.0 | | 7.0 | | 9.2 | ns |
| $t_{OCLRY}$ | Output Asynchronous Clear to Y | | 4.7 | | 5.3 | | 6.0 | | 7.0 | | 9.2 | ns |
| **Predicted Input Routing Delays[2]** | | | | | | | | | | | | |
| $t_{RD1}$ | FO = 1 Routing Delay | | 0.9 | | 1.0 | | 1.1 | | 1.3 | | 1.7 | ns |
| $t_{RD2}$ | FO = 2 Routing Delay | | 1.2 | | 1.4 | | 1.6 | | 1.8 | | 2.4 | ns |
| $t_{RD3}$ | FO = 3 Routing Delay | | 1.4 | | 1.6 | | 1.8 | | 2.1 | | 2.8 | ns |
| $t_{RD4}$ | FO = 4 Routing Delay | | 1.7 | | 1.9 | | 2.2 | | 2.5 | | 3.3 | ns |
| $t_{RD8}$ | FO = 8 Routing Delay | | 2.8 | | 3.2 | | 3.6 | | 4.2 | | 5.5 | ns |
| **I/O Module Sequential Timing (wrt IOCLK pad)** | | | | | | | | | | | | |
| $t_{INH}$ | Input F-F Data Hold | 0.0 | | 0.0 | | 0.0 | | 0.0 | | 0.0 | | ns |
| $t_{INSU}$ | Input F-F Data Setup | 1.3 | | 1.5 | | 1.8 | | 2.0 | | 2.0 | | ns |
| $t_{IDEH}$ | Input Data Enable Hold | 0.0 | | 0.0 | | 0.0 | | 0.0 | | 0.0 | | ns |
| $t_{IDESU}$ | Input Data Enable Setup | 5.8 | | 6.5 | | 7.5 | | 8.6 | | 8.6 | | ns |
| $t_{OUTH}$ | Output F-F Data hold | 0.7 | | 0.8 | | 0.9 | | 1.0 | | 1.0 | | ns |
| $t_{OUTSU}$ | Output F-F Data Setup | 0.7 | | 0.8 | | 0.9 | | 1.0 | | 1.0 | | ns |
| $t_{ODEH}$ | Output Data Enable Hold | 0.3 | | 0.4 | | 0.4 | | 0.5 | | 0.5 | | ns |
| $f_{ODESU}$ | Output Data Enable Setup | 1.3 | | 1.5 | | 1.7 | | 2.0 | | 2.0 | | ns |

*Notes:*

5. *The –2 and –3 speed grades have been discontinued. Refer to PDN 0104, PDN 0203, PDN 0604, and PDN 1004 at http://www.microsemi.com/soc/support/notifications/default.aspx#pdn.*
6. *Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual worst-case performance. Post-route timing is based on actual routing delay measurements performed on the device prior to shipment.*

## A1460A, A14V60A Timing Characteristics (continued)

**Table 2-32 • A1460A, A14V60A Worst-Case Commercial Conditions, VCC = 4.75 V, $T_J$ = 70°C**

| I/O Module – TTL Output Timing[1] | | –3 Speed[2] | | –2 Speed[2] | | –1 Speed | | Std. Speed | | 3.3 V Speed[1] | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Parameter/Description | | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | |
| $t_{DHS}$ | Data to Pad, High Slew | | 5.0 | | 5.6 | | 6.4 | | 7.5 | | 9.8 | ns |
| $t_{DLS}$ | Data to Pad, Low Slew | | 8.0 | | 9.0 | | 10.2 | | 12.0 | | 15.6 | ns |
| $t_{ENZHS}$ | Enable to Pad, Z to H/L, High Slew | | 4.0 | | 4.5 | | 5.1 | | 6.0 | | 7.8 | ns |
| $t_{ENZLS}$ | Enable to Pad, Z to H/L, Low Slew | | 7.4 | | 8.3 | | 9.4 | | 11.0 | | 14.3 | ns |
| $t_{ENHSZ}$ | Enable to Pad, H/L to Z, High Slew | | 7.8 | | 8.7 | | 9.9 | | 11.6 | | 15.1 | ns |
| $t_{ENLSZ}$ | Enable to Pad, H/L to Z, Low Slew | | 7.4 | | 8.3 | | 9.4 | | 11.0 | | 14.3 | ns |
| $t_{CKHS}$ | IOCLK Pad to Pad H/L, High Slew | | 9.0 | | 9.0 | | 10.0 | | 11.5 | | 15.0 | ns |
| $t_{CKLS}$ | IOCLK Pad to Pad H/L, Low Slew | | 12.8 | | 12.8 | | 15.3 | | 17.0 | | 22.1 | ns |
| $d_{TLHHS}$ | Delta Low to High, High Slew | | 0.02 | | 0.02 | | 0.03 | | 0.03 | | 0.04 | ns/pF |
| $d_{TLHLS}$ | Delta Low to High, Low Slew | | 0.05 | | 0.05 | | 0.06 | | 0.07 | | 0.09 | ns/pF |
| $d_{THLHS}$ | Delta High to Low, High Slew | | 0.04 | | 0.04 | | 0.04 | | 0.05 | | 0.07 | ns/pF |
| $d_{THLLS}$ | Delta High to Low, Low Slew | | 0.05 | | 0.05 | | 0.06 | | 0.07 | | 0.09 | ns/pF |
| **I/O Module – CMOS Output Timing[1]** | | | | | | | | | | | | |
| $t_{DHS}$ | Data to Pad, High Slew | | 6.2 | | 7.0 | | 7.9 | | 9.3 | | 12.1 | ns |
| $t_{DLS}$ | Data to Pad, Low Slew | | 11.7 | | 13.1 | | 14.9 | | 17.5 | | 22.8 | ns |
| $t_{ENZHS}$ | Enable to Pad, Z to H/L, High Slew | | 5.2 | | 5.9 | | 6.6 | | 7.8 | | 10.1 | ns |
| $t_{ENZLS}$ | Enable to Pad, Z to H/L, Low Slew | | 8.9 | | 10.0 | | 11.3 | | 13.3 | | 17.3 | ns |
| $t_{ENHSZ}$ | Enable to Pad, H/L to Z, High Slew | | 7.4 | | 8.3 | | 9.4 | | 11.0 | | 14.3 | ns |
| $t_{ENLSZ}$ | Enable to Pad, H/L to Z, Low Slew | | 7.4 | | 8.3 | | 9.4 | | 11.0 | | 14.3 | ns |
| $t_{CKHS}$ | IOCLK Pad to Pad H/L, High Slew | | 10.4 | | 10.4 | | 12.1 | | 13.8 | | 17.9 | ns |
| $t_{CKLS}$ | IOCLK Pad to Pad H/L, Low Slew | | 14.5 | | 14.5 | | 17.4 | | 19.3 | | 25.1 | ns |
| $d_{TLHHS}$ | Delta Low to High, High Slew | | 0.04 | | 0.04 | | 0.05 | | 0.06 | | 0.08 | ns/pF |
| $d_{TLHLS}$ | Delta Low to High, Low Slew | | 0.07 | | 0.08 | | 0.09 | | 0.11 | | 0.14 | ns/pF |
| $d_{THLHS}$ | Delta High to Low, High Slew | | 0.03 | | 0.03 | | 0.03 | | 0.04 | | 0.05 | ns/pF |
| $d_{THLLS}$ | Delta High to Low, Low Slew | | 0.04 | | 0.04 | | 0.04 | | 0.05 | | 0.07 | ns/pF |

*Notes:*

1. *Delays based on 35 pF loading.*
2. *The –2 and –3 speed grades have been discontinued. Refer to PDN 0104, PDN 0203, PDN 0604, and PDN 1004 at http://www.microsemi.com/soc/support/notifications/default.aspx#pdn.*

# Pin Descriptions

**CLKA Clock A (Input)**

Clock input for clock distribution networks. The Clock input is buffered prior to clocking the logic modules. This pin can also be used as an I/O.

**CLKB Clock B (Input)**

Clock input for clock distribution networks. The Clock input is buffered prior to clocking the logic modules. This pin can also be used as an I/O.

**GND Ground**

LOW supply voltage.

**HCLK Dedicated (Hard-wired) Array Clock (Input)**

Clock input for sequential modules. This input is directly wired to each S-Module and offers clock speeds independent of the number of S-Modules being driven. This pin can also be used as an I/O.

**I/O Input/Output (Input, Output)**

The I/O pin functions as an input, output, three-state, or bidirectional buffer. Input and output levels are compatible with standard TTL and CMOS specifications. Unused I/O pins are tristated by the Designer Series software.

**IOCLK Dedicated (Hard-wired) I/O Clock (Input)**

Clock input for I/O modules. This input is directly wired to each I/O module and offers clock speeds independent of the number of I/O modules being driven. This pin can also be used as an I/O.

**IOPCL Dedicated (Hard-wired) I/O Preset/Clear (Input)**

Input for I/O preset or clear. This global input is directly wired to the preset and clear inputs of all I/O registers. This pin functions as an I/O when no I/O preset or clear macros are used.

**MODE Mode (Input)**

The MODE pin controls the use of diagnostic pins (DCLK, PRA, PRB, SDI). When the MODE pin is HIGH, the special functions are active. When the MODE pin is LOW, the pins function as I/Os. To provide Actionprobe capability, the MODE pin should be terminated to GND through a 10K resistor so that the MODE pin can be pulled high when required.

**NC No Connection**

This pin is not connected to circuitry within the device.

**PRA Probe A (Output)**

The Probe A pin is used to output data from any user-defined design node within the device. This independent diagnostic pin can be used in conjunction with the Probe B pin to allow real-time diagnostic output of any signal path within the device. The Probe A pin can be used as a user-defined I/O when debugging has been completed. The pin's probe capabilities can be permanently disabled to protect programmed design confidentiality. PRA is accessible when the MODE pin is HIGH. This pin functions as an I/O when the MODE pin is LOW.

**PRB Probe B (Output)**

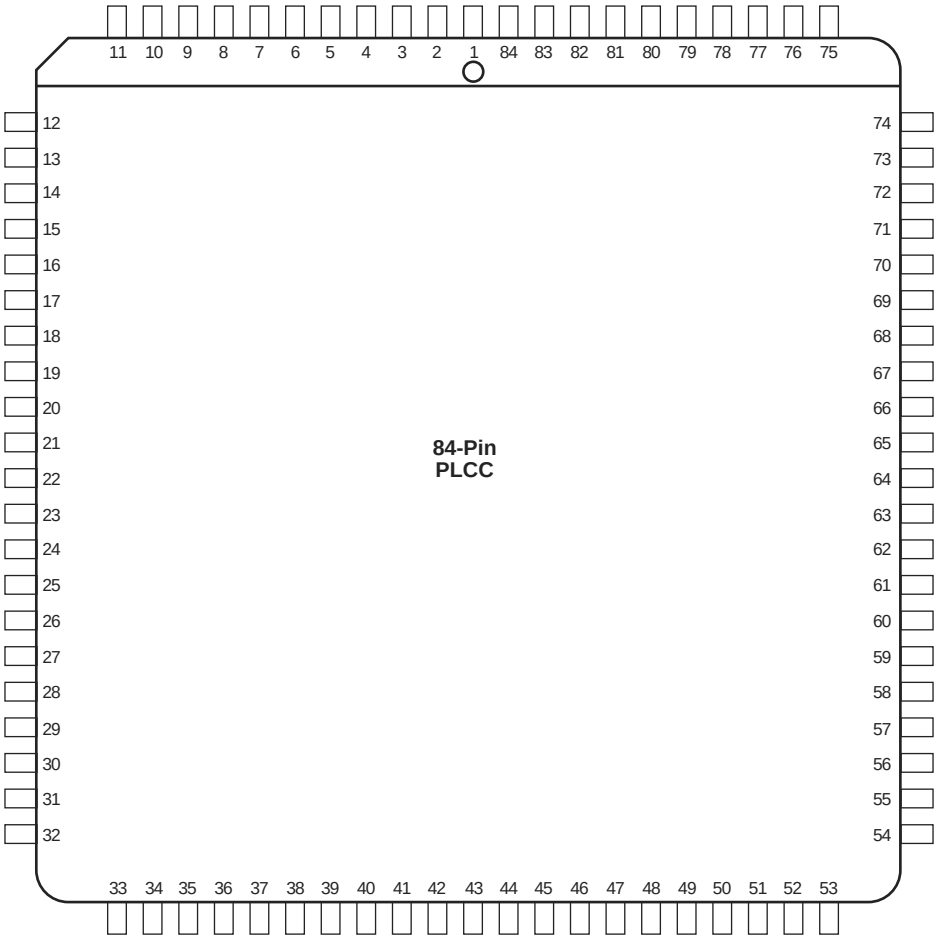
The Probe B pin is used to output data from any user-defined design node within the device. This independent diagnostic pin can be used in conjunction with the Probe A pin to allow real-time diagnostic output of any signal path within the device. The Probe B pin can be used as a user-defined I/O when debugging has been completed. The pin's probe capabilities can be permanently disabled to protect programmed design confidentiality. PRB is accessible when the MODE pin is HIGH. This pin functions as an I/O when the MODE pin is LOW.

**SDI Serial Data Input (Input)**

Serial data input for diagnostic probe and device programming. SDI is active when the MODE pin is HIGH. This pin functions as an I/O when the MODE pin is LOW.

# 3 – Package Pin Assignments

## PL84




*Note: This is the top view of the package.*

### *Note*

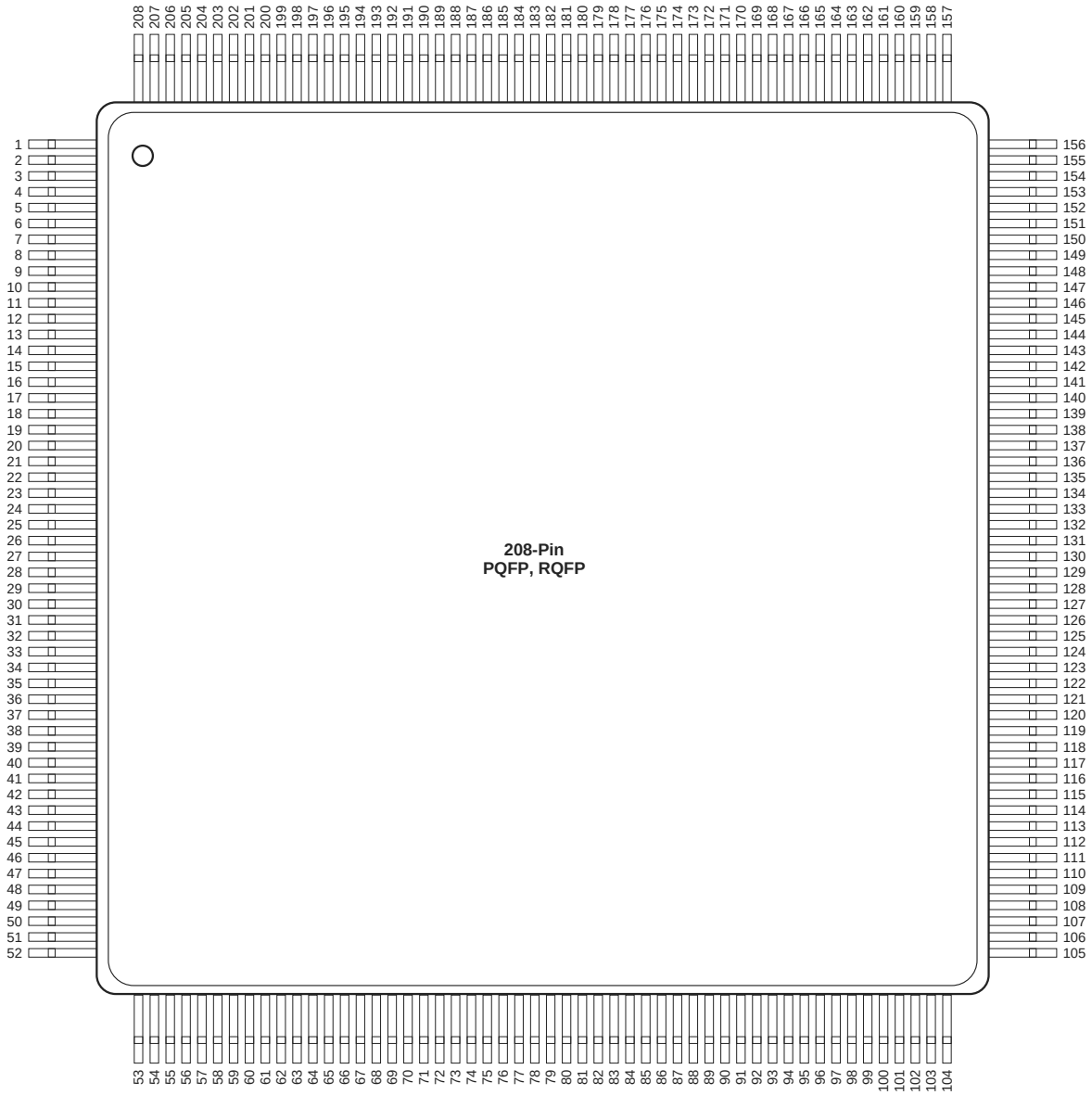
For Package Manufacturing and Environmental information, visit the Resource Center at http://www.microsemi.com/soc/products/solutions/package/docs.aspx.

| PQ100 | | |
|---|---|---|
| **Pin Number** | **A1415 Function** | **A1425 Function** |
| 2 | IOCLK, I/O | IOCLK, I/O |
| 14 | CLKA, I/O | CLKA, I/O |
| 15 | CLKB, I/O | CLKB, I/O |
| 16 | VCC | VCC |
| 17 | GND | GND |
| 18 | VCC | VCC |
| 19 | GND | GND |
| 20 | PRA, I/O | PRA, I/O |
| 27 | DCLK, I/O | DCLK, I/O |
| 28 | GND | GND |
| 29 | SDI, I/O | SDI, I/O |
| 34 | MODE | MODE |
| 35 | VCC | VCC |
| 36 | GND | GND |
| 47 | GND | GND |
| 48 | VCC | VCC |
| 61 | PRB, I/O | PRB, I/O |
| 62 | GND | GND |
| 63 | VCC | VCC |
| 64 | GND | GND |
| 65 | VCC | VCC |
| 67 | HCLK, I/O | HCLK, I/O |
| 77 | SDO | SDO |
| 78 | IOPCL, I/O | IOPCL, I/O |
| 79 | GND | GND |
| 85 | VCC | VCC |
| 86 | VCC | VCC |
| 87 | GND | GND |
| 96 | VCC | VCC |
| 97 | GND | GND |

*Notes:*

1. All unlisted pin numbers are user I/Os.
2. NC denotes no connection.
3. MODE should be terminated to GND through a 10K resistor to enable Actionprobe usage; otherwise it can be terminated directly to GND.

# PQ208, RQ208

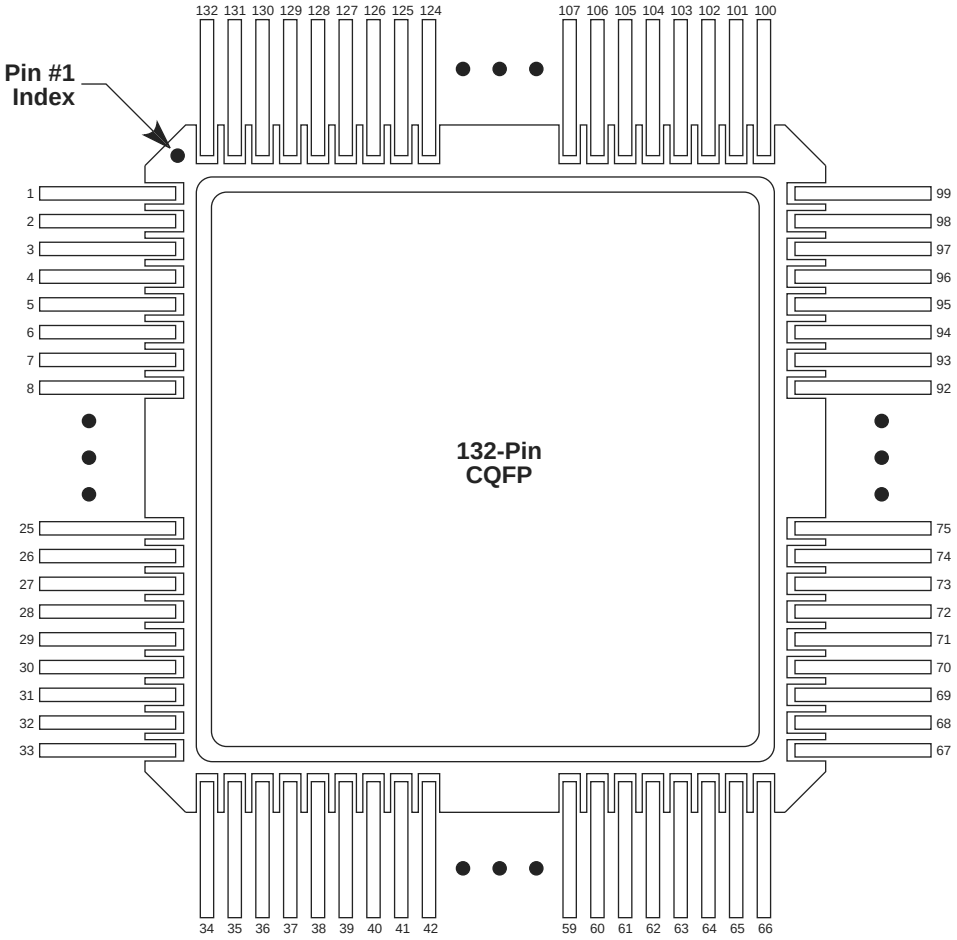



*Note: This is the top view of the package*

## Note

For Package Manufacturing and Environmental information, visit the Resource Center at http://www.microsemi.com/soc/products/solutions/package/docs.aspx

# CQ132




*Note: This is the top view*

## Note

For Package Manufacturing and Environmental information, visit the Resource Center at http://www.microsemi.com/soc/products/solutions/package/docs.aspx

| BG225 | |
|---|---|
| **A1460 Function** | **Location** |
| CLKA or I/O | C8 |
| CLKB or I/O | B8 |
| DCLK or I/O | B2 |
| GND | A1, A15, D15, F8, G7, G8, G9, H6, H7, H8, H9, H10, J7, J8, J9, K8, P2, R15 |
| HCLK or I/O | P9 |
| IOCLK or I/O | B14 |
| IOPCL or I/O | P14 |
| MODE | D1 |
| NC | A11, B5, B7, D8, D12, F6, F11, H1, H12, H14, K11, L1, L13, N8, P5, R1, R8, R11, R14 |
| PRA or I/O | A7 |
| PRB or I/O | L7 |
| SDI or I/O | D4 |
| SDO | N13 |
| VCC | A8, B12, D5, D14, E3, E8, E13, H2, H3, H11, H15, K4, L2, L12, M8, M15, P4, P8, R13 |

*Notes:*

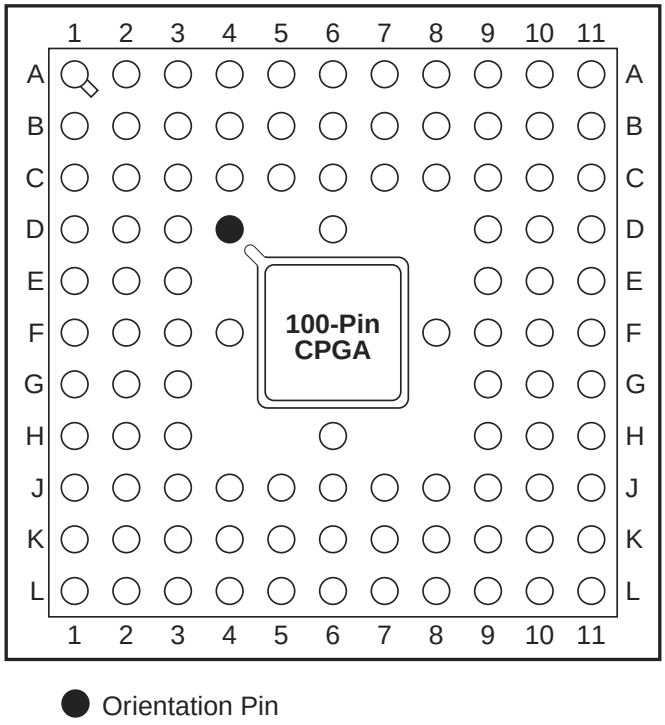
1. All unlisted pin numbers are user I/Os.
2. NC denotes no connection.
3. MODE should be terminated to GND through a 10K resistor to enable Actionprobe usage; otherwise it can be terminated directly to GND.
4. The BG225 package has been discontinued.

| BG313 | |
|---|---|
| **A14100, A14V100 Function** | **Location** |
| CLKA or I/O | J13 |
| CLKB or I/O | G13 |
| DCLK or I/O | B2 |
| GND | A1, A25, AD2, AE25, J21, L13, M12, M14, N11, N13, N15, P12, P14, R13 |
| HCLK or I/O | T14 |
| IOCLK or I/O | B24 |
| IOPCL or I/O | AD24 |
| MODE | G3 |
| NC | A3, A13, A23, AA5, AA9, AA23, AB2, AB4, AB20, AC13, AC25, AD22, AE1, AE21, B14, C5, C25, D4, D24, E3, E21, F6, F10, F16, G1, G25, H18, H24, J1, J7, J25, K12, L15, L17, M6, N1, N5, N7, N21, N23, P20, R11, T6, T8, U9, U13, U21, V16, W7, Y20, Y24 |
| PRA or I/O | H12 |
| PRB or I/O | AD12 |
| SDI or I/O | C1 |
| SDO | AE23 |
| VCC | AB18, AD6, AE13, C13, C19, E13, G9, H22, K8, K20, M16, N3, N9, N25, U5, W13, V2, V22, V24 |

*Notes:*

1. All unlisted pin numbers are user I/Os.
2. NC denotes no connection.
3. MODE should be terminated to GND through a 10K resistor to enable Actionprobe usage; otherwise it can be terminated directly to GND.

# PG100




*Note: This is the top view.*

## Note

For Package Manufacturing and Environmental information, visit the Resource Center at http://www.microsemi.com/soc/products/solutions/package/docs.aspx

| PG175 | |
|---|---|
| **A1440 Function** | **Location** |
| CLKA or I/O | C9 |
| CLKB or I/O | A9 |
| DCLK or I/O | D5 |
| GND | D4, D8, D11, D12, E4, E14, H4, H12, L4, L12, M4, M8, M12 |
| HCLK or I/O | R8 |
| IOCLK or I/O | E12 |
| IOPCL or I/O | P13 |
| MODE | F3 |
| NC | A1, A2, A15, B2, B3, P2, P14, R1, R2, R14, R15 |
| PRA or I/O | B8 |
| PRB or I/O | R7 |
| SDI or I/O | D3 |
| SDO | N12 |
| VCC | C3, C8, C13, E15, H3, H13, L1, L14, N3, N8, N13 |

*Notes:*

1. All unlisted pin numbers are user I/Os.
2. NC denotes no connection.
3. MODE should be terminated to GND through a 10K resistor to enable Actionprobe usage; otherwise it can be terminated directly to GND.
4. The PG175 package has been discontinued.

| PG257 | |
|---|---|
| **A14100 Function** | **Location** |
| CLKA or I/O | L4 |
| CLKB or I/O | L5 |
| DCLK or I/O | E4 |
| GND | B16, C4, D4, D10, D16, E11, J5, K4, K16, L15, R4, T4, T10, T16, T17, X7 |
| HCLK or I/O | J16 |
| IOCLK or I/O | T5 |
| IOPCL or I/O | R16 |
| MODE | A5 |
| NC | E5 |
| PRA or I/O | J1 |
| PRB or I/O | J17 |
| SDI or I/O | B4 |
| SDO | R17 |
| VCC | C3, C10, C13, C17, K3, K17, V3, V7, V10, V17, X14 |

*Notes:*

1. All unlisted pin numbers are user I/Os.
2. NC denotes no connection.
3. MODE should be terminated to GND through a 10K resistor to enable Actionprobe usage; otherwise it can be terminated directly to GND.

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