



Welcome to <u>E-XFL.COM</u>

Understanding <u>Embedded - FPGAs (Field</u> <u>Programmable Gate Array)</u>

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Details	
Product Status	Obsolete
Number of LABs/CLBs	310
Number of Logic Elements/Cells	-
Total RAM Bits	-
Number of I/O	70
Number of Gates	2500
Voltage - Supply	4.5V ~ 5.5V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 70°C (TA)
Package / Case	84-LCC (J-Lead)
Supplier Device Package	84-PLCC (29.31x29.31)
Purchase URL	https://www.e-xfl.com/product-detail/microsemi/a1425a-1pl84c

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

Microsemi

Accelerator Series FPGAs – ACT 3 Family

	Speed Grade ¹				Applic	ation ¹		
Device/Package	Std.	-1	-2	-3	С	I	м	В
A14V40A Device							•	
84-Pin Plastic Leaded Chip Carrier (PLCC)	1	-	-	_	1	_	_	_
100-Pin Very Thin Quad Flatpack (VQFP)	✓	-	-	-	1	-	-	-
160-Pin Plastic Quad Flatpack (PQFP)	~	-	-	-	✓	-	-	-
176-Pin Thin Quad Flatpack (TQFP)	~	-	-	-	✓	-	-	-
A1460A Device		•		I			1	
160-Pin Plastic Quad Flatpack (PQFP)	✓	✓	D	D	1	1	-	-
176-Pin Thin Quad Flatpack (TQFP)	✓	~	D	D	✓	~	-	-
196-Pin Ceramic Quad Flatpack (CQFP)	1	1	-	_	1	-	1	1
207-Pin Ceramic Pin Grid Array (CPGA)	1	1	D	D	1	-	1	1
208-Pin Plastic Quad Flatpack (PQFP)	1	 ✓ 	D	D	1	1	-	_
225-Pin Plastic Ball Grid Array (BGA)	D	D	D	D	D	-	-	-
A14V60A Device					-		-	
160-Pin Plastic Quad Flatpack (PQFP)	~	-	-	_	~	-	_	-
176-Pin Thin Quad Flatpack (TQFP)	✓	-	-	-	1	-	-	-
208-Pin Plastic Quad Flatpack (PQFP)	✓	-	-	_	~	-	_	_
A14100A Device								
208-Pin Power Quad Flatpack (RQFP)	✓	~	D	D	~	~	_	_
257-Pin Ceramic Pin Grid Array (CPGA)	~	~	D	D	~	-	~	~
313-Pin Plastic Ball Grid Array (BGA)	~	~	D	D	~	-	_	-
256-Pin Ceramic Quad Flatpack (CQFP)	✓	~	-	_	~	-	~	~
A14V100A Device								
208-Pin Power Quad Flatpack (RQFP)	\checkmark	_	_	_	1	_	_	_
313-Pin Plastic Ball Grid Array (BGA)	✓	-	-	-	1	-	-	-

Notes:

1. Applications: C = CommercialI = Industrial
 M = Military
 Commercial only

- Availability:
- ✓ = Available
- P = Planned- = Not planned
- D = Discontinued

Speed Grade:

-1 = Approx. 15% faster than Std. -2 = Approx. 25% faster than Std. -3 = Approx. 35% faster than Std. (-2 and -3 speed grades have been discontinued.)

Plastic Device Resources

Device	Logic		User I/Os								
Series	Modules	Gates	PL84	PQ100	PQ160	PQ/RQ208	VQ100	TQ176	BG225*	BG313	
A1415	200	1500	70	80	_	-	80	-	_	_	
A1425	310	2500	70	80	100	-	83	-	-	-	
A1440	564	4000	70	_	131	-	83	140	_	_	
A1460	848	6000	_	_	131	167	_	151	168	_	
A14100	1377	10000	_	-	-	175	-	-	_	228	

Note: *Discontinued

Hermetic Device Resources

Device	Logic		User I/Os							
Series	Modules	Gates	PG100*	PG133*	PG175*	PG207	PG257	CQ132	CQ196	CQ256
A1415	200	1500	80	-	_	_	_	_	_	_
A1425	310	2500	-	100	-	-	-	100	-	-
A1440	564	4000	-	-	140	_	_	_	_	_
A1460	848	6000	-	-	-	168	-	-	168	-
A14100	1377	10000	_	_	_	-	228	-	_	228

Note: *Discontinued

Contact your local Microsemi SoC Products Group (formerly Actel) representative for device availability: http://www.microsemi.com/soc/contact/default.aspx.

Antifuse Connections

An antifuse is a "normally open" structure as opposed to the normally closed fuse structure used in PROMs or PALs. The use of antifuses to implement a programmable logic device results in highly testable structures as well as an efficient programming architecture. The structure is highly testable because there are no preexisting connections; temporary connections can be made using pass transistors. These temporary connections can isolate individual antifuses to be programmed as well as isolate individual circuit structures to be tested. This can be done both before and after programming. For example, all metal tracks can be tested for continuity and shorts between adjacent tracks, and the functionality of all logic modules can be verified.

Four types of antifuse connections are used in the routing structure of the ACT 3 array. (The physical structure of the antifuse is identical in each case; only the usage differs.)

Table 2-1 shows four types of antifuses.

Table 2-1 •	Antifuse	Types
-------------	----------	-------

Туре	Description
XF	Horizontal-to-vertical connection
HF	Horizontal-to-horizontal connection
VF	Vertical-to-vertical connection
FF	"Fast" vertical connection

Examples of all four types of connections are shown in Figure 2-7 on page 2-6 and Figure 2-8 on page 2-6.

Module Interface

Connections to Logic and I/O modules are made through vertical segments that connect to the module inputs and outputs. These vertical segments lie on vertical tracks that span the entire height of the array.

Module Input Connections

The tracks dedicated to module inputs are segmented by pass transistors in each module row. During normal user operation, the pass transistors are inactive, which isolates the inputs of a module from the inputs of the module directly above or below it. During certain test modes, the pass transistors are active to verify the continuity of the metal tracks. Vertical input segments span only the channel above or the channel below. The logic modules are arranged such that half of the inputs are connected to the channel above and half of the inputs to segments in the channel below, as shown in Figure 2-9.



Figure 2-9 • Logic Module Routing Interface

Package Thermal Characteristics

The device junction to case thermal characteristic is θ jc, and the junction to ambient air characteristic is θ ja. The thermal characteristics for θ ja are shown with two different air flow rates.

Maximum junction temperature is 150°C.

A sample calculation of the absolute maximum power dissipation allowed for a CPGA 175-pin package at commercial temperature and still air is as follows:

$$\frac{\text{Max. junction temp. (°C)} - \text{Max. ambient temp. (°C)}}{\theta_{ja} °C/W} = \frac{150°C - 70°C}{25°C/W} = 3.2 \text{ W}$$

EQ 2

Package Type∗	Pin Count	θ_{jc}	θ _{ja} Still Air	θ _{ja} 300 ft./min.	Units
Ceramic Pin Grid Array	100	20	35	17	°C/W
	133	20	30	15	°C/W
	175	20	25	14	°C/W
	207	20	22	13	°C/W
	257	20	15	8	°C/W
Ceramic Quad Flatpack	132	13	55	30	°C/W
	196	13	36	24	°C/W
	256	13	30	18	°C/W
Plastic Quad Flatpack	100	13	51	40	°C/W
	160	10	33	26	°C/W
	208	10	33	26	°C/W
Very Thin Quad Flatpack	100	12	43	35	°C/W
Thin Quad Flatpack	176	11	32	25	°C/W
Power Quad Flatpack	208	0.4	17	13	°C/W
Plastic Leaded Chip Carrier	84	12	37	28	°C/W
Plastic Ball Grid Array	225	10	25	19	°C/W
	313	10	23	17	°C/W

Table 2-8 • Package Thermal Characteristics

Note: Maximum power dissipation in still air:

PQ160 = 2.4 W PQ208 = 2.4 W PQ100 = 1.6 W VQ100 = 1.9 W TQ176 = 2.5 W PL84 = 2.2 W RQ208 = 4.7 W BG225 = 3.2 W BG313 = 3.5 W

Accelerator Series FPGAs – ACT 3 Family

Equivalent capacitance is calculated by measuring ICC active at a specified frequency and voltage for each circuit component of interest. Measurements have been made over a range of frequencies at a fixed value of VCC. Equivalent capacitance is frequency independent so that the results may be used over a wide range of operating conditions. Equivalent capacitance values are shown in Figure 2-10.

Item	CEQ Value
Modules (C _{EQM})	6.7
Input Buffers (C _{EQI})	7.2
Output Buffers (C _{EQO})	10.4
Routed Array Clock Buffer Loads (C _{EQCR})	1.6
Dedicated Clock Buffer Loads (C _{EQCD})	0.7
I/O Clock Buffer Loads (C _{EQCI)}	0.9

To calculate the active power dissipated from the complete design, the switching frequency of each part of the logic must be known. EQ 5 shows a piece-wise linear summation over all components.

Power =VCC² * [(m * C_{EQM} * f_m)_{modules} + (n * C_{EQI} * f_n) inputs

+ ($p * (C_{EQO} + C_L) * f_p$)outputs

+ 0.5 * (q1 * C_{EQCR} * f_{q1})_{routed_Clk1} + (r1 * fq1)_{routed_Clk1}

+ 0.5 * (q2 * C_{EQCR} * fq2)_{routed_Clk2}

+ $(r_2 * f_{q2})_{routed_Clk2}$ + 0.5 * $(s_1 * C_{EQCD} * f_{s1})_{dedicated_Clk}$

+ (s₂ * C_{EQCI} * f_{s2})_{IO_CIk}]

Where: m = Number of logic modules switching at fm n = Number of input buffers switching at fn p = Number of output buffers switching at f_p q1 = Number of clock loads on the first routed array clock q2 = Number of clock loads on the second routed array clock r_1 = Fixed capacitance due to first routed array clock r₂ = Fixed capacitance due to second routed array clock s₁ = Fixed number of clock loads on the dedicated array clock s2 = Fixed number of clock loads on the dedicated I/O clock C_{FOM} = Equivalent capacitance of logic modules in pF C_{EQI} = Equivalent capacitance of input buffers in pF C_{EOO} = Equivalent capacitance of output buffers in pF C_{EOCR} = Equivalent capacitance of routed array clock in pF C_{EQCD} = Equivalent capacitance of dedicated array clock in pF C_{EOCI} = Equivalent capacitance of dedicated I/O clock in pF C₁ = Output lead capacitance in pF f_m = Average logic module switching rate in MHz fn = Average input buffer switching rate in MHz f_p = Average output buffer switching rate in MHz f_{q1} = Average first routed array clock rate in MHz $f_{\alpha 2}$ = Average second routed array clock rate in MHz f_{s1} = Average dedicated array clock rate in MHz f_{s2} = Average dedicated I/O clock rate in MHz

EQ 5

Timing Derating

ACT 3 devices are manufactured in a CMOS process. Therefore, device performance varies according to temperature, voltage, and process variations. Minimum timing parameters reflect maximum operating voltage, minimum operating temperature, and best-case processing. Maximum timing parameters reflect minimum operating voltage, maximum operating temperature, and worst-case processing.

Table 2-15 • Timing Derating Factor (Temperature and Voltage)

(Commercial Minimum/Maximum Specification) x	Indus	strial	Military		
	Min.	Max.	Min.	Max.	
	0.66	1.07	0.63	1.17	

Table 2-16 • Timing Derating Factor for Designs at Typical Temperature ($T_J = 25^{\circ}C$) and Voltage (5.0 V)

(Commercial Maximum Specification) x	0.85

Table 2-17 • Temperature and Voltage Derating Factors

(normalized to Worst-Case Commercial, TJ = 4.75 V, 70°C)

	-55	-40	0	25	70	85	125
4.50	0.72	0.76	0.85	0.90	1.04	1.07	1.117
4.75	0.70	0.73	0.82	0.87	1.00	1.03	1.12
5.00	0.68	0.71	0.79	0.84	0.97	1.00	1.09
5.25	0.66	0.69	0.77	0.82	0.94	0.97	1.06
5.50	0.63	0.66	0.74	0.79	0.90	0.93	1.01



Note: This derating factor applies to all routing and propagation delays.





A1415A, A14V15A Timing Characteristics

Table 2-18 • A1415A, A14V15A Worst-Case Commercial Conditions, VCC = 4.75 V, T_J = 70°C¹

Logic N	Iodule Propagation Delays ²	–3 Speed ³		-2 S	beed ³	-1 Speed		Std. S	speed	3.3 V Speed ¹		Units
Parame	eter/Description	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t _{PD}	Internal Array Module		2.0		2.3		2.6		3.0		3.9	ns
t _{CO}	Sequential Clock to Q		2.0		2.3		2.6		3.0		3.9	ns
t _{CLR}	Asynchronous Clear to Q		2.0		2.3		2.6		3.0		3.9	ns
Predict	ed Routing Delays ⁴			-								
t _{RD1}	FO = 1 Routing Delay		0.9		1.0		1.1		1.3		1.7	ns
t _{RD2}	FO = 2 Routing Delay		1.2		1.4		1.6		1.8		2.4	ns
t _{RD3}	FO = 3 Routing Delay		1.4		1.6		1.8		2.1		2.8	ns
t _{RD4}	FO = 4 Routing Delay		1.7		1.9		2.2		2.5		3.3	ns
t _{RD8}	FO = 8 Routing Delay		2.8		3.2		3.6		4.2		5.5	ns
Logic N	Iodule Sequential Timing			-			-		-	-		-
t _{SUD}	Flip-Flop Data Input Setup	0.5		0.6		0.7		0.8		0.8		ns
t _{HD}	Flip-Flop Data Input Hold	0.0		0.0		0.0		0.0		0.0		ns
t _{SUD}	Latch Data Input Setup	0.5		0.6		0.7		0.8		0.8		ns
t _{HD}	Latch Data Input Hold	0.0		0.0		0.0		0.0		0.0		ns
t _{WASYN}	Asynchronous Pulse Width	1.9		2.4		3.2		3.8		4.8		ns
t _{WCLKA}	Flip-Flop Clock Pulse Width	1.9		2.4		3.2		3.8		4.8		ns
t _A	Flip-Flop Clock Input Period	4.0		5.0		6.8		8.0		10.0		ns
f _{MAX}	Flip-Flop Clock Frequency		250		200		150		125		100	MHz

Notes:

1. VCC = 3.0 V for 3.3 V specifications.

2. For dual-module macros, use $t_{PD} + t_{RD1} + t_{PDn} + t_{CO} + t_{RD1} + t_{PDn}$ or $t_{PD1} + t_{RD1} + t_{SUD}$, whichever is appropriate.

3. The –2 and –3 speed grades have been discontinued. Please refer to the Product Discontinuation Notices (PDNs) listed below:

PDN March 2001 PDN 0104 PDN 0203 PDN 0604 PDN 1004

4. Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual worst-case performance. Post-route timing is based on actual routing delay measurements performed on the device prior to shipment.

A1415A, A14V15A Timing Characteristics (continued)

Table 2-19 • A1415A,	A14V15A Worst-Case	Commercial Conditions,	$VCC = 4.75 V, T_1 = 70^{\circ}C$

I/O Mod	lule Input Propagation Delays	-3 Sp	beed ¹	–2 Speed ¹		-1 Speed		Std. Speed		3.3 V Speed ²		Units
Parame	eter/Description	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t _{INY}	Input Data Pad to Y		2.8		3.2		3.6		4.2		5.5	ns
t _{ICKY}	Input Reg IOCLK Pad to Y		4.7		5.3		6.0		7.0		9.2	ns
t _{OCKY}	Output Reg IOCLK Pad to Y		4.7		5.3		6.0		7.0		9.2	ns
t _{ICLRY}	Input Asynchronous Clear to Y		4.7		5.3		6.0		7.0		9.2	ns
t _{OCLRY}	Output Asynchronous Clear to Y		4.7		5.3		6.0		7.0		9.2	ns
Predict	ed Input Routing Delays ²						•					
t _{RD1}	FO = 1 Routing Delay		0.9		1.0		1.1		1.3		1.7	ns
t _{RD2}	FO = 2 Routing Delay		1.2		1.4		1.6		1.8		2.4	ns
t _{RD3}	FO = 3 Routing Delay		1.4		1.6		1.8		2.1		2.8	ns
t _{RD4}	FO = 4 Routing Delay		1.7		1.9		2.2		2.5		3.3	ns
t _{RD8}	FO = 8 Routing Delay		2.8		3.2		3.6		4.2		5.5	ns
I/O Mod	ule Sequential Timing (wrt IOCLK	oad)		•								
t _{INH}	Input F-F Data Hold	0.0		0.0		0.0		0.0		0.0		ns
t _{INSU}	Input F-F Data Setup	2.0		2.3		2.5		3.0		3.0		ns
t _{IDEH}	Input Data Enable Hold	0.0		0.0		0.0		0.0		0.0		ns
t _{IDESU}	Input Data Enable Setup	5.8		6.5		7.5		8.6		8.6		ns
t _{OUTH}	Output F-F Data hold	0.7		0.8		0.9		1.0		1.0		ns
t _{OUTSU}	Output F-F Data Setup	0.7		0.8		0.9		1.0		1.0		ns
t _{ODEH}	Output Data Enable Hold	0.3		0.4		0.4		0.5		0.5		ns
f _{ODESU}	Output Data Enable Setup	1.3		1.5		1.7		2.0		2.0		ns

Notes:

1. The –2 and –3 speed grades have been discontinued. Please refer to the Product Discontinuation Notices (PDNs) listed below:

PDN March 2001 PDN 0104 PDN 0203 PDN 0604 PDN 1004

 Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual worst-case performance. Post-route timing is based on actual routing delay measurements performed on the device prior to shipment.



A1425A, A14V25A Timing Characteristics (continued)

Table 2-24 • A1425A, A14V25A Worst-Case Commercial Conditions, VCC = 4.75 V, T_J = 70°C

I/O Mod	dule – TTL Output Timing ¹	-3 Sp	beed ²	-2 Sp	beed ²	–1 S	peed	Std.	Speed	3.3 V Speed ¹		Units
Parame	eter/Description	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t _{DHS}	Data to Pad, High Slew		5.0		5.6		6.4		7.5		9.8	ns
t _{DLS}	Data to Pad, Low Slew		8.0		9.0		10.2		12.0		15.6	ns
t _{ENZHS}	Enable to Pad, Z to H/L, High Slew		4.0		4.5		5.1		6.0		7.8	ns
t _{ENZLS}	Enable to Pad, Z to H/L, Low Slew		7.4		8.3		9.4		11.0		14.3	ns
t _{ENHSZ}	Enable to Pad, H/L to Z, High Slew		6.5		7.5		8.5		10.0		13.0	ns
t _{ENLSZ}	Enable to Pad, H/L to Z, Low Slew		6.5		7.5		8.5		10.0		13.0	ns
t _{CKHS}	IOCLK Pad to Pad H/L, High Slew		7.5		7.5		9.0		10.0		13.0	ns
t _{CKLS}	IOCLK Pad to Pad H/L, Low Slew		11.3		11.3		13.5		15.0		19.5	ns
d _{TLHHS}	Delta Low to High, High Slew		0.02		0.02		0.03		0.03		0.04	ns/pF
d _{TLHLS}	Delta Low to High, Low Slew		0.05		0.05		0.06		0.07		0.09	ns/pF
d _{THLHS}	Delta High to Low, High Slew		0.04		0.04		0.04		0.05		0.07	ns/pF
d _{THLLS}	Delta High to Low, Low Slew		0.05		0.05		0.06		0.07		0.09	ns/pF
I/O Moo	dule – CMOS Output Timing ¹			-					-	-		
t _{DHS}	Data to Pad, High Slew		6.2		7.0		7.9		9.3		12.1	ns
t _{DLS}	Data to Pad, Low Slew		11.7		13.1		14.9		17.5		22.8	ns
t _{ENZHS}	Enable to Pad, Z to H/L, High Slew		5.2		5.9		6.6		7.8		10.1	ns
t _{ENZLS}	Enable to Pad, Z to H/L, Low Slew		8.9		10.0		11.3		13.3		17.3	ns
t _{ENHSZ}	Enable to Pad, H/L to Z, High Slew		6.7		7.5		8.5		10.0		13.0	ns
t _{ENLSZ}	Enable to Pad, H/L to Z, Low Slew		6.7		7.5		9.0		10.0		13.0	ns
t _{CKHS}	IOCLK Pad to Pad H/L, High Slew		8.9		8.9		10.7		11.8		15.3	ns
t _{CKLS}	IOCLK Pad to Pad H/L, Low Slew		13.0		13.0		15.6		17.3		22.5	ns
d _{TLHHS}	Delta Low to High, High Slew		0.04		0.04		0.05		0.06		0.08	ns/pF
d _{TLHLS}	Delta Low to High, Low Slew		0.07		0.08		0.09		0.11		0.14	ns/pF
d _{THLHS}	Delta High to Low, High Slew		0.03		0.03		0.03		0.04		0.05	ns/pF
d _{THLLS}	Delta High to Low, Low Slew		0.04		0.04		0.04		0.05		0.07	ns/pF

Notes: *

1. Delays based on 35 pF loading.

2. The –2 and –3 speed grades have been discontinued. Refer to PDN 0104, PDN 0203, PDN 0604, and PDN 1004 at http://www.microsemi.com/soc/support/notifications/default.aspx#pdn.



A1440A, A14V40A Timing Characteristics (continued)

Table 2-28 • A1440A, A14V40A Worst-Case Commercial Conditions, VCC = 4.75 V, T_J = 70°C

I/O Mod	dule – TTL Output Timing ¹	-3 Sp	beed ²	-2 Sp	beed ²	–1 S	peed	Std.	Speed	3.3 V Speed ¹		Units
Parame	eter/Description	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t _{DHS}	Data to Pad, High Slew		5.0		5.6		6.4		7.5		9.8	ns
t _{DLS}	Data to Pad, Low Slew		8.0		9.0		10.2		12.0		15.6	ns
t _{ENZHS}	Enable to Pad, Z to H/L, High Slew		4.0		4.5		5.1		6.0		7.8	ns
t _{ENZLS}	Enable to Pad, Z to H/L, Low Slew		7.4		8.3		9.4		11.0		14.3	ns
t _{ENHSZ}	Enable to Pad, H/L to Z, High Slew		7.4		8.3		9.4		11.0		14.3	ns
t _{ENLSZ}	Enable to Pad, H/L to Z, Low Slew		7.4		8.3		9.4		11.0		14.3	ns
t _{CKHS}	IOCLK Pad to Pad H/L, High Slew		8.5		8.5		9.5		11.0		14.3	ns
t _{CKLS}	IOCLK Pad to Pad H/L, Low Slew		11.3		11.3		13.5		15.0		19.5	ns
d _{TLHHS}	Delta Low to High, High Slew		0.02		0.02		0.03		0.03		0.04	ns/pF
d _{TLHLS}	Delta Low to High, Low Slew		0.05		0.05		0.06		0.07		0.09	ns/pF
d _{THLHS}	Delta High to Low, High Slew		0.04		0.04		0.04		0.05		0.07	ns/pF
d _{THLLS}	Delta High to Low, Low Slew		0.05		0.05		0.06		0.07		0.09	ns/pF
I/O Mod	dule – CMOS Output Timing ¹			-					-	-		
t _{DHS}	Data to Pad, High Slew		6.2		7.0		7.9		9.3		12.1	ns
t _{DLS}	Data to Pad, Low Slew		11.7		13.1		14.9		17.5		22.8	ns
t _{ENZHS}	Enable to Pad, Z to H/L, High Slew		5.2		5.9		6.6		7.8		10.1	ns
t _{ENZLS}	Enable to Pad, Z to H/L, Low Slew		8.9		10.0		11.3		13.3		17.3	ns
t _{ENHSZ}	Enable to Pad, H/L to Z, High Slew		7.4		8.3		9.4		11.0		14.3	ns
t _{ENLSZ}	Enable to Pad, H/L to Z, Low Slew		7.4		8.3		9.4		11.0		14.3	ns
t _{CKHS}	IOCLK Pad to Pad H/L, High Slew		9.0		9.0		10.1		11.8		14.3	ns
t _{CKLS}	IOCLK Pad to Pad H/L, Low Slew		13.0		13.0		15.6		17.3		22.5	ns
d _{TLHHS}	Delta Low to High, High Slew		0.04		0.04		0.05		0.06		0.08	ns/pF
d _{TLHLS}	Delta Low to High, Low Slew		0.07		0.08		0.09		0.11		0.14	ns/pF
d _{THLHS}	Delta High to Low, High Slew		0.03		0.03		0.03		0.04		0.05	ns/pF
d _{THLLS}	Delta High to Low, Low Slew		0.04		0.04		0.04		0.05		0.07	ns/pF

Notes:

1. Delays based on 35 pF loading.

2. The –2 and –3 speed grades have been discontinued. Refer to PDN 0104, PDN 0203, PDN 0604, and PDN 1004 at http://www.microsemi.com/soc/support/notifications/default.aspx#pdn.



A1460A, A14V60A Timing Characteristics (continued)

Table 2-32 • A1460A, A14V60A Worst-Case Commercial Conditions, VCC = 4.75 V, T_J = 70°C

I/O Mod	dule – TTL Output Timing ¹	-3 Sp	beed ²	-2 Sp	beed ²	–1 S	peed	Std.	Speed	3.3 V Speed ¹		Units
Parame	eter/Description	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t _{DHS}	Data to Pad, High Slew		5.0		5.6		6.4		7.5		9.8	ns
t _{DLS}	Data to Pad, Low Slew		8.0		9.0		10.2		12.0		15.6	ns
t _{ENZHS}	Enable to Pad, Z to H/L, High Slew		4.0		4.5		5.1		6.0		7.8	ns
t _{ENZLS}	Enable to Pad, Z to H/L, Low Slew		7.4		8.3		9.4		11.0		14.3	ns
t _{ENHSZ}	Enable to Pad, H/L to Z, High Slew		7.8		8.7		9.9		11.6		15.1	ns
t _{ENLSZ}	Enable to Pad, H/L to Z, Low Slew		7.4		8.3		9.4		11.0		14.3	ns
t _{CKHS}	IOCLK Pad to Pad H/L, High Slew		9.0		9.0		10.0		11.5		15.0	ns
t _{CKLS}	IOCLK Pad to Pad H/L, Low Slew		12.8		12.8		15.3		17.0		22.1	ns
d _{TLHHS}	Delta Low to High, High Slew		0.02		0.02		0.03		0.03		0.04	ns/pF
d _{TLHLS}	Delta Low to High, Low Slew		0.05		0.05		0.06		0.07		0.09	ns/pF
d _{THLHS}	Delta High to Low, High Slew		0.04		0.04		0.04		0.05		0.07	ns/pF
d _{THLLS}	Delta High to Low, Low Slew		0.05		0.05		0.06		0.07		0.09	ns/pF
I/O Mod	dule – CMOS Output Timing ¹			•								
t _{DHS}	Data to Pad, High Slew		6.2		7.0		7.9		9.3		12.1	ns
t _{DLS}	Data to Pad, Low Slew		11.7		13.1		14.9		17.5		22.8	ns
t _{ENZHS}	Enable to Pad, Z to H/L, High Slew		5.2		5.9		6.6		7.8		10.1	ns
t _{ENZLS}	Enable to Pad, Z to H/L, Low Slew		8.9		10.0		11.3		13.3		17.3	ns
t _{ENHSZ}	Enable to Pad, H/L to Z, High Slew		7.4		8.3		9.4		11.0		14.3	ns
t _{ENLSZ}	Enable to Pad, H/L to Z, Low Slew		7.4		8.3		9.4		11.0		14.3	ns
t _{CKHS}	IOCLK Pad to Pad H/L, High Slew		10.4		10.4		12.1		13.8		17.9	ns
t _{CKLS}	IOCLK Pad to Pad H/L, Low Slew		14.5		14.5		17.4		19.3		25.1	ns
d _{TLHHS}	Delta Low to High, High Slew		0.04		0.04		0.05		0.06		0.08	ns/pF
d _{TLHLS}	Delta Low to High, Low Slew		0.07		0.08		0.09		0.11		0.14	ns/pF
d _{THLHS}	Delta High to Low, High Slew		0.03		0.03		0.03		0.04		0.05	ns/pF
d _{THLLS}	Delta High to Low, Low Slew		0.04		0.04		0.04		0.05		0.07	ns/pF

Notes:

1. Delays based on 35 pF loading.

2. The –2 and –3 speed grades have been discontinued. Refer to PDN 0104, PDN 0203, PDN 0604, and PDN 1004 at http://www.microsemi.com/soc/support/notifications/default.aspx#pdn.

A1460A, A14V60A Timing Characteristics (continued)

Table 2-33 • A1460A	A14V60A Worst	-Case Commercia	Conditions.	VCC = 4.75 V. T.	= 70°C
$Iable 2-33 \cdot AI + 00A$	A1400A 1013			, voo = + ./5 v , ij	-100

Dedicate	d (hardwired) I/O Clock Network	-3 Sp	beed ¹	-2 Sp	beed ¹	–1 S	peed	Std.	Speed	3.3 V Speed ¹		Units
Paramete	er/Description	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t _{IOCKH}	Input Low to High (pad to I/O module input)		2.3		2.6		3.0		3.5		4.5	ns
t _{IOPWH}	Minimum Pulse Width High	2.4		3.2		3.8		4.8		6.5		ns
t _{IPOWL}	Minimum Pulse Width Low	2.4		3.2		3.8		4.8		6.5		ns
t _{IOSAPW}	Minimum Asynchronous Pulse Width	2.4		3.2		3.8		4.8		6.5		ns
t _{IOCKSW}	Maximum Skew		0.6		0.6		0.6		0.6		0.6	ns
t _{IOP}	Minimum Period	5.0		6.8		8.0		10.0		13.4		ns
f _{IOMAX}	Maximum Frequency		200		150		125		100		75	MHz
Dedicate	d (hardwired) Array Clock			•				•		-		
^t нскн	Input Low to High (pad to S-module input)		3.7		4.1		4.7		5.5		7.0	ns
t _{HCKL}	Input High to Low (pad to S-module input)		3.7		4.1		4.7		5.5		7.0	ns
t _{HPWH}	Minimum Pulse Width High	2.4		3.2		3.8		4.8		6.5		ns
t _{HPWL}	Minimum Pulse Width Low	2.4		3.2		3.8		4.8		6.5		ns
t _{HCKSW}	Delta High to Low, Low Slew		0.6		0.6		0.6		0.6		0.6	ns
t _{HP}	Minimum Period	5.0		6.8		8.0		10.0		13.4		ns
f _{HMAX}	Maximum Frequency		200		150		125		100		75	MHz
Routed A	rray Clock Networks											
t _{RCKH}	Input Low to High (FO = 64)		6.0		6.8		7.7		9.0		11.8	ns
t _{RCKL}	Input High to Low (FO = 64)		6.0		6.8		7.7		9.0		11.8	ns
t _{RPWH}	Min. Pulse Width High (FO = 64)	4.1		4.5		5.4		6.1		8.2		ns
t _{RPWL}	Min. Pulse Width Low (FO = 64)	4.1		4.5		5.4		6.1		8.2		ns
t _{RCKSW}	Maximum Skew (FO = 128)		1.2		1.4		1.6		1.8		1.8	ns
t _{RP}	Minimum Period (FO = 64)	8.3		9.3		11.1		12.5		16.7		ns
f _{RMAX}	Maximum Frequency (FO = 64)		120		105		90		80		60	MHz
Clock-to-	Clock Skews							-				
t _{IOHCKSW}	I/O Clock to H-Clock Skew	0.0	2.6	0.0	2.7	0.0	2.9	0.0	3.0	0.0	3.0	ns
t _{IORCKSW}	I/O Clock to R-Clock Skew (FO = 64) (FO = 216)	0.0 0.0	1.7 5.0	0.0 0.0	1.7 5.0	0.0 0.0	1.7 5.0	0.0 0.0	1.7 5.0	0.0 0.0	5.0 5.0	ns
t _{HRCKSW}	H-Clock to R-Clock Skew (FO = 64) (FO = 216)	0.0 0.0	1.3 3.0	0.0 0.0	1.0 3.0	0.0 0.0	1.0 3.0	0.0 0.0	1.0 3.0	0.0 0.0	1.0 3.0	ns

Notes:

1. The -2 and -3 speed grades have been discontinued. Refer to PDN 0104, PDN 0203, PDN 0604, and PDN 1004 at http://www.microsemi.com/soc/support/notifications/default.aspx#pdn.

2. Delays based on 35 pF loading.

Accelerator Series FPGAs – ACT 3 Family

SDO Serial Data Output (Output)

Serial data output for diagnostic probe. SDO is active when the MODE pin is High. This pin functions as an I/O when the MODE pin is Low.

DCLK Diagnostic Clock (Input)

Clock input for diagnostic probe and device programming. DCLK is active when the MODE pin is HIGH. This pin functions as an I/O when the MODE pin is LOW.

VCC 5 V Supply Voltage

HIGH supply voltage.

PQ160



Note: This is the top view of the package

Note

For Package Manufacturing and Environmental information, visit the Resource Center at http://www.microsemi.com/soc/products/solutions/package/docs.aspx



Package Pin Assignments

VQ100



Note: This is the top view.

Note

For Package Manufacturing and Environmental information, visit the Resource Center at http://www.microsemi.com/soc/products/solutions/package/docs.aspx

Microsemi

Accelerator Series FPGAs - ACT 3 Family

	CQ256		CQ256
Pin Number	A14100 Function	Pin Number	A14100 Function
1	GND	141	VCC
2	SDI, I/O	158	GND
11	MODE	159	VCC
28	VCC	160	GND
29	GND	161	VCC
30	VCC	174	VCC
31	GND	175	GND
46	VCC	176	GND
59	GND	188	IOCLK, I/O
90	PRB, I/O	189	GND
91	GND	219	CLKA, I/O
92	VCC	220	CLKB, I/O
93	GND	221	VCC
94	VCC	222	GND
96	HCLK, I/O	223	VCC
110	GND	224	GND
126	SDO	225	PRA, I/O
127	IOPCL, I/O	240	GND
128	GND	256	DCLK, I/O

Notes:

- 1. All unlisted pin numbers are user I/Os.
- 2. NC denotes no connection.
- 3. MODE should be terminated to GND through a 10K resistor to enable Actionprobe usage; otherwise it can be terminated directly to GND.

Package Pin Assignments

Microsemi

BG313



Note: This is the top view.

Note

For Package Manufacturing and Environmental information, visit the Resource Center at http://www.microsemi.com/soc/products/solutions/package/docs.aspx



Package Pin Assignments

PG257



Note: This is the top view.

Note

For Package Manufacturing and Environmental information, visit the Resource Center at http://www.microsemi.com/soc/products/solutions/package/docs.aspx

4 – Datasheet Information

List of Changes

The following table lists critical changes that were made in each version of the datasheet.

Revision	Changes	Page
Revision 3 (January 2012)	The description for SDO pins had earlier been removed from the datasheet and has now been included again, in the "Pin Descriptions" section (SAR 35820).	2-21
	SDO pin numbers had earlier been removed from package pin assignment tables in the datasheet, and have now been restored to the pin tables (SAR 35820).	3-1
Revision 2 (September 2011)	The ACT 3 datasheet was formatted newly in the style used for current datasheets. The same information is present (other than noted in the list of changes for this revision) but divided into chapters.	N/A
	The datasheet was revised to note in multiple places that speed grades -2 and -3 have been discontinued. The following device/package combinations have been discontinued for all speed grades and temperatures (SAR 33872): A1415 PG100 A1425 PG133 A1440 PG175 A1460 BG225 Refer to PDN 0104, PDN 0203, PDN 0604, and PDN 1004.	l and others
	The "Features" section was revised to state the clock-to-ouput time and on-chip performance for -1 speed grade as 9.0 ns and 186 MHz. The "General Description" section was revised in accordance (SAR 33872).	I
	The maximum performance values were updated in Table 1 \cdot ACT 3 Family Product Information, and now reflect worst-case commercial for the -1 speed grade (SAR 33872).	I
	The "Product Plan" table was updated as follows to conform to current offerings (SAR 33872): The A1415A device is offered in PL84, PG100, and VQ100 packages for Military application. The A1440A device is offered in TQ176 and VQ100 packages for Industrial application.	Ξ
	Table 1-1 • Chip-to-Chip Performance (worst-case commercial) was updated to include data for all speed grades instead of only –3 (SAR 33872).	1-2
	Figure 1-1 • Predictable Performance (worst-case commercial, –1 speed grade) was revised to reflect values for the –1 speed grade (SAR 33872).	1-1
	Figure 2-10 • Timing Model was updated to show data for the -1 speed grade instead of -3 (SAR 33872).	2-16
	Table 2-14 • Logic Module and Routing Delay by Fanout (ns); Worst-Case Commercial Conditions was updated to include data for all speed grades instead of only –3 (SAR 33872).	2-20
	Package names used in the "Package Pin Assignments" section and throughout the document were revised to match standards given in <i>Package Mechanical Drawings</i> (SAR 27395).	3-1



Microsemi Corporate Headquarters One Enterprise, Aliso Viejo CA 92656 USA Within the USA: +1 (949) 380-6100 Sales: +1 (949) 380-6136 Fax: +1 (949) 215-4996 Microsemi Corporation (NASDAQ: MSCC) offers a comprehensive portfolio of semiconductor solutions for: aerospace, defense and security; enterprise and communications; and industrial and alternative energy markets. Products include high-performance, high-reliability analog and RF devices, mixed signal and RF integrated circuits, customizable SoCs, FPGAs, and complete subsystems. Microsemi is headquartered in Aliso Viejo, Calif. Learn more at **www.microsemi.com**.

© 2012 Microsemi Corporation. All rights reserved. Microsemi and the Microsemi logo are trademarks of Microsemi Corporation. All other trademarks and service marks are the property of their respective owners.