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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications,

Details	
Product Status	Obsolete
Number of LABs/CLBs	310
Number of Logic Elements/Cells	-
Total RAM Bits	-
Number of I/O	100
Number of Gates	2500
Voltage - Supply	4.5V ~ 5.5V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 85°C (TA)
Package / Case	160-BQFP
Supplier Device Package	160-PQFP (28x28)
Purchase URL	https://www.e-xfl.com/product-detail/microsemi/a1425a-1pqg160i

Ordering Information

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A14100    A  –  1   RQ    G    208    C
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Application (Temperature Range)
C = Commercial (0 to +70°C)
I = Industrial (–40 to +85°C)
M = Military (–55 to +125°C)
B = MIL-STD-883

Package Lead Count

Lead-Free Packaging
Blank = Standard Packaging
G = RoHS Compliant Packaging

Package Type
PG = Ceramic Pin Grid Array
PL = Plastic Leaded Chip Carrier
PQ = Plastic Quad Flatpack
RQ = Plastic Power Quad Flatpack
VQ = Very Thin (1.0 mm) Quad Flatpack
TQ = Thin (1.4 mm) Quad Flatpack
CQ = Ceramic Quad Flatpack
BG = Plastic Ball Grid Array

Speed Grade
Std = Standard Speed
–1 = Approximately 15% faster than Standard
–2 = Approximately 25% faster than Standard
–3 = Approximately 35% faster than Standard

Die Revision
A = 1.0 mm CMOS Process

Part Number
A1415A = 1,500 Gates
A14V15A = 1,500 Gates (3.3 V)
A1425A = 2,500 Gates
A14V25A = 2,500 Gates (3.3 V)
A1440A = 4,000 Gates
A14V40A = 4,000 Gates (3.3 V)
A1460A = 6,000 Gates
A14V60A = 6,000 Gates (3.3 V)
A14100A = 10,000 Gates
A14V100A = 10,000 Gates (3.3 V)

Notes:
1. *The –2 and –3 speed grades have been discontinued.*
2. *The Ceramic Pin Grid Array packages PG100, PG133, and PG175 have been discontinued in all device densities, speed grades, and temperature grades.*
3. *The Plastic Ball Grid Array package BG225 has been discontinued in all device densities (specifically for A1460A), all speed grades, and all temperature grades.*
4. *Military Grade devices are no longer available for the A1440A device.*
5. *For more information about discontinued devices, refer to the Product Discontinuation Notices (PDNs) listed below, available on the Microsemi SoC Products Group website:*
PDN March 2001
PDN 0104
PDN 0203
PDN 0604
PDN 1004

Horizontal Routing

Horizontal channels are located between the rows of modules and are composed of several routing tracks. The horizontal routing tracks within the channel are divided into one or more segments. The minimum horizontal segment length is the width of a module-pair, and the maximum horizontal segment length is the full length of the channel. Any segment that spans more than one-third the row length is considered a long horizontal segment. A typical channel is shown in Figure 2-7. Undedicated horizontal routing tracks are used to route signal nets. Dedicated routing tracks are used for the global clock networks and for power and ground tie-off tracks.
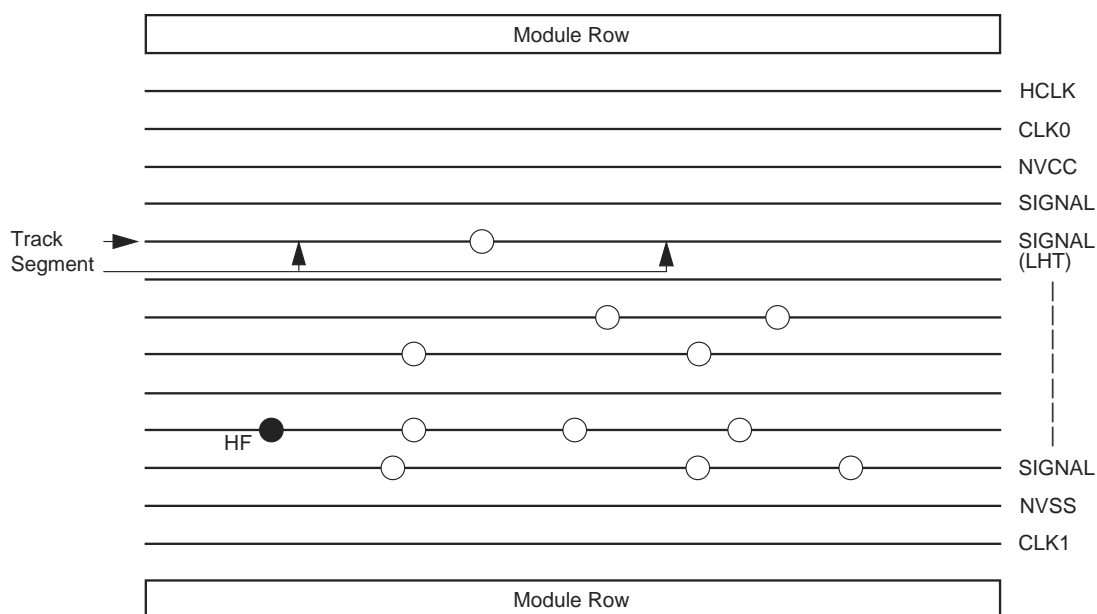

Figure 2-7 •   Horizontal Routing Tracks and Segments

Vertical Routing

Other tracks run vertically through the modules. Vertical tracks are of three types: input, output, and long. Vertical tracks are also divided into one or more segments. Each segment in an input track is dedicated to the input of a particular module. Each segment in an output track is dedicated to the output of a particular module. Long segments are uncommitted and can be assigned during routing. Each output segment spans four channels (two above and two below), except near the top and bottom of the array where edge effects occur. LVTs contain either one or two segments. An example of vertical routing tracks and segments is shown in Figure 2-8.
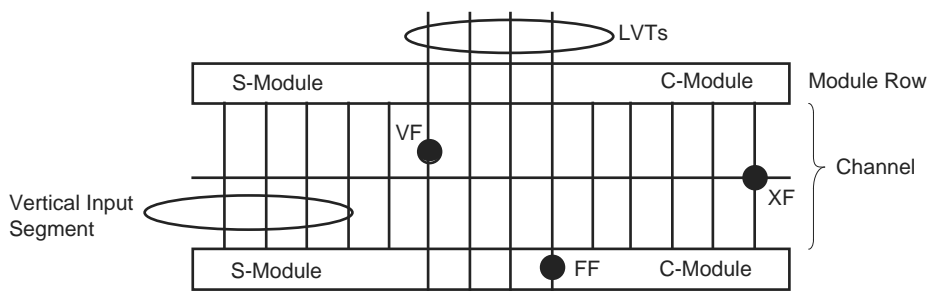

Figure 2-8 •   Vertical Routing Tracks and Segments

3.3 V Operating Conditions

Table 2-5 • **Absolute Maximum Ratings[1], Free Air Temperature Range**

Symbol	Parameter	Limits	Units
VCC	DC supply voltage	−0.5 to +7.0	V
VI	Input voltage	−0.5 to VCC + 0.5	V
VO	Output voltage	−0.5 to VCC + 0.5	V
IIO	I/O source sink current[2]	±20	mA
T$_{STG}$	Storage temperature	−65 to +150	°C

Notes:

1. *Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum rated conditions for extended periods may affect device reliability. Device should not be operated outside the recommended operating conditions.*
2. *Device inputs are normally high impedance and draw extremely low current. However, when input voltage is greater than VCC + 0.5 V for less than GND −0.5 V, the internal protection diodes will forward bias and can draw excessive current.*

Table 2-6 • **Recommended Operating Conditions**

Parameter	Commercial	Units
Temperature range*	0 to +70	°C
Power supply tolerance	3.0 to 3.6	V

*Note: *Ambient temperature (T_A) is used for commercial.*

Table 2-7 • **Electrical Specifications**

Parameter		Commercial		Units
		Min.	Max.	
VOH[1]	IOH = −4 mA	2.15	–	V
	IOH = −3.2 mA	2.4		V
VOL[1]	IOL = 6 mA		0.4	V
VIL		−0.3	0.8	V
VIH		2.0	VCC + 0.3	V
Input transition time t$_R$, t$_F$[2]	VI = VCC or GND	−10	+10	µA
C$_{IO}$ I/O Capacitance[2,3]			10	pF
Standby current, ICC[4] (typical = 0.3 mA)			0.75	mA
Leakage current[5]		−10	10	µA

1. *Only one output tested at a time. VCC = minimum.*
2. *Not tested; for information only.*
3. *Includes worst-case 84-pin PLCC package capacitance. VOUT = 0 V, f - 1 MHz.*
4. *Typical standby current = 0.3 mA. All outputs unloaded. All inputs = VCC or GND.*
5. *VO, VIN = VCC or GND*

Equivalent capacitance is calculated by measuring ICC active at a specified frequency and voltage for each circuit component of interest. Measurements have been made over a range of frequencies at a fixed value of VCC. Equivalent capacitance is frequency independent so that the results may be used over a wide range of operating conditions. Equivalent capacitance values are shown in Figure 2-10.

Table 2-10 • **CEQ Values for Microsemi FPGAs**

Item	CEQ Value
Modules (C_{EQM})	6.7
Input Buffers (C_{EQI})	7.2
Output Buffers (C_{EQO})	10.4
Routed Array Clock Buffer Loads (C_{EQCR})	1.6
Dedicated Clock Buffer Loads (C_{EQCD})	0.7
I/O Clock Buffer Loads (C_{EQCI})	0.9

To calculate the active power dissipated from the complete design, the switching frequency of each part of the logic must be known. EQ 5 shows a piece-wise linear summation over all components.

Power $= VCC^2 * [(m * C_{EQM} * f_m)_{modules} + (n * C_{EQI} * f_n)_{inputs}$

$+ (p * (C_{EQO} + C_L) * f_p)_{outputs}$

$+ 0.5 * (q1 * C_{EQCR} * f_{q1})_{routed\_Clk1} + (r1 * f_{q1})_{routed\_Clk1}$

$+ 0.5 * (q2 * C_{EQCR} * f_{q2})_{routed\_Clk2}$

$+ (r_2 * f_{q2})_{routed\_Clk2} + 0.5 * (s_1 * C_{EQCD} * f_{s1})_{dedicated\_Clk}$

$+ (s_2 * C_{EQCI} * f_{s2})_{IO\_Clk}]$

EQ 5

Where:

m = Number of logic modules switching at f_m

n = Number of input buffers switching at f_n

p = Number of output buffers switching at f_p

q1 = Number of clock loads on the first routed array clock

q2 = Number of clock loads on the second routed array clock

r_1 = Fixed capacitance due to first routed array clock

r_2 = Fixed capacitance due to second routed array clock

s_1 = Fixed number of clock loads on the dedicated array clock

s_2 = Fixed number of clock loads on the dedicated I/O clock

C_{EQM} = Equivalent capacitance of logic modules in pF

C_{EQI} = Equivalent capacitance of input buffers in pF

C_{EQO} = Equivalent capacitance of output buffers in pF

C_{EQCR} = Equivalent capacitance of routed array clock in pF

C_{EQCD} = Equivalent capacitance of dedicated array clock in pF

C_{EQCI} = Equivalent capacitance of dedicated I/O clock in pF

C_L = Output lead capacitance in pF

f_m = Average logic module switching rate in MHz

f_n = Average input buffer switching rate in MHz

f_p = Average output buffer switching rate in MHz

f_{q1} = Average first routed array clock rate in MHz

f_{q2} = Average second routed array clock rate in MHz

f_{s1} = Average dedicated array clock rate in MHz

f_{s2} = Average dedicated I/O clock rate in MHz

A1415A, A14V15A Timing Characteristics (continued)

Table 2-19 • **A1415A, A14V15A Worst-Case Commercial Conditions, VCC = 4.75 V, T$_J$ = 70°C**

I/O Module Input Propagation Delays		–3 Speed[1]		–2 Speed[1]		–1 Speed		Std. Speed		3.3 V Speed[2]		Units
Parameter/Description		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t$_{INY}$	Input Data Pad to Y		2.8		3.2		3.6		4.2		5.5	ns
t$_{ICKY}$	Input Reg IOCLK Pad to Y		4.7		5.3		6.0		7.0		9.2	ns
t$_{OCKY}$	Output Reg IOCLK Pad to Y		4.7		5.3		6.0		7.0		9.2	ns
t$_{ICLRY}$	Input Asynchronous Clear to Y		4.7		5.3		6.0		7.0		9.2	ns
t$_{OCLRY}$	Output Asynchronous Clear to Y		4.7		5.3		6.0		7.0		9.2	ns
Predicted Input Routing Delays[2]												
t$_{RD1}$	FO = 1 Routing Delay		0.9		1.0		1.1		1.3		1.7	ns
t$_{RD2}$	FO = 2 Routing Delay		1.2		1.4		1.6		1.8		2.4	ns
t$_{RD3}$	FO = 3 Routing Delay		1.4		1.6		1.8		2.1		2.8	ns
t$_{RD4}$	FO = 4 Routing Delay		1.7		1.9		2.2		2.5		3.3	ns
t$_{RD8}$	FO = 8 Routing Delay		2.8		3.2		3.6		4.2		5.5	ns
I/O Module Sequential Timing (wrt IOCLK pad)												
t$_{INH}$	Input F-F Data Hold	0.0		0.0		0.0		0.0		0.0		ns
t$_{INSU}$	Input F-F Data Setup	2.0		2.3		2.5		3.0		3.0		ns
t$_{IDEH}$	Input Data Enable Hold	0.0		0.0		0.0		0.0		0.0		ns
t$_{IDESU}$	Input Data Enable Setup	5.8		6.5		7.5		8.6		8.6		ns
t$_{OUTH}$	Output F-F Data hold	0.7		0.8		0.9		1.0		1.0		ns
t$_{OUTSU}$	Output F-F Data Setup	0.7		0.8		0.9		1.0		1.0		ns
t$_{ODEH}$	Output Data Enable Hold	0.3		0.4		0.4		0.5		0.5		ns
f$_{ODESU}$	Output Data Enable Setup	1.3		1.5		1.7		2.0		2.0		ns

Notes:

1. *The –2 and –3 speed grades have been discontinued. Please refer to the Product Discontinuation Notices (PDNs) listed below:*

    PDN March 2001
    PDN 0104
    PDN 0203
    PDN 0604
    PDN 1004

2. *Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual worst-case performance. Post-route timing is based on actual routing delay measurements performed on the device prior to shipment.*

Microsemi

A1415A, A14V15A Timing Characteristics (continued)

Table 2-20 • **A1415A, A14V15A Worst-Case Commercial Conditions, VCC = 4.75 V, T$_J$ = 70°C**

I/O Module – TTL Output Timing[1]		–3 Speed[2]		–2 Speed[2]		–1 Speed		Std. Speed		3.3 V Speed[1]		Units
Parameter/Description		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t$_{DHS}$	Data to Pad, High Slew		5.0		5.6		6.4		7.5		9.8	ns
t$_{DLS}$	Data to Pad, Low Slew		8.0		9.0		10.2		12.0		15.6	ns
t$_{ENZHS}$	Enable to Pad, Z to H/L, High Slew		4.0		4.5		5.1		6.0		7.8	ns
t$_{ENZLS}$	Enable to Pad, Z to H/L, Low Slew		7.4		8.3		9.4		11.0		14.3	ns
t$_{ENHSZ}$	Enable to Pad, H/L to Z, High Slew		6.5		7.5		8.5		10.0		13.0	ns
t$_{ENLSZ}$	Enable to Pad, H/L to Z, Low Slew		6.5		7.5		8.5		10.0		13.0	ns
t$_{CKHS}$	IOCLK Pad to Pad H/L, High Slew		7.5		7.5		9.0		10.0		13.0	ns
t$_{CKLS}$	IOCLK Pad to Pad H/L, Low Slew		11.3		11.3		13.5		15.0		19.5	ns
d$_{TLHHS}$	Delta Low to High, High Slew		0.02		0.02		0.03		0.03		0.04	ns/pF
d$_{TLHLS}$	Delta Low to High, Low Slew		0.05		0.05		0.06		0.07		0.09	ns/pF
d$_{THLHS}$	Delta High to Low, High Slew		0.04		0.04		0.04		0.05		0.07	ns/pF
d$_{THLLS}$	Delta High to Low, Low Slew		0.05		0.05		0.06		0.07		0.09	ns/pF
I/O Module – CMOS Output Timing[1]												
t$_{DHS}$	Data to Pad, High Slew		6.2		7.0		7.9		9.3		12.1	ns
t$_{DLS}$	Data to Pad, Low Slew		11.7		13.1		14.9		17.5		22.8	ns
t$_{ENZHS}$	Enable to Pad, Z to H/L, High Slew		5.2		5.9		6.6		7.8		10.1	ns
t$_{ENZLS}$	Enable to Pad, Z to H/L, Low Slew		8.9		10.0		11.3		13.3		17.3	ns
t$_{ENHSZ}$	Enable to Pad, H/L to Z, High Slew		6.7		7.5		8.5		10.0		13.0	ns
t$_{ENLSZ}$	Enable to Pad, H/L to Z, Low Slew		6.7		7.5		9.0		10.0		13.0	ns
t$_{CKHS}$	IOCLK Pad to Pad H/L, High Slew		8.9		8.9		10.7		11.8		15.3	ns
t$_{CKLS}$	IOCLK Pad to Pad H/L, Low Slew		13.0		13.0		15.6		17.3		22.5	ns
d$_{TLHHS}$	Delta Low to High, High Slew		0.04		0.04		0.05		0.06		0.08	ns/pF
d$_{TLHLS}$	Delta Low to High, Low Slew		0.07		0.08		0.09		0.11		0.14	ns/pF
d$_{THLHS}$	Delta High to Low, High Slew		0.03		0.03		0.03		0.04		0.05	ns/pF
d$_{THLLS}$	Delta High to Low, Low Slew		0.04		0.04		0.04		0.05		0.07	ns/pF

Notes:

1. Delays based on 35 pF loading.

2. The –2 and –3 speed grades have been discontinued. Please refer to the Product Discontinuation Notices (PDNs) listed below:

PDN March 2001
PDN 0104
PDN 0203
PDN 0604
PDN 1004

A1440A, A14V40A Timing Characteristics (continued)

Table 2-29 • **A1440A, A14V40A Worst-Case Commercial Conditions, VCC = 4.75 V, T$_J$ = 70°C**

Dedicated (hardwired) I/O Clock Network		–3 Speed[1]		–2 Speed[1]		–1 Speed		Std. Speed		3.3 V Speed[1]		Units
Parameter/Description		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t$_{IOCKH}$	Input Low to High (pad to I/O module input)		2.0		2.3		2.6		3.0		3.5	ns
t$_{IOPWH}$	Minimum Pulse Width High	1.9		2.4		3.3		3.8		4.8		ns
t$_{IPOWL}$	Minimum Pulse Width Low	1.9		2.4		3.3		3.8		4.8		ns
t$_{IOSAPW}$	Minimum Asynchronous Pulse Width	1.9		2.4		3.3		3.8		4.8		ns
t$_{IOCKSW}$	Maximum Skew		0.4		0.4		0.4		0.4		0.4	ns
t$_{IOP}$	Minimum Period	4.0		5.0		6.8		8.0		10.0		ns
f$_{IOMAX}$	Maximum Frequency		250		200		150		125		100	MHz
Dedicated (hardwired) Array Clock												
t$_{HCKH}$	Input Low to High (pad to S-module input)		3.0		3.4		3.9		4.5		5.5	ns
t$_{HCKL}$	Input High to Low (pad to S-module input)		3.0		3.4		3.9		4.5		5.5	ns
t$_{HPWH}$	Minimum Pulse Width High	1.9		2.4		3.3		3.8		4.8		ns
t$_{HPWL}$	Minimum Pulse Width Low	1.9		2.4		3.3		3.8		4.8		ns
t$_{HCKSW}$	Delta High to Low, Low Slew		0.3		0.3		0.3		0.3		0.3	ns
t$_{HP}$	Minimum Period	4.0		5.0		6.8		8.0		10.0		ns
f$_{HMAX}$	Maximum Frequency		250		200		150		125		100	MHz
Routed Array Clock Networks												
t$_{RCKH}$	Input Low to High (FO = 64)		3.7		4.1		4.7		5.5		9.0	ns
t$_{RCKL}$	Input High to Low (FO = 64)		4.0		4.5		5.1		6.0		9.0	ns
t$_{RPWH}$	Min. Pulse Width High (FO = 64)	3.3		3.8		4.2		4.9		6.5		ns
t$_{RPWL}$	Min. Pulse Width Low (FO = 64)	3.3		3.8		4.2		4.9		6.5		ns
t$_{RCKSW}$	Maximum Skew (FO = 128)		0.7		0.8		0.9		1.0		1.0	ns
t$_{RP}$	Minimum Period (FO = 64)	6.8		8.0		8.7		10.0		13.4		ns
f$_{RMAX}$	Maximum Frequency (FO = 64)		150		125		115		100		75	MHz
Clock-to-Clock Skews												
t$_{IOHCKSW}$	I/O Clock to H-Clock Skew	0.0	1.7	0.0	1.8	0.0	2.0	0.0	2.2	0.0	3.0	ns
t$_{IORCKSW}$	I/O Clock to R-Clock Skew (FO = 64) (FO = 144)	0.0 0.0	1.0 3.0	0.0 0.0	1.0 3.0	0.0 0.0	1.0 3.0	0.0 0.0	1.0 3.0	0.0 0.0	3.0 3.0	ns
t$_{HRCKSW}$	H-Clock to R-Clock Skew (FO = 64) (FO = 144)	0.0 0.0	1.0 3.0	0.0 0.0	1.0 3.0	0.0 0.0	1.0 3.0	0.0 0.0	1.0 3.0	0.0 0.0	1.0 3.0	ns

Notes:

1. *The –2 and –3 speed grades have been discontinued. Refer to PDN 0104, PDN 0203, PDN 0604, and PDN 1004 at http://www.microsemi.com/soc/support/notifications/default.aspx#pdn.*

2. *Delays based on 35 pF loading.*

A1460A, A14V60A Timing Characteristics (continued)

Table 2-31 • **A1460A, A14V60A Worst-Case Commercial Conditions, VCC = 4.75 V, T$_J$ = 70°C**

I/O Module Input Propagation Delays		–3 Speed[1]		–2 Speed[1]		–1 Speed		Std. Speed		3.3 V Speed[1]		Units
Parameter/Description		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t$_{INY}$	Input Data Pad to Y		2.8		3.2		3.6		4.2		5.5	ns
t$_{ICKY}$	Input Reg IOCLK Pad to Y		4.7		5.3		6.0		7.0		9.2	ns
t$_{OCKY}$	Output Reg IOCLK Pad to Y		4.7		5.3		6.0		7.0		9.2	ns
t$_{ICLRY}$	Input Asynchronous Clear to Y		4.7		5.3		6.0		7.0		9.2	ns
t$_{OCLRY}$	Output Asynchronous Clear to Y		4.7		5.3		6.0		7.0		9.2	ns
Predicted Input Routing Delays[2]												
t$_{RD1}$	FO = 1 Routing Delay		0.9		1.0		1.1		1.3		1.7	ns
t$_{RD2}$	FO = 2 Routing Delay		1.2		1.4		1.6		1.8		2.4	ns
t$_{RD3}$	FO = 3 Routing Delay		1.4		1.6		1.8		2.1		2.8	ns
t$_{RD4}$	FO = 4 Routing Delay		1.7		1.9		2.2		2.5		3.3	ns
t$_{RD8}$	FO = 8 Routing Delay		2.8		3.2		3.6		4.2		5.5	ns
I/O Module Sequential Timing (wrt IOCLK pad)												
t$_{INH}$	Input F-F Data Hold	0.0		0.0		0.0		0.0		0.0		ns
t$_{INSU}$	Input F-F Data Setup	1.3		1.5		1.8		2.0		2.0		ns
t$_{IDEH}$	Input Data Enable Hold	0.0		0.0		0.0		0.0		0.0		ns
t$_{IDESU}$	Input Data Enable Setup	5.8		6.5		7.5		8.6		8.6		ns
t$_{OUTH}$	Output F-F Data hold	0.7		0.8		0.9		1.0		1.0		ns
t$_{OUTSU}$	Output F-F Data Setup	0.7		0.8		0.9		1.0		1.0		ns
t$_{ODEH}$	Output Data Enable Hold	0.3		0.4		0.4		0.5		0.5		ns
f$_{ODESU}$	Output Data Enable Setup	1.3		1.5		1.7		2.0		2.0		ns

Notes:

5. *The –2 and –3 speed grades have been discontinued. Refer to PDN 0104, PDN 0203, PDN 0604, and PDN 1004 at http://www.microsemi.com/soc/support/notifications/default.aspx#pdn.*

6. *Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual worst-case performance. Post-route timing is based on actual routing delay measurements performed on the device prior to shipment.*

PQ100
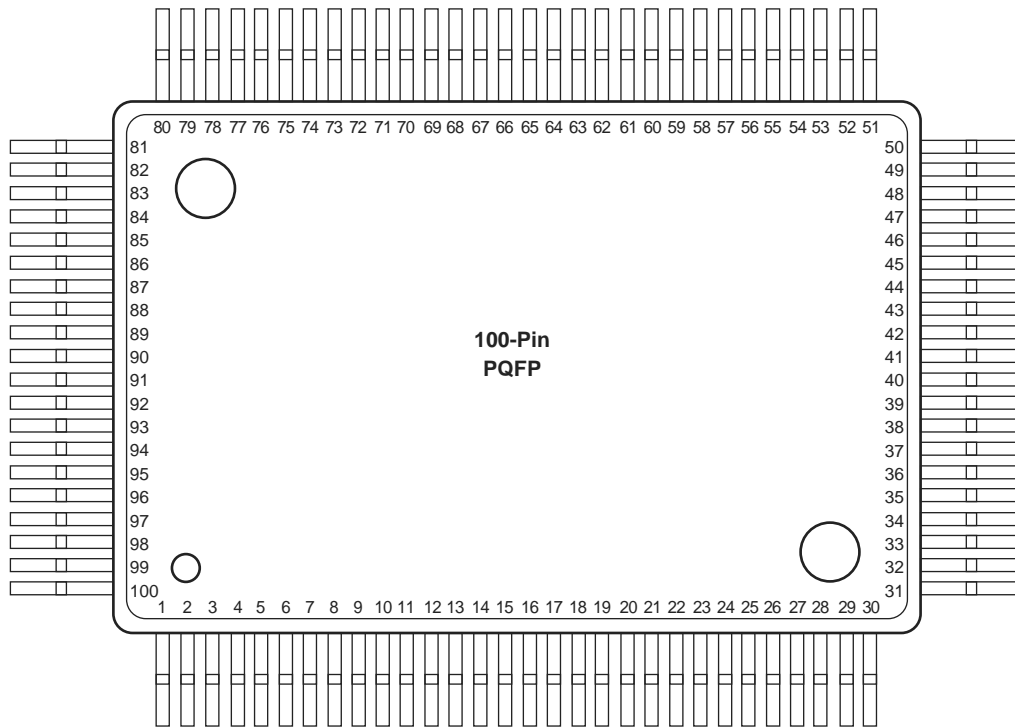
**100-Pin
PQFP**

Note: This is the top view of the package.

Note

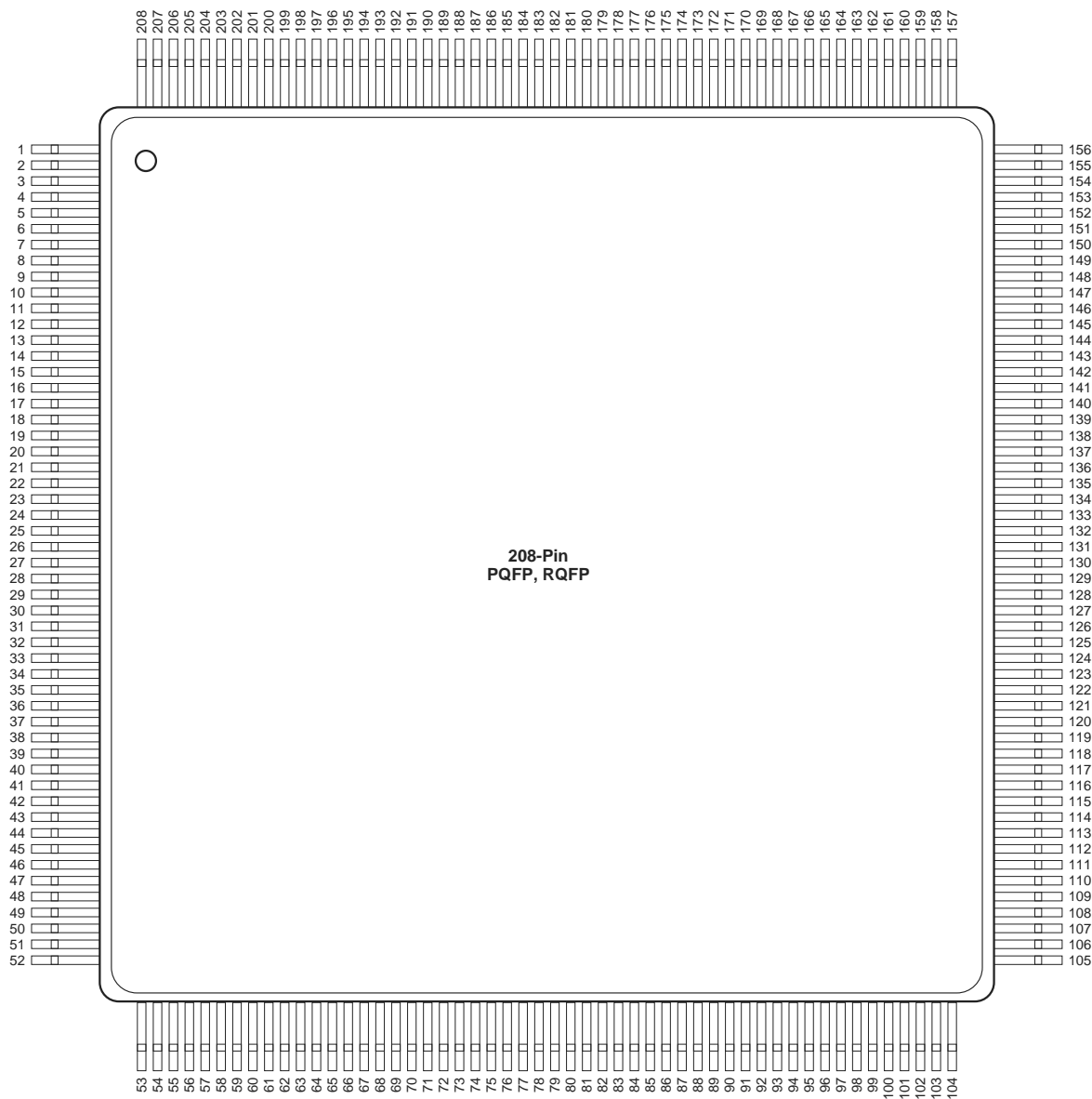For Package Manufacturing and Environmental information, visit the Resource Center at
http://www.microsemi.com/soc/products/solutions/package/docs.aspx

PQ160			
Pin Number	**A1425, A14V25 Function**	**A1440, A14V40 Function**	**A1460, A14V60 Function**
1	GND	GND	GND
2	SDI, I/O	SDI, I/O	SDI, I/O
5	NC	I/O	I/O
9	MODE	MODE	MODE
10	VCC	VCC	VCC
14	NC	I/O	I/O
15	GND	GND	GND
18	VCC	VCC	VCC
19	GND	GND	GND
20	NC	I/O	I/O
24	NC	I/O	I/O
27	NC	I/O	I/O
28	VCC	VCC	VCC
29	VCC	VCC	VCC
40	GND	GND	GND
41	NC	I/O	I/O
43	NC	I/O	I/O
45	NC	I/O	I/O
46	VCC	VCC	VCC
47	NC	I/O	I/O
49	NC	I/O	I/O
51	NC	I/O	I/O
53	NC	I/O	I/O
58	PRB, I/O	PRB, I/O	PRB, I/O
59	GND	GND	GND
60	VCC	VCC	VCC
62	HCLK, I/O	HCLK, I/O	HCLK, I/O
63	GND	GND	GND
74	NC	I/O	I/O
75	VCC	VCC	VCC
76	NC	I/O	I/O
77	NC	I/O	I/O
78	NC	I/O	I/O
79	SDO	SDO	SDO
80	IOPCL, I/O	IOPCL, I/O	IOPCL, I/O
81	GND	GND	GND
90	VCC	VCC	VCC
91	VCC	VCC	VCC

PQ160			
Pin Number	A1425, A14V25 Function	A1440, A14V40 Function	A1460, A14V60 Function
92	NC	I/O	I/O
93	NC	I/O	I/O
98	GND	GND	GND
99	VCC	VCC	VCC
100	NC	I/O	I/O
103	GND	GND	GND
107	NC	I/O	I/O
109	NC	I/O	I/O
110	VCC	VCC	VCC
111	GND	GND	GND
112	VCC	VCC	VCC
113	NC	I/O	I/O
119	NC	I/O	I/O
120	IOCLK, I/O	IOCLK, I/O	IOCLK, I/O
121	GND	GND	GND
124	NC	I/O	I/O
127	NC	I/O	I/O
136	CLKA, I/O	CLKA, I/O	CLKA, I/O
137	CLKB, I/O	CLKB, I/O	CLKB, I/O
138	VCC	VCC	VCC
139	GND	GND	GND
140	VCC	VCC	VCC
141	GND	GND	GND
142	PRA, I/O	PRA, I/O	PRA, I/O
143	NC	I/O	I/O
145	NC	I/O	I/O
147	NC	I/O	I/O
149	NC	I/O	I/O
151	NC	I/O	I/O
153	NC	I/O	I/O
154	VCC	VCC	VCC
160	DCLK, I/O	DCLK, I/O	DCLK, I/O

Notes:

1. All unlisted pin numbers are user I/Os.
2. NC denotes no connection.
3. MODE should be terminated to GND through a 10K resistor to enable Actionprobe usage; otherwise it can be terminated directly to GND.
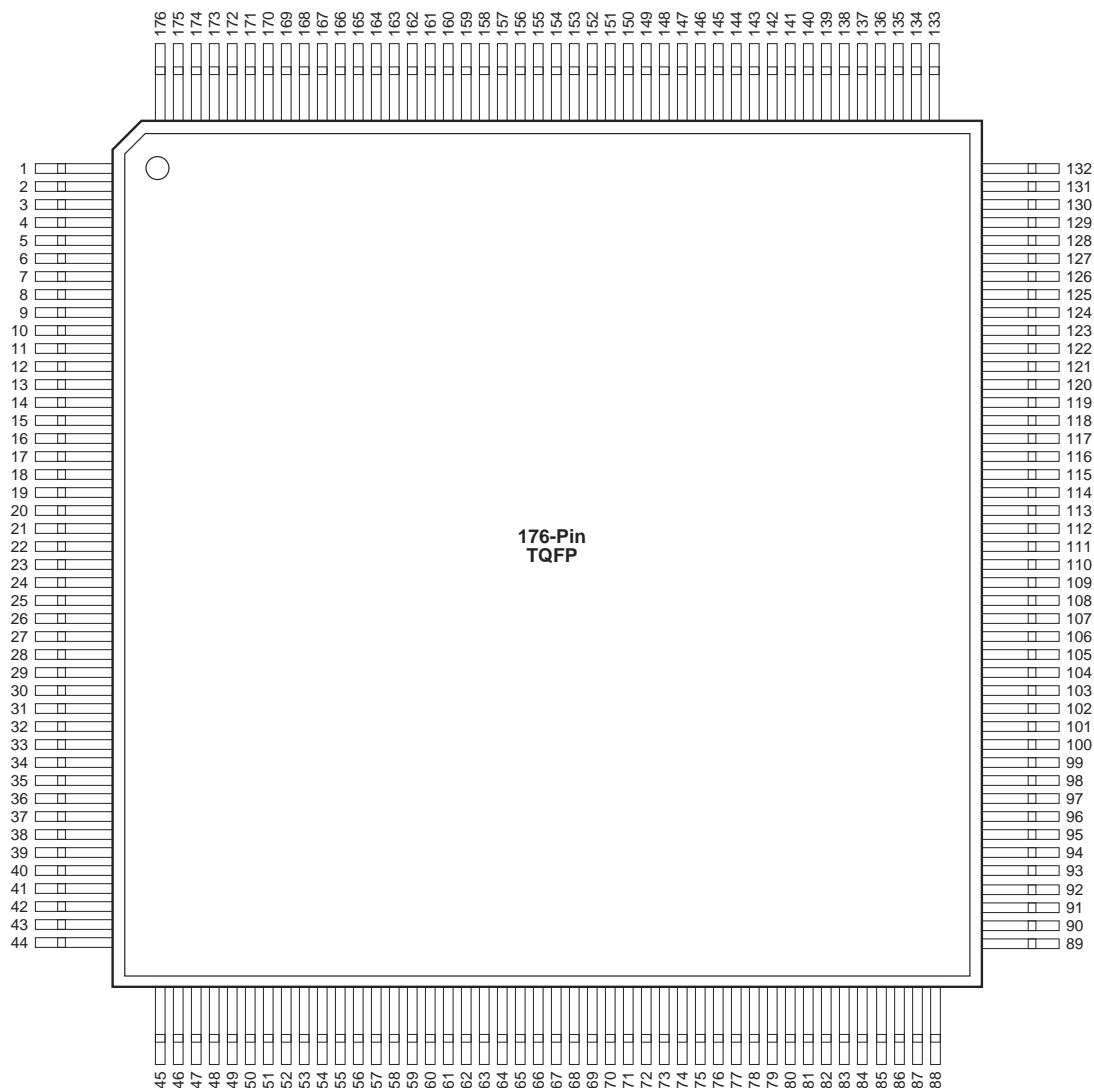
PQ208, RQ208

208-Pin
PQFP, RQFP

Note: This is the top view of the package

Note

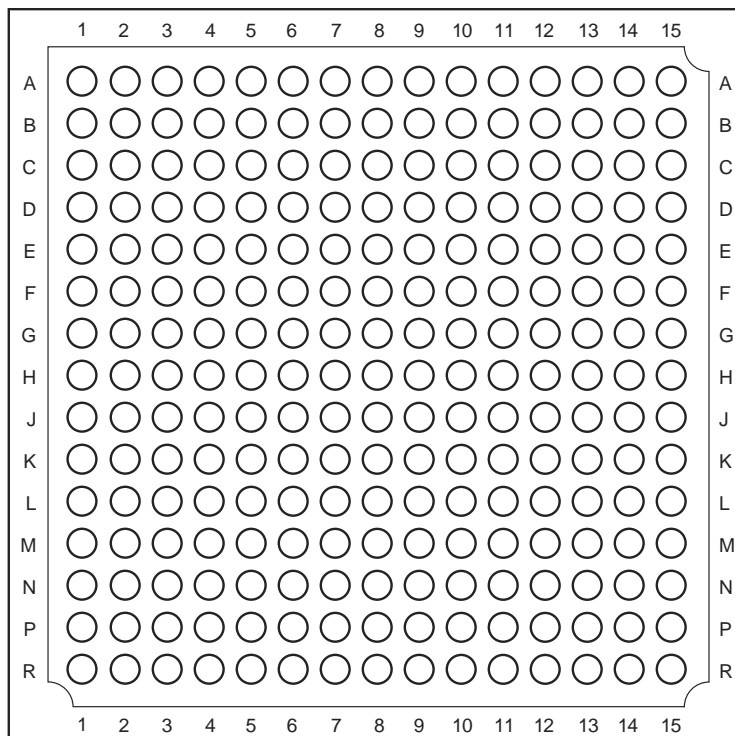For Package Manufacturing and Environmental information, visit the Resource Center at
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TQ176

Note: This is the top view.

Note

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CQ132		CQ132	
Pin Number	A1425 Function	Pin Number	A1425 Function
1	NC	67	NC
2	GND	74	GND
3	SDI, I/O	75	VCC
9	MODE	78	VCC
10	GND	89	VCC
11	VCC	90	GND
22	VCC	91	VCC
26	GND	92	GND
27	VCC	98	IOCLK, I/O
34	NC	99	NC
36	GND	100	NC
42	GND	101	GND
43	VCC	106	GND
48	PRB, I/O	107	VCC
50	HCLK, I/O	116	CLKA, I/O
58	GND	117	CLKB, I/O
59	VCC	118	PRA, I/O
63	SDO	122	GND
64	IOPCL, I/O	123	VCC
65	GND	131	DCLK, I/O
66	NC	132	NC

Notes:

1. All unlisted pin numbers are user I/Os.

2. NC denotes no connection.

3. MODE should be terminated to GND through a 10K resistor to enable Actionprobe usage; otherwise it can be terminated directly to GND.

BG225

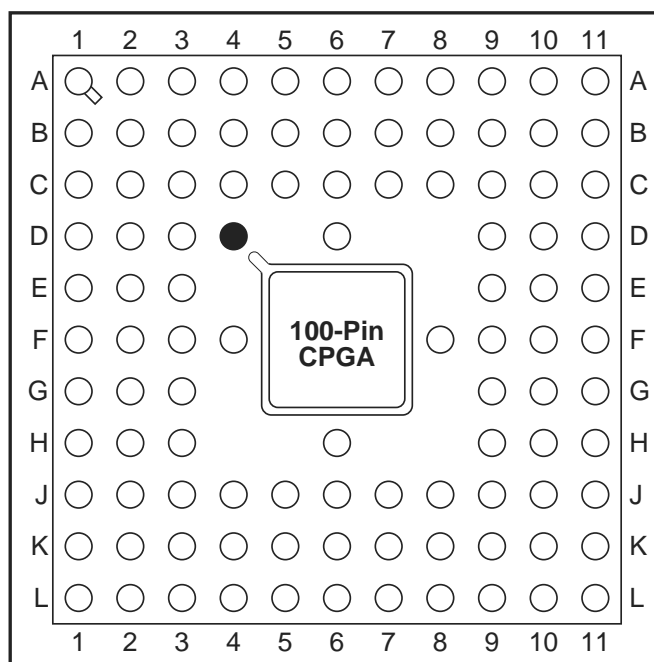

Note: This is the top view.

Note

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BG225	
A1460 Function	**Location**
CLKA or I/O	C8
CLKB or I/O	B8
DCLK or I/O	B2
GND	A1, A15, D15, F8, G7, G8, G9, H6, H7, H8, H9, H10, J7, J8, J9, K8, P2, R15
HCLK or I/O	P9
IOCLK or I/O	B14
IOPCL or I/O	P14
MODE	D1
NC	A11, B5, B7, D8, D12, F6, F11, H1, H12, H14, K11, L1, L13, N8, P5, R1, R8, R11, R14
PRA or I/O	A7
PRB or I/O	L7
SDI or I/O	D4
SDO	N13
VCC	A8, B12, D5, D14, E3, E8, E13, H2, H3, H11, H15, K4, L2, L12, M8, M15, P4, P8, R13

Notes:

1. All unlisted pin numbers are user I/Os.

2. NC denotes no connection.

3. MODE should be terminated to GND through a 10K resistor to enable Actionprobe usage; otherwise it can be terminated directly to GND.

4. The BG225 package has been discontinued.

PG100

● Orientation Pin

Note: This is the top view.

Note

For Package Manufacturing and Environmental information, visit the Resource Center at
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PG175	
A1440 Function	**Location**
CLKA or I/O	C9
CLKB or I/O	A9
DCLK or I/O	D5
GND	D4, D8, D11, D12, E4, E14, H4, H12, L4, L12, M4, M8, M12
HCLK or I/O	R8
IOCLK or I/O	E12
IOPCL or I/O	P13
MODE	F3
NC	A1, A2, A15, B2, B3, P2, P14, R1, R2, R14, R15
PRA or I/O	B8
PRB or I/O	R7
SDI or I/O	D3
SDO	N12
VCC	C3, C8, C13, E15, H3, H13, L1, L14, N3, N8, N13

Notes:

1. All unlisted pin numbers are user I/Os.

2. NC denotes no connection.

3. MODE should be terminated to GND through a 10K resistor to enable Actionprobe usage; otherwise it can be terminated directly to GND.

4. The PG175 package has been discontinued.

Revision	Changes	Page
Revision 2 (continued)	In the "Package Pin Assignments" section, notes were added to the pin tables for the following packages, stating that they are discontinued:	
	"BG225"	3-20
	"PG100"	3-24
	"PG133"	3-26
	"PG175"	3-28
Revision 1 (June 2006)	RoHS compliant information was added to the "Ordering Information" section.	II

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