Welcome to E-XFL.COM

Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications,

Details	
Product Status	Obsolete
Number of LABs/CLBs	310
Number of Logic Elements/Cells	-
Total RAM Bits	-
Number of I/O	83
Number of Gates	2500
Voltage - Supply	4.5V ~ 5.5V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 70°C (TA)
Package / Case	100-TQFP
Supplier Device Package	100-VQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/microsemi/a1425a-1vqg100c

Device/Package	Speed Grade[1]				Application[1]			
	Std.	−1	−2	−3	C	I	M	B
A14V40A Device								
84-Pin Plastic Leaded Chip Carrier (PLCC)	✓	−	−	−	✓	−	−	−
100-Pin Very Thin Quad Flatpack (VQFP)	✓	−	−	−	✓	−	−	−
160-Pin Plastic Quad Flatpack (PQFP)	✓	−	−	−	✓	−	−	−
176-Pin Thin Quad Flatpack (TQFP)	✓	−	−	−	✓	−	−	−
A1460A Device								
160-Pin Plastic Quad Flatpack (PQFP)	✓	✓	D	D	✓	✓	−	−
176-Pin Thin Quad Flatpack (TQFP)	✓	✓	D	D	✓	✓	−	−
196-Pin Ceramic Quad Flatpack (CQFP)	✓	✓	−	−	✓	−	✓	✓
207-Pin Ceramic Pin Grid Array (CPGA)	✓	✓	D	D	✓	−	✓	✓
208-Pin Plastic Quad Flatpack (PQFP)	✓	✓	D	D	✓	✓	−	−
225-Pin Plastic Ball Grid Array (BGA)	D	D	D	D	D	−	−	−
A14V60A Device								
160-Pin Plastic Quad Flatpack (PQFP)	✓	−	−	−	✓	−	−	−
176-Pin Thin Quad Flatpack (TQFP)	✓	−	−	−	✓	−	−	−
208-Pin Plastic Quad Flatpack (PQFP)	✓	−	−	−	✓	−	−	−
A14100A Device								
208-Pin Power Quad Flatpack (RQFP)	✓	✓	D	D	✓	✓	−	−
257-Pin Ceramic Pin Grid Array (CPGA)	✓	✓	D	D	✓	−	✓	✓
313-Pin Plastic Ball Grid Array (BGA)	✓	✓	D	D	✓	−	−	−
256-Pin Ceramic Quad Flatpack (CQFP)	✓	✓	−	−	✓	−	✓	✓
A14V100A Device								
208-Pin Power Quad Flatpack (RQFP)	✓	−	−	−	✓	−	−	−
313-Pin Plastic Ball Grid Array (BGA)	✓	−	−	−	✓	−	−	−

Notes:

1. Applications:
 C = Commercial
 I = Industrial
 M = Military
2. Commercial only

Availability:
✓ = Available
P = Planned
− = Not planned
D = Discontinued

Speed Grade:
−1 = Approx. 15% faster than Std.
−2 = Approx. 25% faster than Std.
−3 = Approx. 35% faster than Std.
(−2 and −3 speed grades have been discontinued.)

Table 1-1 • **Chip-to-Chip Performance (worst-case commercial)**

Device and Speed Grade	t_{CKHS} (ns)	t_{TRACE} (ns)	t_{INSU} (ns)	Total (ns)	MHz
A1425A -3	7.5	1.0	1.8	10.3	97
A1460A -3	9.0	1.0	1.3	11.3	88
A1425A -2	7.5	1.0	2.0	10.5	95
A1460A -2	9.0	1.0	1.5	11.5	87
A1425A -1	9.0	1.0	2.3	12.3	81
A1460A -1	10.0	1.0	1.8	12.8	78
A1425A STD	10.0	1.0	2.7	13.7	73
A1460A STD	11.5	1.0	2.0	14.5	69

Note: The –2 and –3 speed grades have been discontinued. Refer to PDN 0104, PDN 0203, PDN 0604, and PDN 1004 at http://www.microsemi.com/soc/support/notifications/default.aspx#pdn.

The I/O module output Y is used to bring Pad signals into the array or to feed the output register back into the array. This allows the output register to be used in high-speed state machine applications. Side I/O modules have a dedicated output segment for Y extending into the routing channels above and below (similar to logic modules). Top/Bottom I/O modules have no dedicated output segment. Signals coming into the chip from the top or bottom are routed using F-fuses and LVTs (F-fuses and LVTs are explained in detail in the routing section).

I/O Pad Drivers

All pad drivers are capable of being tristate. Each buffer connects to an associated I/O module with four signals: OE (Output Enable), IE (Input Enable), DataOut, and DataIn. Certain special signals used only during programming and test also connect to the pad drivers: OUTEN (global output enable), INEN (global input enable), and SLEW (individual slew selection). See Figure 2-5.
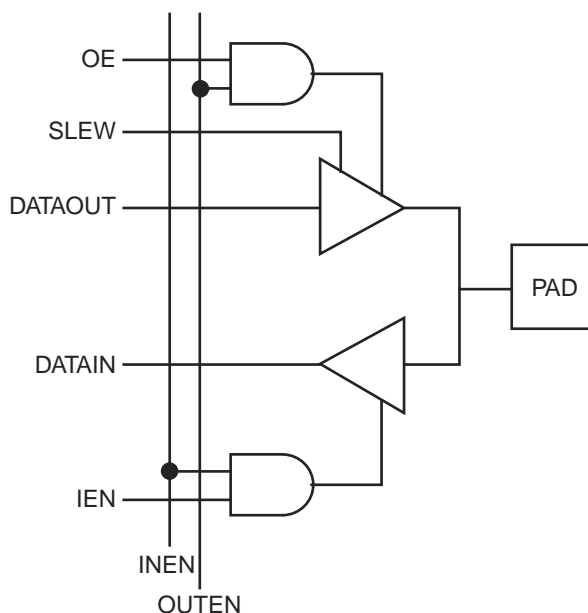

Figure 2-5 • **Function Diagram for I/O Pad Driver**

Special I/Os

The special I/Os are of two types: temporary and permanent. Temporary special I/Os are used during programming and testing. They function as normal I/Os when the MODE pin is inactive. Permanent special I/Os are user programmed as either normal I/Os or special I/Os. Their function does not change once the device has been programmed. The permanent special I/Os consist of the array clock input buffers (CLKA and CLKB), the hard-wired array clock input buffer (HCLK), the hard-wired I/O clock input buffer (IOCLK), and the hard-wired I/O register preset/clear input buffer (IOPCL). Their function is determined by the I/O macros selected.

Clock Networks

The ACT 3 architecture contains four clock networks: two high-performance dedicated clock networks and two general purpose routed networks. The high-performance networks function up to 200 MHz, while the general purpose routed networks function up to 150 MHz.

Horizontal Routing

Horizontal channels are located between the rows of modules and are composed of several routing tracks. The horizontal routing tracks within the channel are divided into one or more segments. The minimum horizontal segment length is the width of a module-pair, and the maximum horizontal segment length is the full length of the channel. Any segment that spans more than one-third the row length is considered a long horizontal segment. A typical channel is shown in Figure 2-7. Undedicated horizontal routing tracks are used to route signal nets. Dedicated routing tracks are used for the global clock networks and for power and ground tie-off tracks.
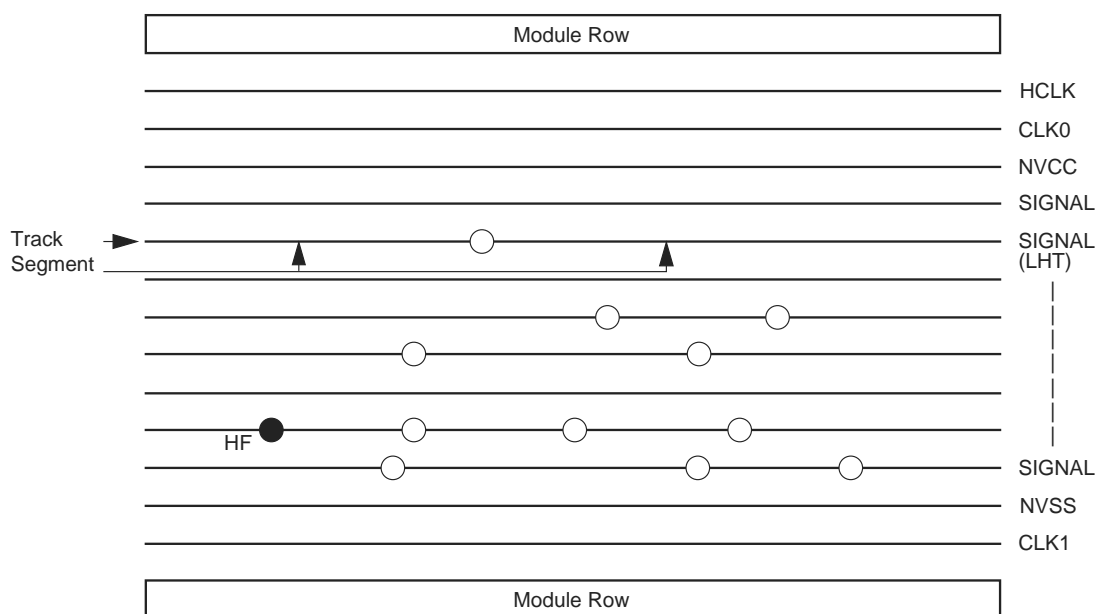

Figure 2-7 • **Horizontal Routing Tracks and Segments**

Vertical Routing

Other tracks run vertically through the modules. Vertical tracks are of three types: input, output, and long. Vertical tracks are also divided into one or more segments. Each segment in an input track is dedicated to the input of a particular module. Each segment in an output track is dedicated to the output of a particular module. Long segments are uncommitted and can be assigned during routing. Each output segment spans four channels (two above and two below), except near the top and bottom of the array where edge effects occur. LVTs contain either one or two segments. An example of vertical routing tracks and segments is shown in Figure 2-8.
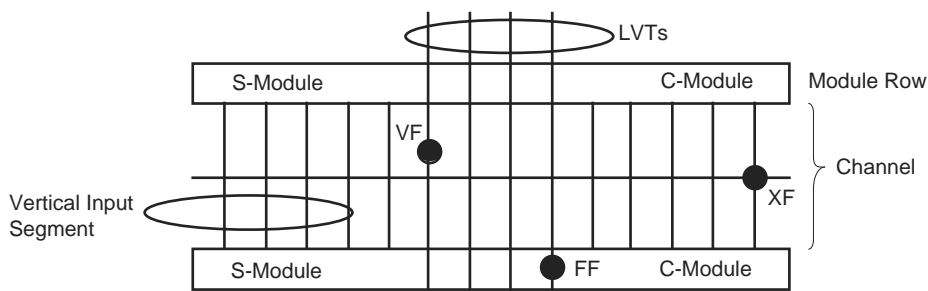

Figure 2-8 • **Vertical Routing Tracks and Segments**

Antifuse Connections

An antifuse is a "normally open" structure as opposed to the normally closed fuse structure used in PROMs or PALs. The use of antifuses to implement a programmable logic device results in highly testable structures as well as an efficient programming architecture. The structure is highly testable because there are no preexisting connections; temporary connections can be made using pass transistors. These temporary connections can isolate individual antifuses to be programmed as well as isolate individual circuit structures to be tested. This can be done both before and after programming. For example, all metal tracks can be tested for continuity and shorts between adjacent tracks, and the functionality of all logic modules can be verified.

Four types of antifuse connections are used in the routing structure of the ACT 3 array. (The physical structure of the antifuse is identical in each case; only the usage differs.)

Table 2-1 shows four types of antifuses.

Table 2-1 • **Antifuse Types**

Type	Description
XF	Horizontal-to-vertical connection
HF	Horizontal-to-horizontal connection
VF	Vertical-to-vertical connection
FF	"Fast" vertical connection

Examples of all four types of connections are shown in Figure 2-7 on page 2-6 and Figure 2-8 on page 2-6.

Module Interface

Connections to Logic and I/O modules are made through vertical segments that connect to the module inputs and outputs. These vertical segments lie on vertical tracks that span the entire height of the array.

Module Input Connections

The tracks dedicated to module inputs are segmented by pass transistors in each module row. During normal user operation, the pass transistors are inactive, which isolates the inputs of a module from the inputs of the module directly above or below it. During certain test modes, the pass transistors are active to verify the continuity of the metal tracks. Vertical input segments span only the channel above or the channel below. The logic modules are arranged such that half of the inputs are connected to the channel above and half of the inputs to segments in the channel below, as shown in Figure 2-9.
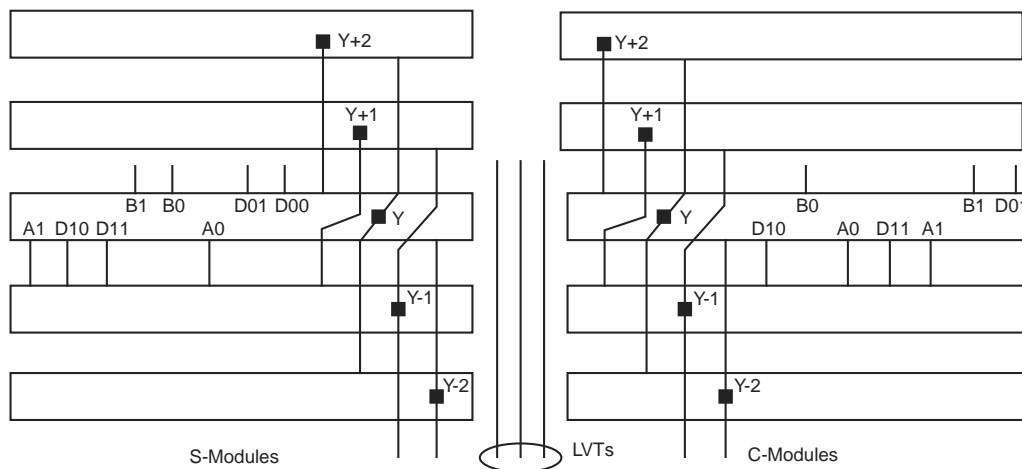

Figure 2-9 • **Logic Module Routing Interface**

Power Dissipation

$$P = [ICC \text{ standby} + Iactive] * VCC * IOL * VOL * N + IOH * (VCC - VOH) * M$$

EQ 3

where:

ICC standby is the current flowing when no inputs or outputs are changing

Iactive is the current flowing due to CMOS switching.

IOL and IOH are TTL sink/source current.

VOL and VOH are TTL level output voltages.

N is the number of outputs driving TTL loads to VOL.

M equals the number of outputs driving TTL loads to VOH.

An accurate determination of N and M is problematic because their values depend on the design and on the system I/O. The power can be divided into two components: static and active.

Static Power Component

Microsemi FPGAs have small static power components that result in lower power dissipation than PALs or PLDs. By integrating multiple PALs/PLDs into one FPGA, an even greater reduction in board-level power dissipation can be achieved.

The power due to standby current is typically a small component of the overall power. Standby power is calculated in Table 2-9 for commercial, worst case conditions.

Table 2-9 • **Standby Power Calculation**

ICC	VCC	Power
2 mA	5.25 V	10.5 mW

The static power dissipated by TTL loads depends on the number of outputs driving high or low and the DC load current. Again, this value is typically small. For instance, a 32-bit bus sinking 4 mA at 0.33 V will generate 42 mW with all outputs driving low, and 140 mW with all outputs driving high. The actual dissipation will average somewhere between as I/Os switch states with time.

Active Power Component

Power dissipation in CMOS devices is usually dominated by the active (dynamic) power dissipation. This component is frequency dependent, a function of the logic and the external I/O. Active power dissipation results from charging internal chip capacitances of the interconnect, unprogrammed antifuses, module inputs, and module outputs, plus external capacitance due to PC board traces and load device inputs.

An additional component of the active power dissipation is the totem-pole current in CMOS transistor pairs. The net effect can be associated with an equivalent capacitance that can be combined with frequency and voltage to represent active power dissipation.

Equivalent Capacitance

The power dissipated by a CMOS circuit can be expressed by EQ 4.

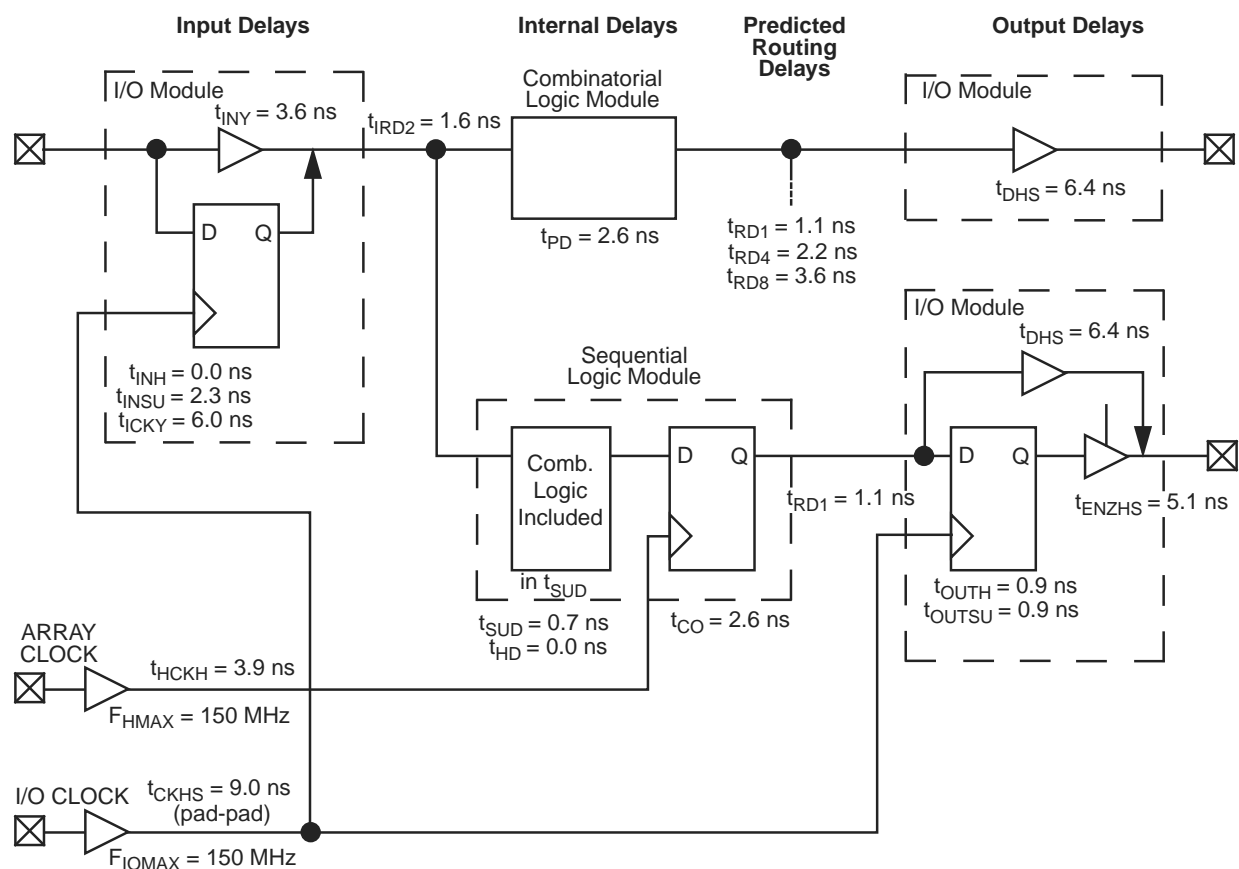$$\text{Power } (\mu W) = C_{EQ} * VCC^2 * F$$

EQ 4

Where:

C_{EQ} is the equivalent capacitance expressed in pF.

VCC is the power supply in volts.

F is the switching frequency in MHz.

ACT 3 Timing Model

Note: Values shown for A1425A –1 speed grade device.

Figure 2-10 • **Timing Model**

A1425A, A14V25A Timing Characteristics

Table 2-22 • A1425A, A14V25A Worst-Case Commercial Conditions, VCC = 4.75 V, T_J = 70°C[1]

Logic Module Propagation Delays[2]		–3 Speed[3]		–2 Speed[3]		–1 Speed		Std. Speed		3.3 V Speed[1]		Units
Parameter/Description		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t_{PD}	Internal Array Module		2.0		2.3		2.6		3.0		3.9	ns
t_{CO}	Sequential Clock to Q		2.0		2.3		2.6		3.0		3.9	ns
t_{CLR}	Asynchronous Clear to Q		2.0		2.3		2.6		3.0		3.9	ns
Predicted Routing Delays[4]												
t_{RD1}	FO = 1 Routing Delay		0.9		1.0		1.1		1.3		1.7	ns
t_{RD2}	FO = 2 Routing Delay		1.2		1.4		1.6		1.8		2.4	ns
t_{RD3}	FO = 3 Routing Delay		1.4		1.6		1.8		2.1		2.8	ns
t_{RD4}	FO = 4 Routing Delay		1.7		1.9		2.2		2.5		3.3	ns
t_{RD8}	FO = 8 Routing Delay		2.8		3.2		3.6		4.2		5.5	ns
Logic Module Sequential Timing												
t_{SUD}	Flip-Flop Data Input Setup	0.5		0.6		0.7		0.8		0.8		ns
t_{HD}	Flip-Flop Data Input Hold	0.0		0.0		0.0		0.0		0.0		ns
t_{SUD}	Latch Data Input Setup	0.5		0.6		0.7		0.8		0.8		ns
t_{HD}	Latch Data Input Hold	0.0		0.0		0.0		0.0		0.0		ns
t_{WASYN}	Asynchronous Pulse Width	1.9		2.4		3.2		3.8		4.8		ns
t_{WCLKA}	Flip-Flop Clock Pulse Width	1.9		2.4		3.2		3.8		4.8		ns
t_A	Flip-Flop Clock Input Period	4.0		5.0		6.8		8.0		10.0		ns
f_{MAX}	Flip-Flop Clock Frequency		250		200		150		125		100	MHz

Notes:

1. *VCC = 3.0 V for 3.3 V specifications.*
2. *For dual-module macros, use $t_{PD} + t_{RD1} + t_{PDn} + t_{CO} + t_{RD1} + t_{PDn}$ or $t_{PD1} + t_{RD1} + t_{SUD}$, whichever is appropriate.*
3. *The –2 and –3 speed grades have been discontinued. Refer to PDN 0104, PDN 0203, PDN 0604, and PDN 1004 at http://www.microsemi.com/soc/support/notifications/default.aspx#pdn.*
4. *Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual worst-case performance. Post-route timing is based on actual routing delay measurements performed on the device prior to shipment.*

A1425A, A14V25A Timing Characteristics (continued)

Table 2-25 • A1425A, A14V25A Worst-Case Commercial Conditions, VCC = 4.75 V, T_J = 70°C

Dedicated (hardwired) I/O Clock Network		–3 Speed[1]		–2 Speed[1]		–1 Speed		Std. Speed		3.3 V Speed[1]		Units
Parameter/Description		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t_{IOCKH}	Input Low to High (pad to I/O module input)		2.0		2.3		2.6		3.0		3.5	ns
t_{IOPWH}	Minimum Pulse Width High	1.9		2.4		3.3		3.8		4.8		ns
t_{IPOWL}	Minimum Pulse Width Low	1.9		2.4		3.3		3.8		4.8		ns
t_{IOSAPW}	Minimum Asynchronous Pulse Width	1.9		2.4		3.3		3.8		4.8		ns
t_{IOCKSW}	Maximum Skew		0.4		0.4		0.4		0.4		0.4	ns
t_{IOP}	Minimum Period	4.0		5.0		6.8		8.0		10.0		ns
f_{IOMAX}	Maximum Frequency		250		200		150		125		100	MHz
Dedicated (hardwired) Array Clock												
t_{HCKH}	Input Low to High (pad to S-module input)		3.0		3.4		3.9		4.5		5.5	ns
t_{HCKL}	Input High to Low (pad to S-module input)		3.0		3.4		3.9		4.5		5.5	ns
t_{HPWH}	Minimum Pulse Width High	1.9		2.4		3.3		3.8		4.8		ns
t_{HPWL}	Minimum Pulse Width Low	1.9		2.4		3.3		3.8		4.8		ns
t_{HCKSW}	Delta High to Low, Low Slew		0.3		0.3		0.3		0.3		0.3	ns
t_{HP}	Minimum Period	4.0		5.0		6.8		8.0		10.0		ns
f_{HMAX}	Maximum Frequency		250		200		150		125		100	MHz
Routed Array Clock Networks												
t_{RCKH}	Input Low to High (FO = 64)		3.7		4.1		4.7		5.5		9.0	ns
t_{RCKL}	Input High to Low (FO = 64)		4.0		4.5		5.1		6.0		9.0	ns
t_{RPWH}	Min. Pulse Width High (FO = 64)	3.3		3.8		4.2		4.9		6.5		ns
t_{RPWL}	Min. Pulse Width Low (FO = 64)	3.3		3.8		4.2		4.9		6.5		ns
t_{RCKSW}	Maximum Skew (FO = 128)		0.7		0.8		0.9		1.0		1.0	ns
t_{RP}	Minimum Period (FO = 64)	6.8		8.0		8.7		10.0		13.4		Units
f_{RMAX}	Maximum Frequency (FO = 64)		150		125		115		100		75	MHz
Clock-to-Clock Skews												
$t_{IOHCKSW}$	I/O Clock to H-Clock Skew	0.0	1.7	0.0	1.8	0.0	2.0	0.0	2.2	0.0	3.0	ns
$t_{IORCKSW}$	I/O Clock to R-Clock Skew (FO = 64) (FO = 80)	0.0 0.0	1.0 3.0	0.0 0.0	1.0 3.0	0.0 0.0	1.0 3.0	0.0 0.0	1.0 3.0	0.0 0.0	3.0 3.0	ns
t_{HRCKSW}	H-Clock to R-Clock Skew (FO = 64) (FO = 80)	0.0 0.0	1.0 3.0	0.0 0.0	1.0 3.0	0.0 0.0	1.0 3.0	0.0 0.0	1.0 3.0	0.0 0.0	1.0 3.0	ns

Notes:

1. *The –2 and –3 speed grades have been discontinued. Refer to PDN 0104, PDN 0203, PDN 0604, and PDN 1004 at http://www.microsemi.com/soc/support/notifications/default.aspx#pdn.*

2. *Delays based on 35 pF loading.*

A14100A, A14V100A Timing Characteristics

Table 2-34 • **A14100A, A14V100A Worst-Case Commercial Conditions, VCC = 4.75 V, T$_J$ = 70°C[1]**

Logic Module Propagation Delays[2]		−3 Speed[3]		−2 Speed[3]		−1 Speed		Std. Speed		3.3 V Speed[1]		Units
Parameter/Description		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t$_{PD}$	Internal Array Module		2.0		2.3		2.6		3.0		3.9	ns
t$_{CO}$	Sequential Clock to Q		2.0		2.3		2.6		3.0		3.9	ns
t$_{CLR}$	Asynchronous Clear to Q		2.0		2.3		2.6		3.0		3.9	ns
Predicted Routing Delays[4]												
t$_{RD1}$	FO = 1 Routing Delay		0.9		1.0		1.1		1.3		1.7	ns
t$_{RD2}$	FO = 2 Routing Delay		1.2		1.4		1.6		1.8		2.4	ns
t$_{RD3}$	FO = 3 Routing Delay		1.4		1.6		1.8		2.1		2.8	ns
t$_{RD4}$	FO = 4 Routing Delay		1.7		1.9		2.2		2.5		3.3	ns
t$_{RD8}$	FO = 8 Routing Delay		2.8		3.2		3.6		4.2		5.5	ns
Logic Module Sequential Timing												
t$_{SUD}$	Flip-Flop Data Input Setup	0.5		0.6		0.8		0.8		0.8		ns
t$_{HD}$	Flip-Flop Data Input Hold	0.0		0.0		0.5		0.5		0.5		ns
t$_{SUD}$	Latch Data Input Setup	0.5		0.6		0.8		0.8		0.8		ns
t$_{HD}$	Latch Data Input Hold	0.0		0.0		0.5		0.5		0.5		ns
t$_{WASYN}$	Asynchronous Pulse Width	2.4		3.2		3.8		4.8		6.5		ns
t$_{WCLKA}$	Flip-Flop Clock Pulse Width	2.4		3.2		3.8		4.8		6.5		ns
t$_A$	Flip-Flop Clock Input Period	5.0		6.8		8.0		10.0		13.4		ns
f$_{MAX}$	Flip-Flop Clock Frequency		200		150		125		100		75	MHz

Notes:

1. *VCC = 3.0 V for 3.3 V specifications.*

2. *For dual-module macros, use t$_{PD}$ + t$_{RD1}$ + t$_{PDn}$ + t$_{CO}$ + t$_{RD1}$ + t$_{PDn}$ or t$_{PD1}$ + t$_{RD1}$ + t$_{SUD}$, whichever is appropriate.*

3. *The −2 and −3 speed grades have been discontinued. Refer to PDN 0104, PDN 0203, PDN 0604, and PDN 1004 at http://www.microsemi.com/soc/support/notifications/default.aspx#pdn.*

4. *Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual worst-case performance. Post-route timing is based on actual routing delay measurements performed on the device prior to shipment.*

A14100A, A14V100A Timing Characteristics (continued)

Table 2-35 • **A14100A, A14V100A Worst-Case Commercial Conditions, VCC = 4.75 V, T$_J$ = 70°C**

I/O Module Input Propagation Delays		–3 Speed[1]		–2 Speed[1]		–1 Speed		Std. Speed		3.3 V Speed[1]		Units
Parameter/Description		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t$_{INY}$	Input Data Pad to Y		2.8		3.2		3.6		4.2		5.5	ns
t$_{ICKY}$	Input Reg IOCLK Pad to Y		4.7		5.3		6.0		7.0		9.2	ns
t$_{OCKY}$	Output Reg IOCLK Pad to Y		4.7		5.3		6.0		7.0		9.2	ns
t$_{ICLRY}$	Input Asynchronous Clear to Y		4.7		5.3		6.0		7.0		9.2	ns
t$_{OCLRY}$	Output Asynchronous Clear to Y		4.7		5.3		6.0		7.0		9.2	ns
Predicted Input Routing Delays[2]												
t$_{RD1}$	FO = 1 Routing Delay		0.9		1.0		1.1		1.3		1.7	ns
t$_{RD2}$	FO = 2 Routing Delay		1.2		1.4		1.6		1.8		2.4	ns
t$_{RD3}$	FO = 3 Routing Delay		1.4		1.6		1.8		2.1		2.8	ns
t$_{RD4}$	FO = 4 Routing Delay		1.7		1.9		2.2		2.5		3.3	ns
t$_{RD8}$	FO = 8 Routing Delay		2.8		3.2		3.6		4.2		5.5	ns
I/O Module Sequential Timing (wrt IOCLK pad)												
t$_{INH}$	Input F-F Data Hold	0.0		0.0		0.0		0.0		0.0		ns
t$_{INSU}$	Input F-F Data Setup	1.2		1.4		1.5		1.8		1.8		ns
t$_{IDEH}$	Input Data Enable Hold	0.0		0.0		0.0		0.0		0.0		ns
t$_{IDESU}$	Input Data Enable Setup	5.8		6.5		7.5		8.6		8.6		ns
t$_{OUTH}$	Output F-F Data hold	0.7		0.8		1.0		1.0		1.0		ns
t$_{OUTSU}$	Output F-F Data Setup	0.7		0.8		1.0		1.0		1.0		ns
t$_{ODEH}$	Output Data Enable Hold	0.3		0.4		0.5		0.5		0.5		ns
f$_{ODESU}$	Output Data Enable Setup	1.3		1.5		2.0		2.0		2.0		ns

Notes: *

1. *The –2 and –3 speed grades have been discontinued. Refer to PDN 0104, PDN 0203, PDN 0604, and PDN 1004 at http://www.microsemi.com/soc/support/notifications/default.aspx#pdn.*

2. *Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual worst-case performance. Post-route timing is based on actual routing delay measurements performed on the device prior to shipment.*

A14100A, A14V100A Timing Characteristics (continued)

Table 2-37 • **A14100A, A14V100A Worst-Case Commercial Conditions, VCC = 4.75 V, T$_J$ = 70°C**

Dedicated (hardwired) I/O Clock Network		–3 Speed[1]		–2 Speed[1]		–1 Speed		Std. Speed		3.3 V Speed[1]		Units
Parameter/Description		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t$_{IOCKH}$	Input Low to High (pad to I/O module input)		2.3		2.6		3.0		3.5		4.5	ns
t$_{IOPWH}$	Minimum Pulse Width High	2.4		3.3		3.8		4.8		6.5		ns
t$_{IPOWL}$	Minimum Pulse Width Low	2.4		3.3		3.8		4.8		6.5		ns
t$_{IOSAPW}$	Minimum Asynchronous Pulse Width	2.4		3.3		3.8		4.8		6.5		ns
t$_{IOCKSW}$	Maximum Skew		0.6		0.6		0.7		0.8		0.6	ns
t$_{IOP}$	Minimum Period	5.0		6.8		8.0		10.0		13.4		ns
f$_{IOMAX}$	Maximum Frequency		200		150		125		100		75	MHz
Dedicated (hardwired) Array Clock												
t$_{HCKH}$	Input Low to High (pad to S-module input)		3.7		4.1		4.7		5.5		7.0	ns
t$_{HCKL}$	Input High to Low (pad to S-module input)		3.7		4.1		4.7		5.5		7.0	ns
t$_{HPWH}$	Minimum Pulse Width High	2.4		3.3		3.8		4.8		6.5		ns
t$_{HPWL}$	Minimum Pulse Width Low	2.4		3.3		3.8		4.8		6.5		ns
t$_{HCKSW}$	Delta High to Low, Low Slew		0.6		0.6		0.7		0.8		0.6	ns
t$_{HP}$	Minimum Period	5.0		6.8		8.0		10.0		13.4		ns
f$_{HMAX}$	Maximum Frequency		200		150		125		100		75	MHz
Routed Array Clock Networks												
t$_{RCKH}$	Input Low to High (FO = 64)		6.0		6.8		7.7		9.0		11.8	ns
t$_{RCKL}$	Input High to Low (FO = 64)		6.0		6.8		7.7		9.0		11.8	ns
t$_{RPWH}$	Min. Pulse Width High (FO = 64)	4.1		4.5		5.4		6.1		8.2		ns
t$_{RPWL}$	Min. Pulse Width Low (FO = 64)	4.1		4.5		5.4		6.1		8.2		ns
t$_{RCKSW}$	Maximum Skew (FO = 128)		1.2		1.4		1.6		1.8		1.8	ns
t$_{RP}$	Minimum Period (FO = 64)	8.3		9.3		11.1		12.5		16.7		Units
f$_{RMAX}$	Maximum Frequency (FO = 64)		120		105		90		80		60	MHz
Clock-to-Clock Skews												
t$_{IOHCKSW}$	I/O Clock to H-Clock Skew	0.0	2.6	0.0	2.7	0.0	2.9	0.0	3.0	0.0	3.0	ns
t$_{IORCKSW}$	I/O Clock to R-Clock Skew (FO = 64) (FO = 350)	0.0 0.0	1.7 5.0	0.0 0.0	1.7 5.0	0.0 0.0	1.7 5.0	0.0 0.0	1.7 5.0	0.0 0.0	5.0 5.0	ns
t$_{HRCKSW}$	H-Clock to R-Clock Skew (FO = 64) (FO = 350)	0.0 0.0	1.3 3.0	0.0 0.0	1.0 3.0	0.0 0.0	1.0 3.0	0.0 0.0	1.0 3.0	0.0 0.0	1.0 3.0	ns

Notes: *

1. *The –2 and –3 speed grades have been discontinued. Refer to PDN 0104, PDN 0203, PDN 0604, and PDN 1004 at http://www.microsemi.com/soc/support/notifications/default.aspx#pdn.*

2. *Delays based on 35 pF loading.*

PL84			
Pin Number	A1415, A14V15 Function	A1425, A14V25 Function	A1440, A14V40 Function
1	VCC	VCC	VCC
2	GND	GND	GND
3	VCC	VCC	VCC
4	PRA, I/O	PRA, I/O	PRA, I/O
11	DCLK, I/O	DCLK, I/O	DCLK, I/O
12	SDI, I/O	SDI, I/O	SDI, I/O
16	MODE	MODE	MODE
27	GND	GND	GND
28	VCC	VCC	VCC
40	PRB, I/O	PRB, I/O	PRB, I/O
41	VCC	VCC	VCC
42	GND	GND	GND
43	VCC	VCC	VCC
45	HCLK, I/O	HCLK, I/O	HCLK, I/O
52	SDO	SDO	SDO
53	IOPCL, I/O	IOPCL, I/O	IOPCL, I/O
59	VCC	VCC	VCC
60	VCC	VCC	VCC
61	GND	GND	GND
68	VCC	VCC	VCC
69	GND	GND	GND
74	IOCLK, I/O	IOCLK, I/O	IOCLK, I/O
83	CLKA, I/O	CLKA, I/O	CLKA, I/O
84	CLKB, I/O	CLKB, I/O	CLKB, I/O

Notes:

1. All unlisted pin numbers are user I/Os.
2. NC denotes no connection.
3. MODE should be terminated to GND through a 10K resistor to enable Actionprobe usage; otherwise it can be terminated directly to GND.

PQ100
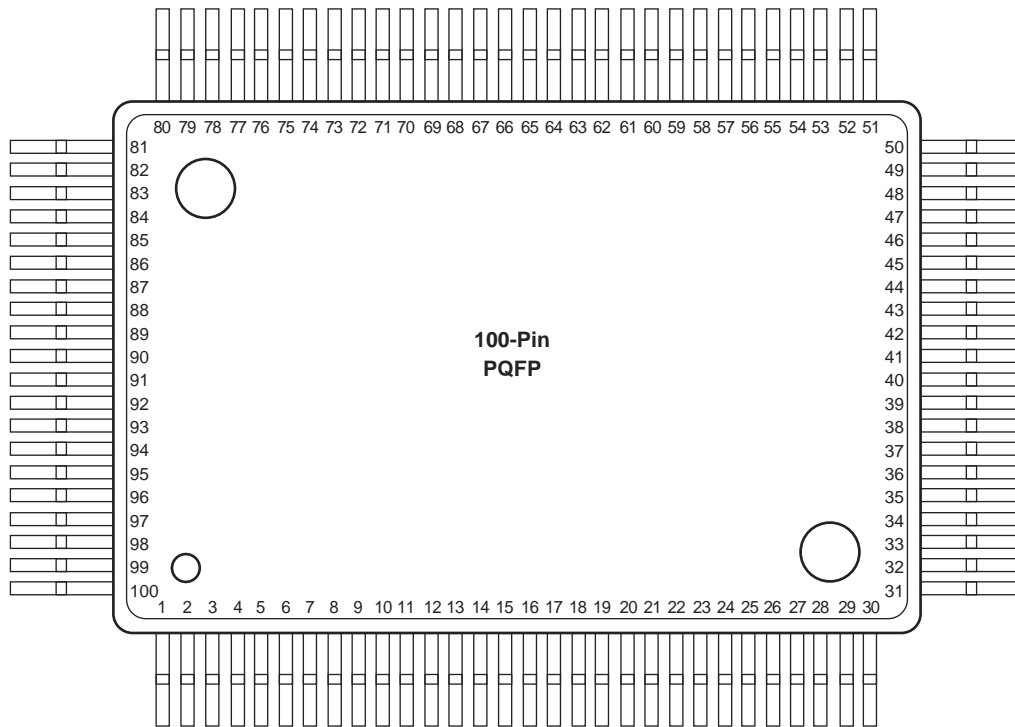
Note: This is the top view of the package.

Note

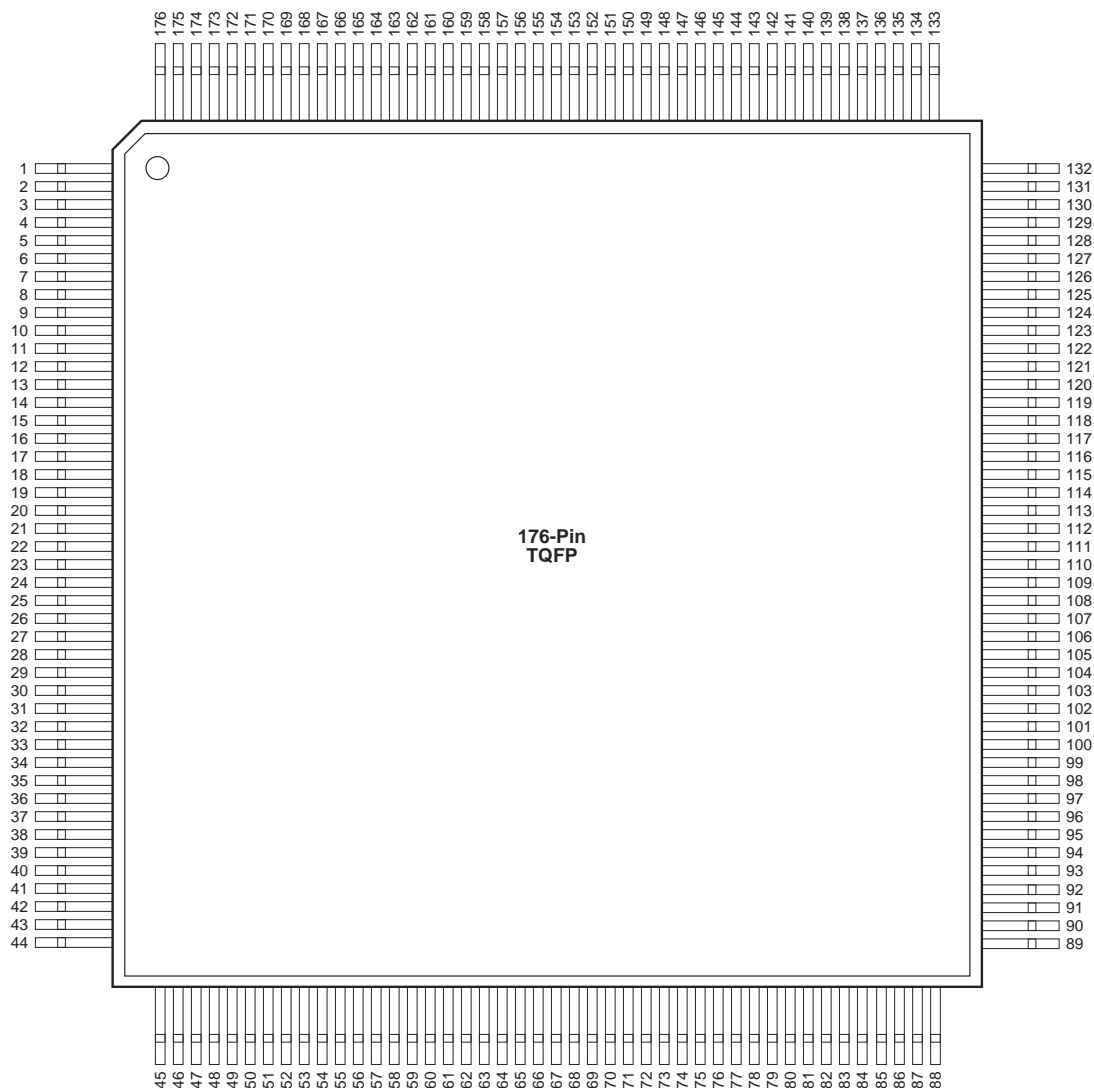For Package Manufacturing and Environmental information, visit the Resource Center at
http://www.microsemi.com/soc/products/solutions/package/docs.aspx

PQ100		
Pin Number	A1415 Function	A1425 Function
2	IOCLK, I/O	IOCLK, I/O
14	CLKA, I/O	CLKA, I/O
15	CLKB, I/O	CLKB, I/O
16	VCC	VCC
17	GND	GND
18	VCC	VCC
19	GND	GND
20	PRA, I/O	PRA, I/O
27	DCLK, I/O	DCLK, I/O
28	GND	GND
29	SDI, I/O	SDI, I/O
34	MODE	MODE
35	VCC	VCC
36	GND	GND
47	GND	GND
48	VCC	VCC
61	PRB, I/O	PRB, I/O
62	GND	GND
63	VCC	VCC
64	GND	GND
65	VCC	VCC
67	HCLK, I/O	HCLK, I/O
77	SDO	SDO
78	IOPCL, I/O	IOPCL, I/O
79	GND	GND
85	VCC	VCC
86	VCC	VCC
87	GND	GND
96	VCC	VCC
97	GND	GND

Notes:

1. All unlisted pin numbers are user I/Os.
2. NC denotes no connection.
3. MODE should be terminated to GND through a 10K resistor to enable Actionprobe usage; otherwise it can be terminated directly to GND.

| PQ160			
Pin Number	**A1425, A14V25 Function**	**A1440, A14V40 Function**	**A1460, A14V60 Function**
1	GND	GND	GND
2	SDI, I/O	SDI, I/O	SDI, I/O
5	NC	I/O	I/O
9	MODE	MODE	MODE
10	VCC	VCC	VCC
14	NC	I/O	I/O
15	GND	GND	GND
18	VCC	VCC	VCC
19	GND	GND	GND
20	NC	I/O	I/O
24	NC	I/O	I/O
27	NC	I/O	I/O
28	VCC	VCC	VCC
29	VCC	VCC	VCC
40	GND	GND	GND
41	NC	I/O	I/O
43	NC	I/O	I/O
45	NC	I/O	I/O
46	VCC	VCC	VCC
47	NC	I/O	I/O
49	NC	I/O	I/O
51	NC	I/O	I/O
53	NC	I/O	I/O
58	PRB, I/O	PRB, I/O	PRB, I/O
59	GND	GND	GND
60	VCC	VCC	VCC
62	HCLK, I/O	HCLK, I/O	HCLK, I/O
63	GND	GND	GND
74	NC	I/O	I/O
75	VCC	VCC	VCC
76	NC	I/O	I/O
77	NC	I/O	I/O
78	NC	I/O	I/O
79	SDO	SDO	SDO
80	IOPCL, I/O	IOPCL, I/O	IOPCL, I/O
81	GND	GND	GND
90	VCC	VCC	VCC
91	VCC	VCC	VCC

TQ176

Note: This is the top view.

Note

For Package Manufacturing and Environmental information, visit the Resource Center at
http://www.microsemi.com/soc/products/solutions/package/docs.aspx

CQ132

Note: This is the top view

Note

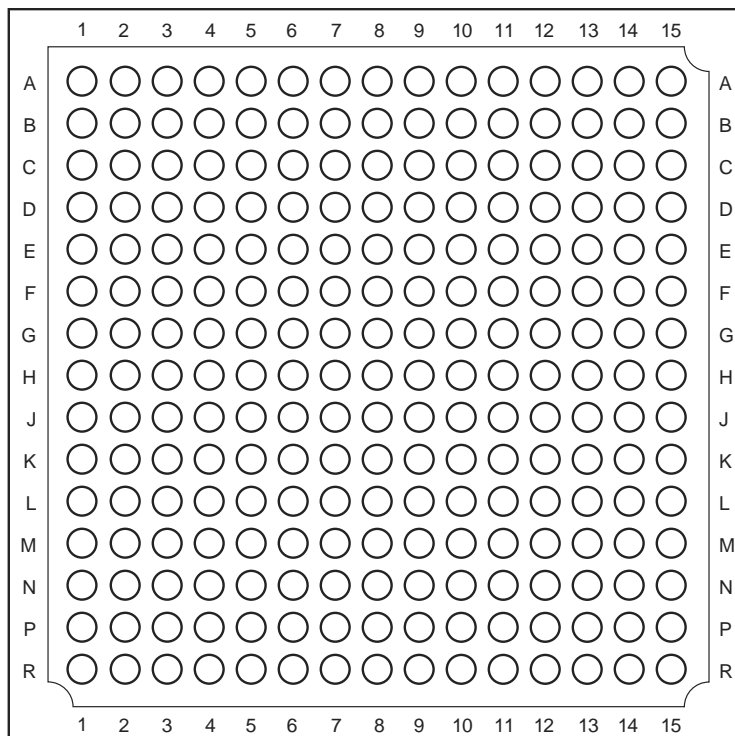For Package Manufacturing and Environmental information, visit the Resource Center at
http://www.microsemi.com/soc/products/solutions/package/docs.aspx
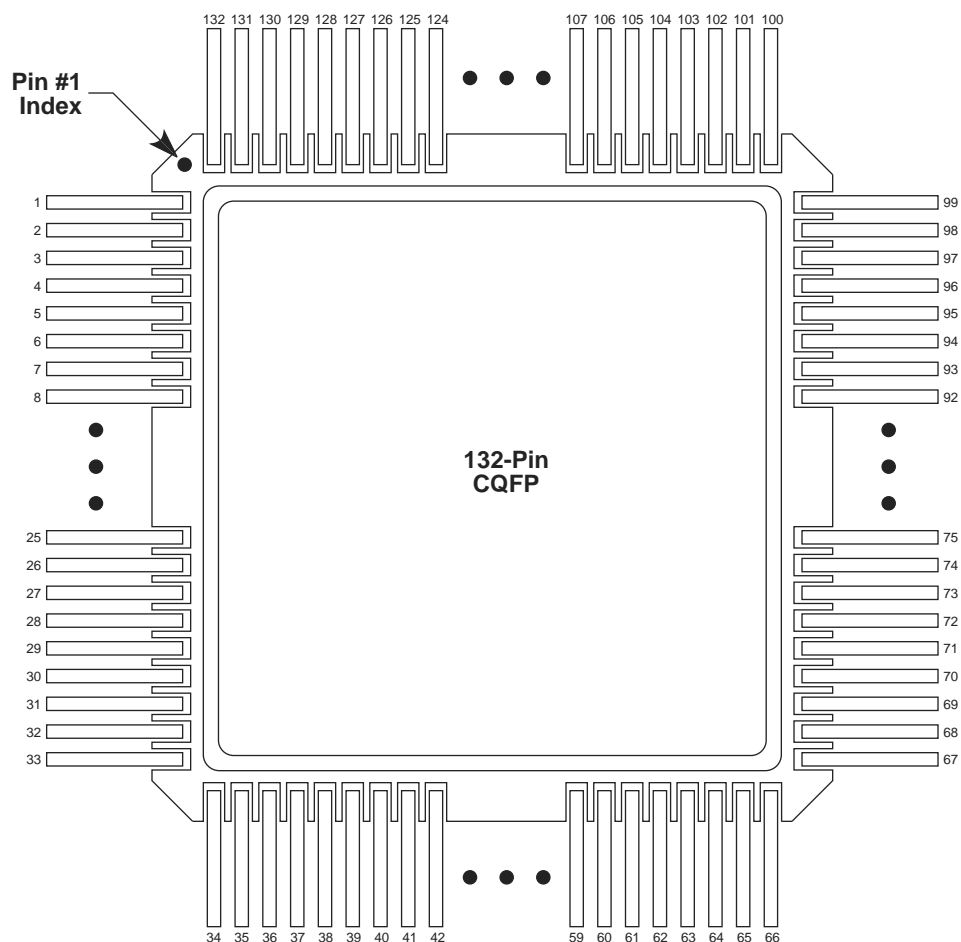
CQ132		CQ132	
Pin Number	**A1425 Function**	**Pin Number**	**A1425 Function**
1	NC	67	NC
2	GND	74	GND
3	SDI, I/O	75	VCC
9	MODE	78	VCC
10	GND	89	VCC
11	VCC	90	GND
22	VCC	91	VCC
26	GND	92	GND
27	VCC	98	IOCLK, I/O
34	NC	99	NC
36	GND	100	NC
42	GND	101	GND
43	VCC	106	GND
48	PRB, I/O	107	VCC
50	HCLK, I/O	116	CLKA, I/O
58	GND	117	CLKB, I/O
59	VCC	118	PRA, I/O
63	SDO	122	GND
64	IOPCL, I/O	123	VCC
65	GND	131	DCLK, I/O
66	NC	132	NC

Notes:

1. All unlisted pin numbers are user I/Os.

2. NC denotes no connection.

3. MODE should be terminated to GND through a 10K resistor to enable Actionprobe usage; otherwise it can be terminated directly to GND.

![Microsemi logo]

BG225

Note: This is the top view.

Note

For Package Manufacturing and Environmental information, visit the Resource Center at
http://www.microsemi.com/soc/products/solutions/package/docs.aspx