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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	310
Number of Logic Elements/Cells	-
Total RAM Bits	-
Number of I/O	70
Number of Gates	2500
Voltage - Supply	4.5V ~ 5.5V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 70°C (TA)
Package / Case	84-LCC (J-Lead)
Supplier Device Package	84-PLCC (29.31x29.31)
Purchase URL	https://www.e-xfl.com/product-detail/microsemi/a1425a-plg84c

Product Plan

Device/Package	Speed Grade[1]				Application[1]			
	Std.	–1	–2	–3	C	I	M	B
A1415A Device								
84-Pin Plastic Leaded Chip Carrier (PLCC)	✓	✓	D	D	✓	✓	✓	–
100-Pin Plastic Quad Flatpack (PQFP)	✓	✓	D	D	✓	✓	✓	–
100-Pin Very Thin Quad Flatpack (VQFP)	✓	✓	D	D	✓	✓	✓	–
100-Pin Ceramic Pin Grid Array (CPGA)	D	D	D	D	D	–	–	–
A14V15A Device								
84-Pin Plastic Leaded Chip Carrier (PLCC)	✓	–	–	–	✓	–	–	–
100-Pin Very Thin Quad Flatpack (VQFP)	✓	–	–	–	✓	–	–	–
A1425A Device								
84-Pin Plastic Leaded Chip Carrier (PLCC)	✓	✓	D	D	✓	✓		
100-Pin Plastic Quad Flatpack (PQFP)	✓	✓	D	D	✓	✓	–	–
100-Pin Very Thin Quad Flatpack (VQFP)	✓	✓	D	D	✓	✓	–	–
132-Pin Ceramic Quad Flatpack (CQFP)	✓	✓	–	–	✓	–	✓	✓
133-Pin Ceramic Pin Grid Array (CPGA)	D	D	D	D	D	–	D	D
160-Pin Plastic Quad Flatpack (PQFP)	✓	✓	D	D	✓	✓	–	–
A14V25A Device								
84-Pin Plastic Leaded Chip Carrier (PLCC)	✓	–	–	–	✓	–	–	–
100-Pin Very Thin Quad Flatpack (VQFP)	✓	–	–	–	✓	–	–	–
160-Pin Plastic Quad Flatpack (PQFP)	✓	–	–	–	✓	–	–	–
A1440A Device								
84-Pin Plastic Leaded Chip Carrier (PLCC)	✓	✓	D	D	✓	✓	–	–
100-Pin Very Thin Quad Flatpack (VQFP)	✓	✓	D	D	✓	✓	–	–
160-Pin Plastic Quad Flatpack (PQFP)	✓	✓	D	D	✓	✓	–	–
175-Pin Ceramic Pin Grid Array (CPGA)	D	D	D	D	D	–	–	–
176-Pin Thin Quad Flatpack (TQFP)	✓	✓	D	D	✓	✓	–	–

Notes:

1. *Applications:*
   C = Commercial
   I = Industrial
   M = Military
2. *Commercial only*

Availability:
✓ = Available
P = Planned
– = Not planned
D = Discontinued

Speed Grade:
–1 = Approx. 15% faster than Std.
–2 = Approx. 25% faster than Std.
–3 = Approx. 35% faster than Std.
(–2 and –3 speed grades have been discontinued.)

Horizontal Routing

Horizontal channels are located between the rows of modules and are composed of several routing tracks. The horizontal routing tracks within the channel are divided into one or more segments. The minimum horizontal segment length is the width of a module-pair, and the maximum horizontal segment length is the full length of the channel. Any segment that spans more than one-third the row length is considered a long horizontal segment. A typical channel is shown in Figure 2-7. Undedicated horizontal routing tracks are used to route signal nets. Dedicated routing tracks are used for the global clock networks and for power and ground tie-off tracks.

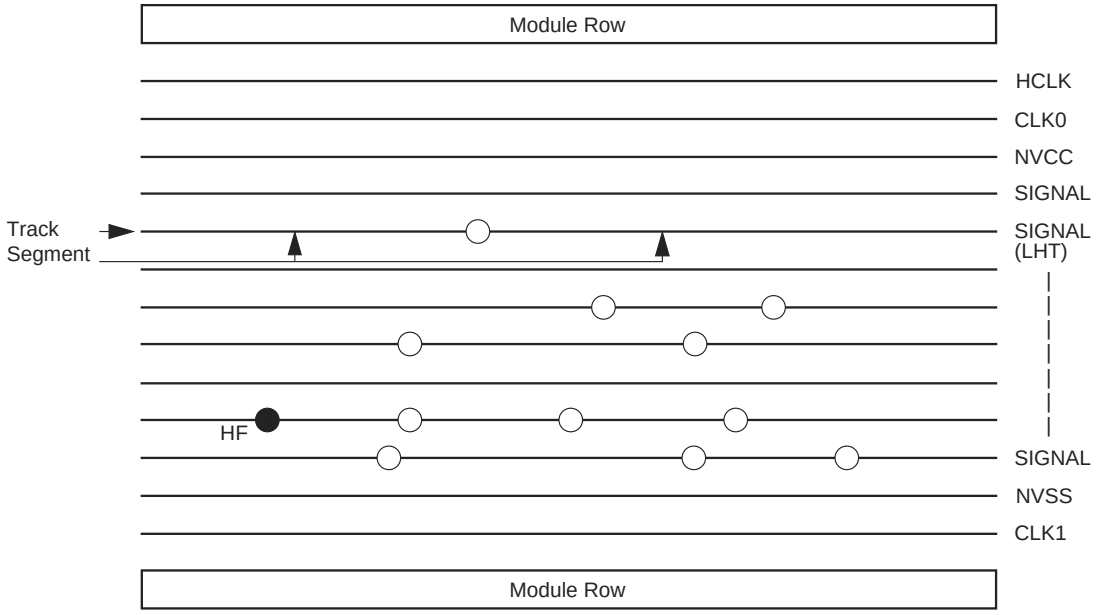


Figure 2-7 • **Horizontal Routing Tracks and Segments**

Vertical Routing

Other tracks run vertically through the modules. Vertical tracks are of three types: input, output, and long. Vertical tracks are also divided into one or more segments. Each segment in an input track is dedicated to the input of a particular module. Each segment in an output track is dedicated to the output of a particular module. Long segments are uncommitted and can be assigned during routing. Each output segment spans four channels (two above and two below), except near the top and bottom of the array where edge effects occur. LVTs contain either one or two segments. An example of vertical routing tracks and segments is shown in Figure 2-8.

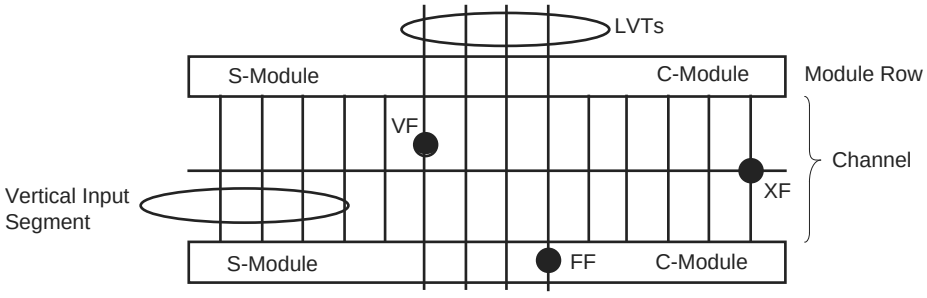


Figure 2-8 • **Vertical Routing Tracks and Segments**

Antifuse Connections

An antifuse is a “normally open” structure as opposed to the normally closed fuse structure used in PROMs or PALs. The use of antifuses to implement a programmable logic device results in highly testable structures as well as an efficient programming architecture. The structure is highly testable because there are no preexisting connections; temporary connections can be made using pass transistors. These temporary connections can isolate individual antifuses to be programmed as well as isolate individual circuit structures to be tested. This can be done both before and after programming. For example, all metal tracks can be tested for continuity and shorts between adjacent tracks, and the functionality of all logic modules can be verified.

Four types of antifuse connections are used in the routing structure of the ACT 3 array. (The physical structure of the antifuse is identical in each case; only the usage differs.)

Table 2-1 shows four types of antifuses.

Table 2-1 • **Antifuse Types**

Type	Description
XF	Horizontal-to-vertical connection
HF	Horizontal-to-horizontal connection
VF	Vertical-to-vertical connection
FF	"Fast" vertical connection

Examples of all four types of connections are shown in Figure 2-7 on page 2-6 and Figure 2-8 on page 2-6.

Module Interface

Connections to Logic and I/O modules are made through vertical segments that connect to the module inputs and outputs. These vertical segments lie on vertical tracks that span the entire height of the array.

Module Input Connections

The tracks dedicated to module inputs are segmented by pass transistors in each module row. During normal user operation, the pass transistors are inactive, which isolates the inputs of a module from the inputs of the module directly above or below it. During certain test modes, the pass transistors are active to verify the continuity of the metal tracks. Vertical input segments span only the channel above or the channel below. The logic modules are arranged such that half of the inputs are connected to the channel above and half of the inputs to segments in the channel below, as shown in Figure 2-9.

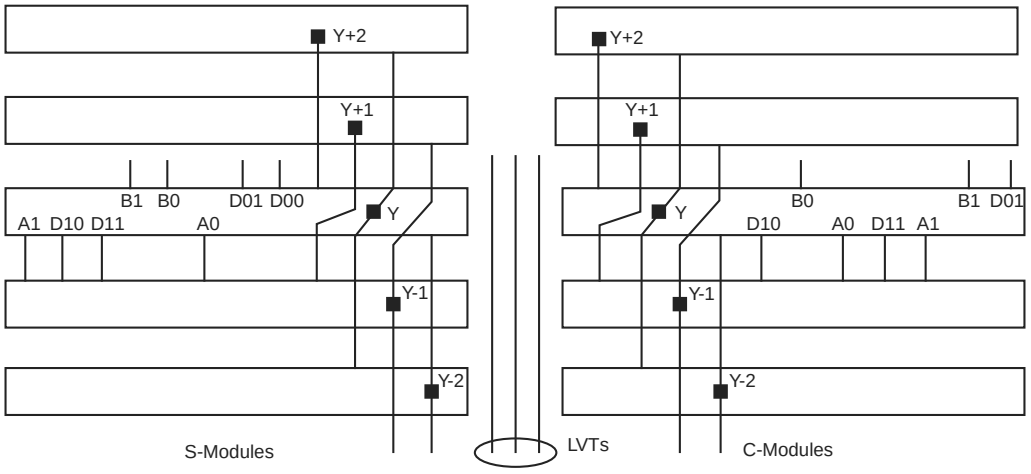


Figure 2-9 • **Logic Module Routing Interface**

Module Output Connections

Module outputs have dedicated output segments. Output segments extend vertically two channels above and two channels below, except at the top or bottom of the array. Output segments twist, as shown in Figure 10, so that only four vertical tracks are required.

LVT Connections

Outputs may also connect to nondedicated segments called Long Vertical Tracks (LVTs). Each module pair in the array shares four LVTs that span the length of the column. Any module in the column pair can connect to one of the LVTs in the column using an FF connection. The FF connection uses antifuses connected directly to the driver stage of the module output, bypassing the isolation transistor. FF antifuses are programmed at a higher current level than HF, VF, or XF antifuses to produce a lower resistance value.

Antifuse Connections

In general every intersection of a vertical segment and a horizontal segment contains an unprogrammed antifuse (XF-type). One exception is in the case of the clock networks.

Clock Connections

To minimize loading on the clock networks, a subset of inputs has antifuses on the clock tracks. Only a few of the C-module and S-module inputs can be connected to the clock networks. To further reduce loading on the clock network, only a subset of the horizontal routing tracks can connect to the clock inputs of the S-module.

Programming and Test Circuits

The array of logic and I/O modules is surrounded by test and programming circuits controlled by the temporary special I/O pins MODE, SDI, and DCLK. The function of these pins is similar to all ACT family devices. The ACT 3 family also includes support for two Actionprobe® circuits, allowing complete observability of any logic or I/O module in the array using the temporary special I/O pins, PRA and PRB.

Equivalent capacitance is calculated by measuring ICC active at a specified frequency and voltage for each circuit component of interest. Measurements have been made over a range of frequencies at a fixed value of VCC. Equivalent capacitance is frequency independent so that the results may be used over a wide range of operating conditions. Equivalent capacitance values are shown in Figure 2-10.

***Table 2-10* • CEQ Values for Microsemi FPGAs**

Item	CEQ Value
Modules (C_{EQM})	6.7
Input Buffers (C_{EQI})	7.2
Output Buffers (C_{EQO})	10.4
Routed Array Clock Buffer Loads (C_{EQCR})	1.6
Dedicated Clock Buffer Loads (C_{EQCD})	0.7
I/O Clock Buffer Loads ($C_{EQCI)}$	0.9

To calculate the active power dissipated from the complete design, the switching frequency of each part of the logic must be known. EQ 5 shows a piece-wise linear summation over all components.

$$\text{Power} = VCC^2 * [(m * C_{EQM} * f_m)_{modules} + (n * C_{EQI} * f_n)_{inputs} + (p * (C_{EQO} + C_L) * fp)_{outputs} + 0.5 * (q1 * C_{EQCR} * f_{q1})_{routed\_Clk1} + (r1 * fq1)_{routed\_Clk1} + 0.5 * (q2 * C_{EQCR} * fq2)_{routed\_Clk2} + (r_2 * f_{q2})_{routed\_Clk2} + 0.5 * (s_1 * C_{EQCD} * f_{s1})_{dedicated\_Clk} + (s_2 * C_{EQCI} * f_{s2})_{IO\_Clk}]$$

EQ 5

Where:

m = Number of logic modules switching at f_m
n = Number of input buffers switching at f_n
p = Number of output buffers switching at f_p
q1 = Number of clock loads on the first routed array clock
q2 = Number of clock loads on the second routed array clock
r_1 = Fixed capacitance due to first routed array clock
r_2 = Fixed capacitance due to second routed array clock
s_1 = Fixed number of clock loads on the dedicated array clock
s_2 = Fixed number of clock loads on the dedicated I/O clock
C_{EQM} = Equivalent capacitance of logic modules in pF
C_{EQI} = Equivalent capacitance of input buffers in pF
C_{EQO} = Equivalent capacitance of output buffers in pF
C_{EQCR} = Equivalent capacitance of routed array clock in pF
C_{EQCD} = Equivalent capacitance of dedicated array clock in pF
C_{EQCI} = Equivalent capacitance of dedicated I/O clock in pF
C_L = Output lead capacitance in pF
f_m = Average logic module switching rate in MHz
f_n = Average input buffer switching rate in MHz
f_p = Average output buffer switching rate in MHz
f_{q1} = Average first routed array clock rate in MHz
f_{q2} = Average second routed array clock rate in MHz
f_{s1} = Average dedicated array clock rate in MHz
f_{s2} = Average dedicated I/O clock rate in MHz

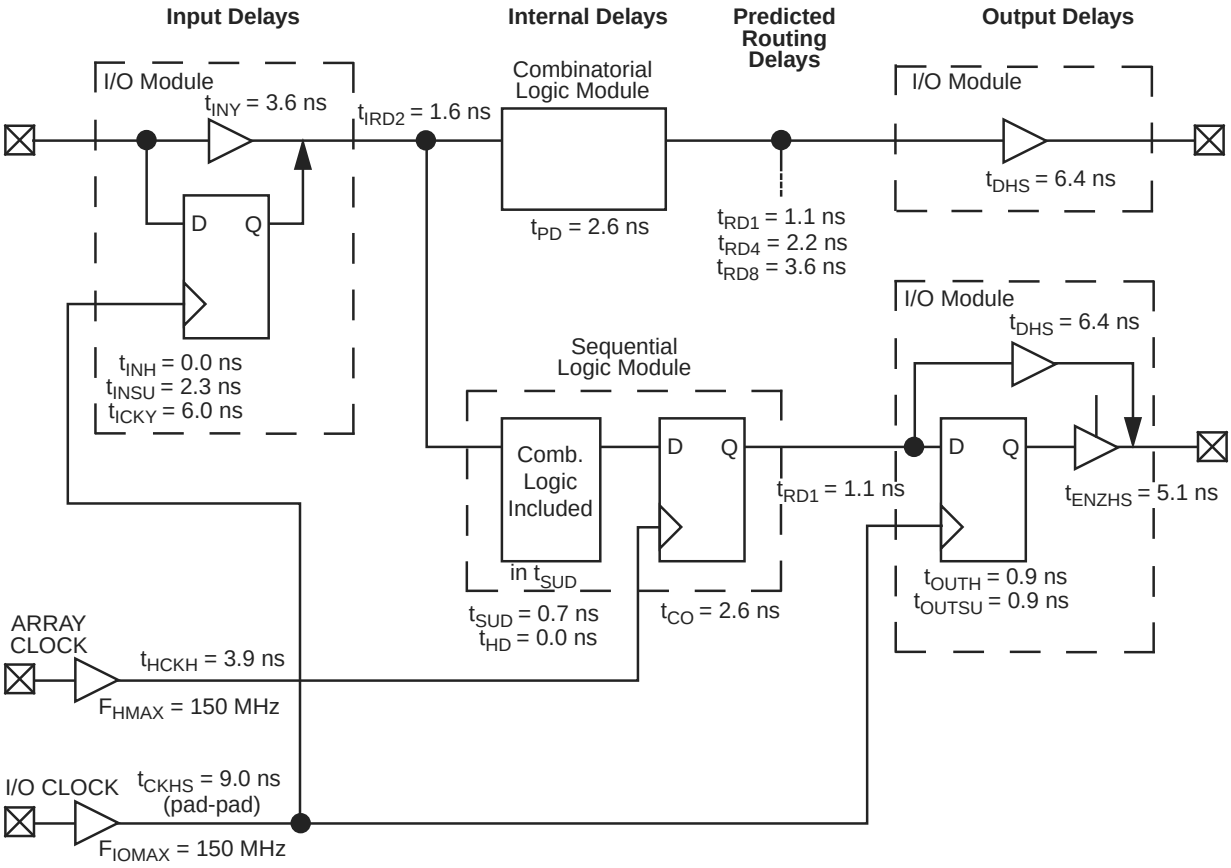
***Table 2-11* • Fixed Capacitance Values for Microsemi FPGAs**

Device Type	r1, routed_Clk1	r2, routed_Clk2
A1415A	60	60
A14V15A	57	57
A1425A	75	75
A14V25A	72	72
A1440A	105	105
A14V40A	100	100
A1440B	105	105
A1460A	165	165
A14V60A	157	157
A1460B	165	165
A14100A	195	195
A14V100A	185	185
A14100B	195	195

***Table 2-12* • Fixed Clock Loads (s1/s2)**

Device Type	s1, Clock Loads on Dedicated Array Clock	s2, Clock Loads on Dedicated I/O Clock
A1415A	104	80
A14V15A	104	80
A1425A	160	100
A14V25A	160	100
A1440A	288	140
A14V40A	288	140
A1440B	288	140
A1460A	432	168
A14V60A	432	168
A1460B	432	168
A14100A	697	228
A14V100A	697	228
A14100B	697	228

ACT 3 Timing Model



Note: Values shown for A1425A –1 speed grade device.

Figure 2-10 • **Timing Model**

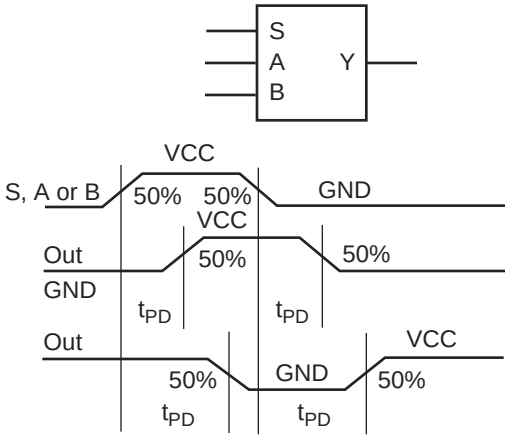


Figure 2-14 • **Module Delays**

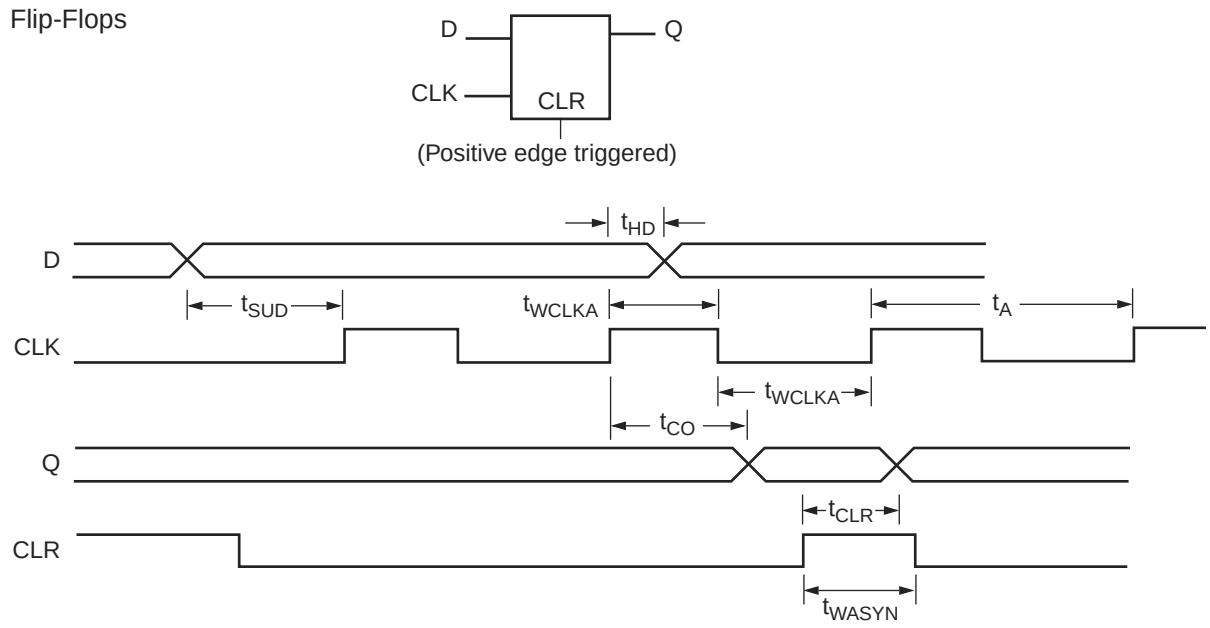


Figure 2-15 • **Sequential Module Timing Characteristics**

SDO **Serial Data Output (Output)**

Serial data output for diagnostic probe. SDO is active when the MODE pin is High. This pin functions as an I/O when the MODE pin is Low.

DCLK **Diagnostic Clock (Input)**

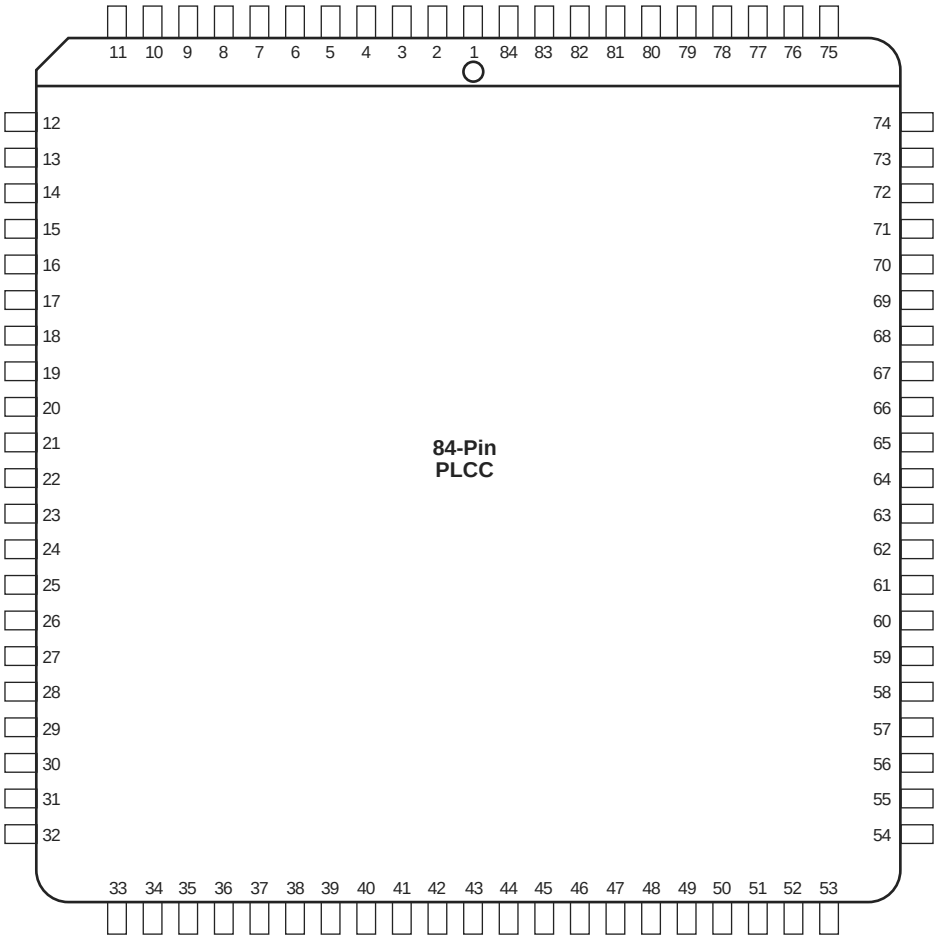
Clock input for diagnostic probe and device programming. DCLK is active when the MODE pin is HIGH. This pin functions as an I/O when the MODE pin is LOW.

VCC **5 V Supply Voltage**

HIGH supply voltage.

3 – Package Pin Assignments

PL84

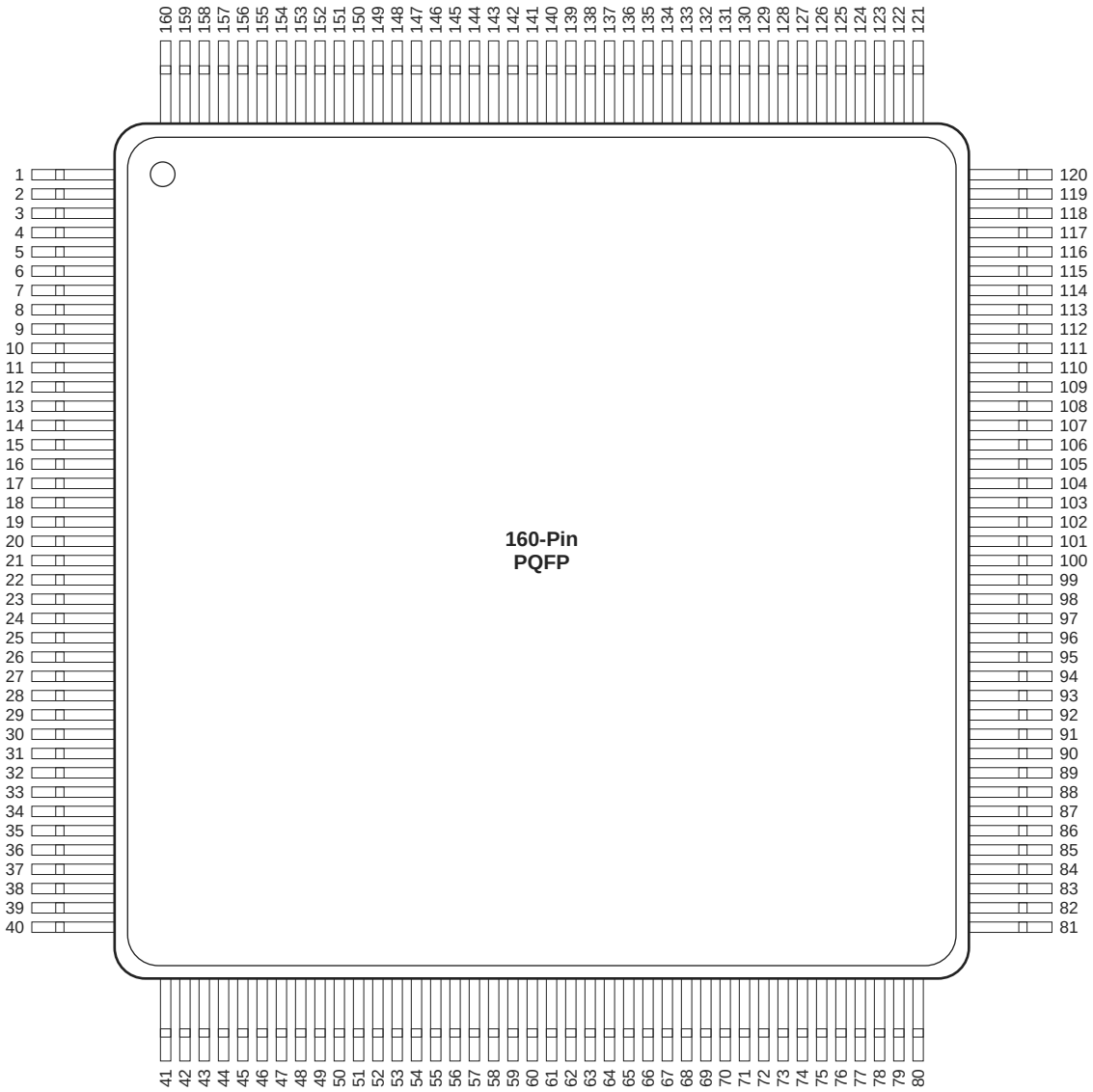


Note: This is the top view of the package.

Note

For Package Manufacturing and Environmental information, visit the Resource Center at http://www.microsemi.com/soc/products/solutions/package/docs.aspx.

PQ160



Note: This is the top view of the package

Note

For Package Manufacturing and Environmental information, visit the Resource Center at http://www.microsemi.com/soc/products/solutions/package/docs.aspx

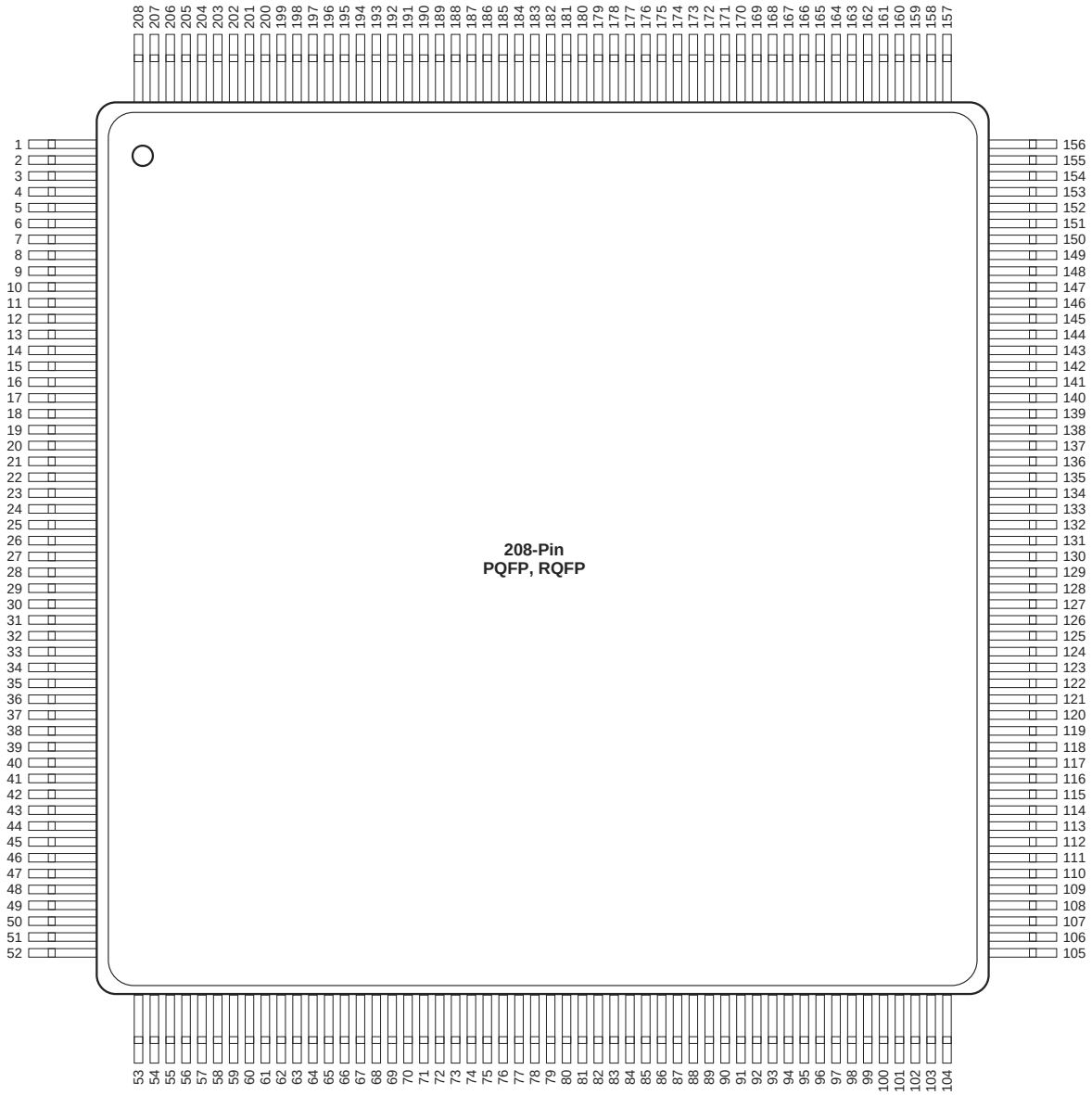
PQ160			
Pin Number	**A1425, A14V25 Function**	**A1440, A14V40 Function**	**A1460, A14V60 Function**
1	GND	GND	GND
2	SDI, I/O	SDI, I/O	SDI, I/O
5	NC	I/O	I/O
9	MODE	MODE	MODE
10	VCC	VCC	VCC
14	NC	I/O	I/O
15	GND	GND	GND
18	VCC	VCC	VCC
19	GND	GND	GND
20	NC	I/O	I/O
24	NC	I/O	I/O
27	NC	I/O	I/O
28	VCC	VCC	VCC
29	VCC	VCC	VCC
40	GND	GND	GND
41	NC	I/O	I/O
43	NC	I/O	I/O
45	NC	I/O	I/O
46	VCC	VCC	VCC
47	NC	I/O	I/O
49	NC	I/O	I/O
51	NC	I/O	I/O
53	NC	I/O	I/O
58	PRB, I/O	PRB, I/O	PRB, I/O
59	GND	GND	GND
60	VCC	VCC	VCC
62	HCLK, I/O	HCLK, I/O	HCLK, I/O
63	GND	GND	GND
74	NC	I/O	I/O
75	VCC	VCC	VCC
76	NC	I/O	I/O
77	NC	I/O	I/O
78	NC	I/O	I/O
79	SDO	SDO	SDO
80	IOPCL, I/O	IOPCL, I/O	IOPCL, I/O
81	GND	GND	GND
90	VCC	VCC	VCC
91	VCC	VCC	VCC

PQ160			
Pin Number	**A1425, A14V25 Function**	**A1440, A14V40 Function**	**A1460, A14V60 Function**
92	NC	I/O	I/O
93	NC	I/O	I/O
98	GND	GND	GND
99	VCC	VCC	VCC
100	NC	I/O	I/O
103	GND	GND	GND
107	NC	I/O	I/O
109	NC	I/O	I/O
110	VCC	VCC	VCC
111	GND	GND	GND
112	VCC	VCC	VCC
113	NC	I/O	I/O
119	NC	I/O	I/O
120	IOCLK, I/O	IOCLK, I/O	IOCLK, I/O
121	GND	GND	GND
124	NC	I/O	I/O
127	NC	I/O	I/O
136	CLKA, I/O	CLKA, I/O	CLKA, I/O
137	CLKB, I/O	CLKB, I/O	CLKB, I/O
138	VCC	VCC	VCC
139	GND	GND	GND
140	VCC	VCC	VCC
141	GND	GND	GND
142	PRA, I/O	PRA, I/O	PRA, I/O
143	NC	I/O	I/O
145	NC	I/O	I/O
147	NC	I/O	I/O
149	NC	I/O	I/O
151	NC	I/O	I/O
153	NC	I/O	I/O
154	VCC	VCC	VCC
160	DCLK, I/O	DCLK, I/O	DCLK, I/O

Notes:

1. All unlisted pin numbers are user I/Os.
2. NC denotes no connection.
3. MODE should be terminated to GND through a 10K resistor to enable Actionprobe usage; otherwise it can be terminated directly to GND.

PQ208, RQ208



Note: This is the top view of the package

Note

For Package Manufacturing and Environmental information, visit the Resource Center at http://www.microsemi.com/soc/products/solutions/package/docs.aspx

PQ208, RQ208		
Pin Number	A1460, A14V60 Function	A14100, A14V100 Function
1	GND	GND
2	SDI, I/O	SDI, I/O
11	MODE	MODE
12	VCC	VCC
25	VCC	VCC
26	GND	GND
27	VCC	VCC
28	GND	GND
40	VCC	VCC
41	VCC	VCC
52	GND	GND
53	NC	I/O
60	VCC	VCC
65	NC	I/O
76	PRB, I/O	PRB, I/O
77	GND	GND
78	VCC	VCC
79	GND	GND
80	VCC	VCC
82	HCLK, I/O	HCLK, I/O
98	VCC	VCC
102	NC	I/O
103	SDO	SDO
104	IOPCL, I/O	IOPCL, I/O
105	GND	GND
114	VCC	VCC

PQ208, RQ208		
Pin Number	A1460, A14V60 Function	A14100, A14V100 Function
115	VCC	VCC
116	NC	I/O
129	GND	GND
130	VCC	VCC
131	GND	GND
132	VCC	VCC
145	VCC	VCC
146	GND	GND
147	NC	I/O
148	VCC	VCC
156	IOCLK, I/O	IOCLK, I/O
157	GND	GND
158	NC	I/O
164	VCC	VCC
180	CLKA, I/O	CLKA, I/O
181	CLKB, I/O	CLKB, I/O
182	VCC	VCC
183	GND	GND
184	VCC	VCC
185	GND	GND
186	PRA, I/O	PRA, I/O
195	NC	I/O
201	VCC	VCC
205	NC	I/O
208	DCLK, I/O	DCLK, I/O

Notes:

1. All unlisted pin numbers are user I/Os.
2. NC denotes no connection.
3. MODE should be terminated to GND through a 10K resistor to enable Actionprobe usage; otherwise it can be terminated directly to GND.

CQ132	
Pin Number	**A1425 Function**
1	NC
2	GND
3	SDI, I/O
9	MODE
10	GND
11	VCC
22	VCC
26	GND
27	VCC
34	NC
36	GND
42	GND
43	VCC
48	PRB, I/O
50	HCLK, I/O
58	GND
59	VCC
63	SDO
64	IOPCL, I/O
65	GND
66	NC

CQ132	
Pin Number	**A1425 Function**
67	NC
74	GND
75	VCC
78	VCC
89	VCC
90	GND
91	VCC
92	GND
98	IOCLK, I/O
99	NC
100	NC
101	GND
106	GND
107	VCC
116	CLKA, I/O
117	CLKB, I/O
118	PRA, I/O
122	GND
123	VCC
131	DCLK, I/O
132	NC

Notes:

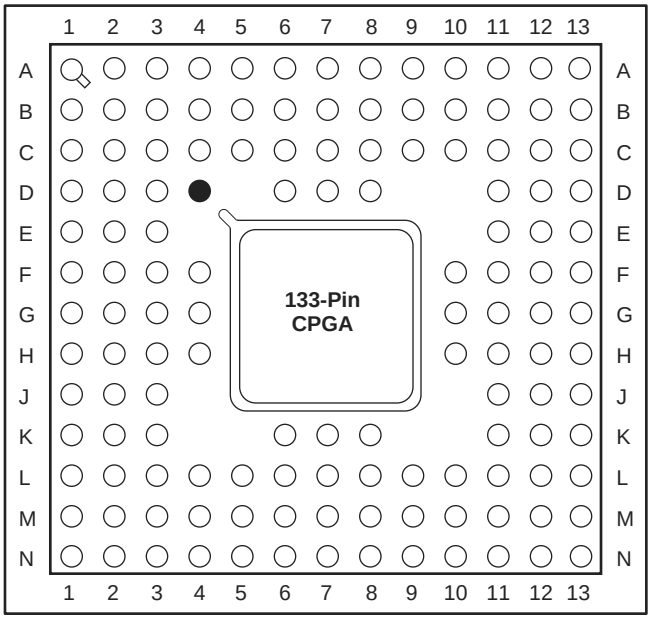
1. All unlisted pin numbers are user I/Os.
2. NC denotes no connection.
3. MODE should be terminated to GND through a 10K resistor to enable Actionprobe usage; otherwise it can be terminated directly to GND.

PG100	
A1415 Function	**Location**
CLKA or I/O	C7
CLKB or I/O	D6
DCLK or I/O	C4
GND	C3, C6, C9, E9, F3, F9, J3, J6, J8, J9
HCLK or I/O	H6
IOCLK or I/O	C10
IOPCL or I/O	K9
MODE	C2
PRA or I/O	A6
PRB or I/O	L3
SDI or I/O	B3
SDO	L9
VCC	B6, B10, E11, F2, F10, G2, K2, K6, K10

Notes:

1. All unlisted pin numbers are user I/Os.
2. NC denotes no connection.
3. MODE should be terminated to GND through a 10K resistor to enable Actionprobe usage; otherwise it can be terminated directly to GND.
4. The PG100 package has been discontinued.

PG133



Note: This is the top view.

Note

For Package Manufacturing and Environmental information, visit the Resource Center at http://www.microsemi.com/soc/products/solutions/package/docs.aspx

PG133	
A1425 Function	**Location**
CLKA or I/O	D7
CLKB or I/O	B6
DCLK or I/O	D4
GND	A2, C3, C7, C11, C12, F10, G3, G11, L3, L7, L11, M3, N12
HCLK or I/O	K7
IOCLK or I/O	C10
IOPCL or I/O	L10
MODE	E3
NC	A1, A7, A13, G1, G13, N1, N7, N13
PRA or I/O	A6
PRB or I/O	L6
SDI or I/O	C2
SDO	M11
VCC	B2, B7, B12, E11, G2, G12, J2, J12, M2, M7, M12

Notes:

1. All unlisted pin numbers are user I/Os.
2. NC denotes no connection.
3. MODE should be terminated to GND through a 10K resistor to enable Actionprobe usage; otherwise it can be terminated directly to GND.
4. The PG133 package has been discontinued.

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