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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	310
Number of Logic Elements/Cells	-
Total RAM Bits	-
Number of I/O	80
Number of Gates	2500
Voltage - Supply	4.5V ~ 5.5V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 85°C (TA)
Package / Case	100-BQFP
Supplier Device Package	100-PQFP (20x14)
Purchase URL	https://www.e-xfl.com/product-detail/microsemi/a1425a-pq100i

Product Plan

Device/Package	Speed Grade[1]				Application[1]			
	Std.	–1	–2	–3	C	I	M	B
A1415A Device								
84-Pin Plastic Leaded Chip Carrier (PLCC)	✓	✓	D	D	✓	✓	✓	–
100-Pin Plastic Quad Flatpack (PQFP)	✓	✓	D	D	✓	✓	✓	–
100-Pin Very Thin Quad Flatpack (VQFP)	✓	✓	D	D	✓	✓	✓	–
100-Pin Ceramic Pin Grid Array (CPGA)	D	D	D	D	D	–	–	–
A14V15A Device								
84-Pin Plastic Leaded Chip Carrier (PLCC)	✓	–	–	–	✓	–	–	–
100-Pin Very Thin Quad Flatpack (VQFP)	✓	–	–	–	✓	–	–	–
A1425A Device								
84-Pin Plastic Leaded Chip Carrier (PLCC)	✓	✓	D	D	✓	✓		
100-Pin Plastic Quad Flatpack (PQFP)	✓	✓	D	D	✓	✓	–	–
100-Pin Very Thin Quad Flatpack (VQFP)	✓	✓	D	D	✓	✓	–	–
132-Pin Ceramic Quad Flatpack (CQFP)	✓	✓	–	–	✓	–	✓	✓
133-Pin Ceramic Pin Grid Array (CPGA)	D	D	D	D	D	–	D	D
160-Pin Plastic Quad Flatpack (PQFP)	✓	✓	D	D	✓	✓	–	–
A14V25A Device								
84-Pin Plastic Leaded Chip Carrier (PLCC)	✓	–	–	–	✓	–	–	–
100-Pin Very Thin Quad Flatpack (VQFP)	✓	–	–	–	✓	–	–	–
160-Pin Plastic Quad Flatpack (PQFP)	✓	–	–	–	✓	–	–	–
A1440A Device								
84-Pin Plastic Leaded Chip Carrier (PLCC)	✓	✓	D	D	✓	✓	–	–
100-Pin Very Thin Quad Flatpack (VQFP)	✓	✓	D	D	✓	✓	–	–
160-Pin Plastic Quad Flatpack (PQFP)	✓	✓	D	D	✓	✓	–	–
175-Pin Ceramic Pin Grid Array (CPGA)	D	D	D	D	D	–	–	–
176-Pin Thin Quad Flatpack (TQFP)	✓	✓	D	D	✓	✓	–	–

Notes:

1. *Applications:*
   C = Commercial
   I = Industrial
   M = Military
2. *Commercial only*

Availability:
✓ = Available
P = Planned
– = Not planned
D = Discontinued

Speed Grade:
–1 = Approx. 15% faster than Std.
–2 = Approx. 25% faster than Std.
–3 = Approx. 35% faster than Std.
(–2 and –3 speed grades have been discontinued.)

ACT 3 Family Overview

Detailed Specifications

Package Pin Assignments

Datasheet Information

1 – ACT 3 Family Overview

General Description

Microsemi's ACT 3 Accelerator Series of FPGAs offers the industry's fastest high-capacity programmable logic device. ACT 3 FPGAs offer a high performance, PCI compliant programmable solution capable of 186 MHz on-chip performance and 9.0 nanosecond clock-to-output (–1 speed grade), with capacities spanning from 1,500 to 10,000 gate array equivalent gates.

The ACT 3 family builds on the proven two-module architecture consisting of combinatorial and sequential logic modules used in Microsemi's 3200DX and 1200XL families. In addition, the ACT 3 I/O modules contain registers which deliver 9.0 nanosecond clock-to-out times (–1 speed grade). The devices contain four clock distribution networks, including dedicated array and I/O clocks, supporting very fast synchronous and asynchronous designs. In addition, routed clocks can be used to drive high fanout signals such as flip-flop resets and output.

The ACT 3 family is supported by Microsemi's Designer Series Development System which offers automatic placement and routing (with automatic or fixed pin assignments), static timing analysis, user programming, and debug and diagnostic probe capabilities.

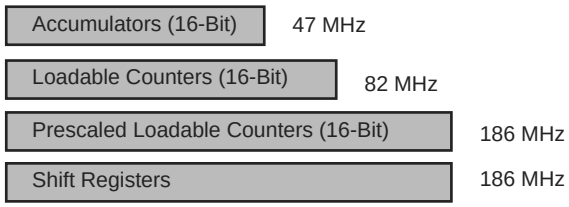
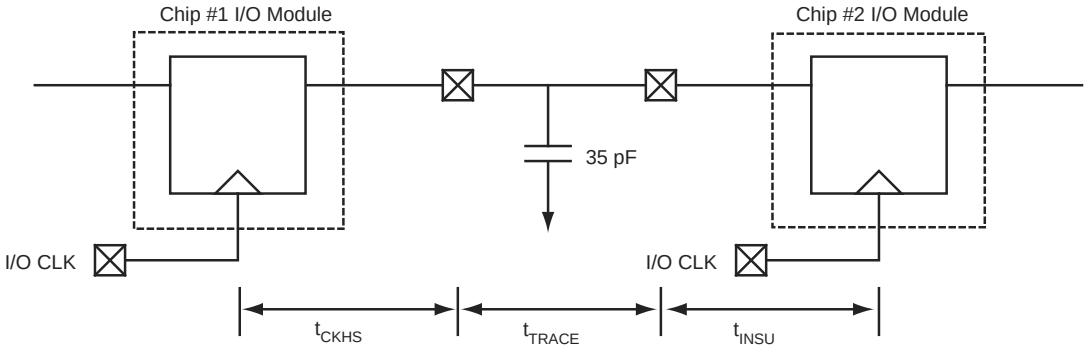


Figure 1-1 • **Predictable Performance (worst-case commercial, –1 speed grade)**

System Performance Model



Horizontal Routing

Horizontal channels are located between the rows of modules and are composed of several routing tracks. The horizontal routing tracks within the channel are divided into one or more segments. The minimum horizontal segment length is the width of a module-pair, and the maximum horizontal segment length is the full length of the channel. Any segment that spans more than one-third the row length is considered a long horizontal segment. A typical channel is shown in Figure 2-7. Undedicated horizontal routing tracks are used to route signal nets. Dedicated routing tracks are used for the global clock networks and for power and ground tie-off tracks.

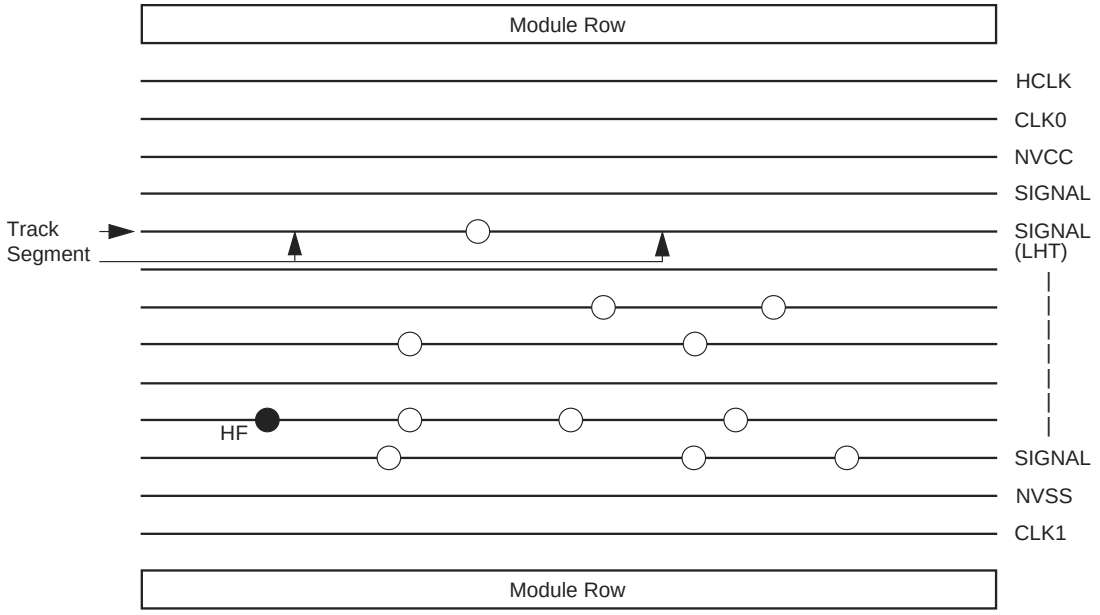


Figure 2-7 • **Horizontal Routing Tracks and Segments**

Vertical Routing

Other tracks run vertically through the modules. Vertical tracks are of three types: input, output, and long. Vertical tracks are also divided into one or more segments. Each segment in an input track is dedicated to the input of a particular module. Each segment in an output track is dedicated to the output of a particular module. Long segments are uncommitted and can be assigned during routing. Each output segment spans four channels (two above and two below), except near the top and bottom of the array where edge effects occur. LVTs contain either one or two segments. An example of vertical routing tracks and segments is shown in Figure 2-8.

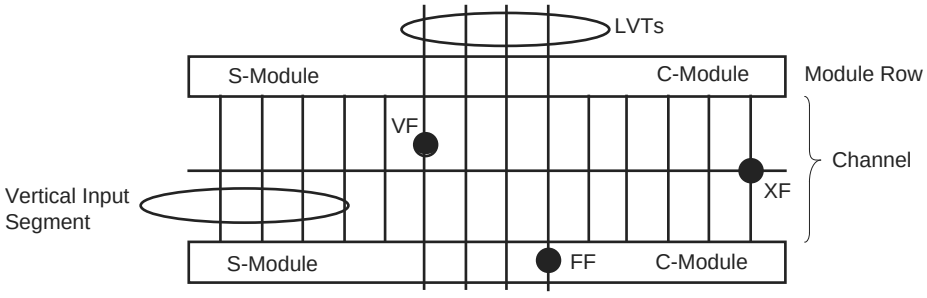


Figure 2-8 • **Vertical Routing Tracks and Segments**

Antifuse Connections

An antifuse is a “normally open” structure as opposed to the normally closed fuse structure used in PROMs or PALs. The use of antifuses to implement a programmable logic device results in highly testable structures as well as an efficient programming architecture. The structure is highly testable because there are no preexisting connections; temporary connections can be made using pass transistors. These temporary connections can isolate individual antifuses to be programmed as well as isolate individual circuit structures to be tested. This can be done both before and after programming. For example, all metal tracks can be tested for continuity and shorts between adjacent tracks, and the functionality of all logic modules can be verified.

Four types of antifuse connections are used in the routing structure of the ACT 3 array. (The physical structure of the antifuse is identical in each case; only the usage differs.)

Table 2-1 shows four types of antifuses.

Table 2-1 • **Antifuse Types**

Type	Description
XF	Horizontal-to-vertical connection
HF	Horizontal-to-horizontal connection
VF	Vertical-to-vertical connection
FF	"Fast" vertical connection

Examples of all four types of connections are shown in Figure 2-7 on page 2-6 and Figure 2-8 on page 2-6.

Module Interface

Connections to Logic and I/O modules are made through vertical segments that connect to the module inputs and outputs. These vertical segments lie on vertical tracks that span the entire height of the array.

Module Input Connections

The tracks dedicated to module inputs are segmented by pass transistors in each module row. During normal user operation, the pass transistors are inactive, which isolates the inputs of a module from the inputs of the module directly above or below it. During certain test modes, the pass transistors are active to verify the continuity of the metal tracks. Vertical input segments span only the channel above or the channel below. The logic modules are arranged such that half of the inputs are connected to the channel above and half of the inputs to segments in the channel below, as shown in Figure 2-9.

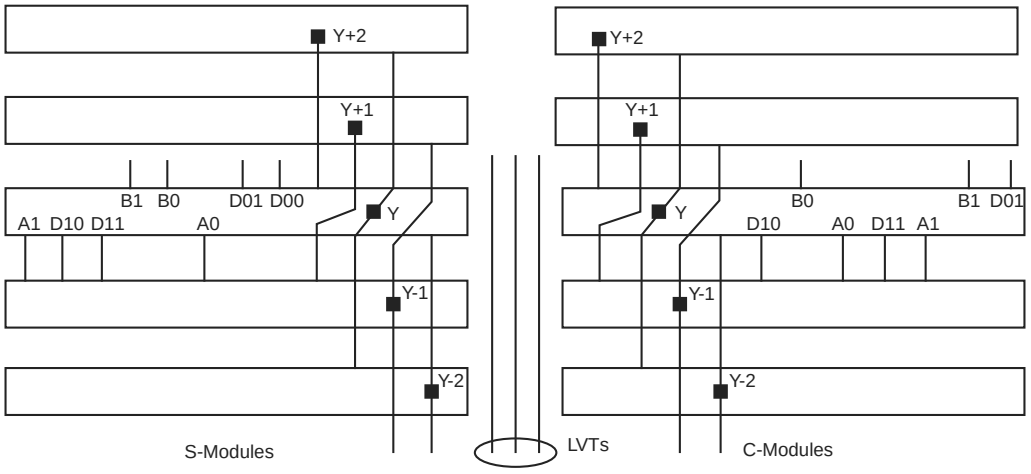


Figure 2-9 • **Logic Module Routing Interface**

3.3 V Operating Conditions

Table 2-5 • **Absolute Maximum Ratings[1], Free Air Temperature Range**

Symbol	Parameter	Limits	Units
VCC	DC supply voltage	–0.5 to +7.0	V
VI	Input voltage	–0.5 to VCC + 0.5	V
VO	Output voltage	–0.5 to VCC + 0.5	V
IIO	I/O source sink current[2]	±20	mA
T_{STG}	Storage temperature	–65 to +150	°C

Notes:

1. *Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum rated conditions for extended periods may affect device reliability. Device should not be operated outside the recommended operating conditions.*
2. *Device inputs are normally high impedance and draw extremely low current. However, when input voltage is greater than VCC + 0.5 V for less than GND –0.5 V, the internal protection diodes will forward bias and can draw excessive current.*

Table 2-6 • **Recommended Operating Conditions**

Parameter	Commercial	Units
Temperature range*	0 to +70	°C
Power supply tolerance	3.0 to 3.6	V

*Note: *Ambient temperature (T_A) is used for commercial.*

Table 2-7 • **Electrical Specifications**

Parameter		Commercial		Units
		Min.	Max.	
VOH[1]	IOH = –4 mA	2.15	–	V
	IOH = –3.2 mA	2.4		V
VOL[1]	IOL = 6 mA		0.4	V
VIL		–0.3	0.8	V
VIH		2.0	VCC + 0.3	V
Input transition time t_R, t_F[2]	VI = VCC or GND	–10	+10	µA
C_{IO} I/O Capacitance[2,3]			10	pF
Standby current, ICC[4] (typical = 0.3 mA)			0.75	mA
Leakage current[5]		–10	10	µA

1. *Only one output tested at a time. VCC = minimum.*
2. *Not tested; for information only.*
3. *Includes worst-case 84-pin PLCC package capacitance. VOUT = 0 V, f - 1 MHz.*
4. *Typical standby current = 0.3 mA. All outputs unloaded. All inputs = VCC or GND.*
5. *VO, VIN = VCC or GND*

Equivalent capacitance is calculated by measuring ICC active at a specified frequency and voltage for each circuit component of interest. Measurements have been made over a range of frequencies at a fixed value of VCC. Equivalent capacitance is frequency independent so that the results may be used over a wide range of operating conditions. Equivalent capacitance values are shown in Figure 2-10.

***Table 2-10* • CEQ Values for Microsemi FPGAs**

Item	CEQ Value
Modules (C_{EQM})	6.7
Input Buffers (C_{EQI})	7.2
Output Buffers (C_{EQO})	10.4
Routed Array Clock Buffer Loads (C_{EQCR})	1.6
Dedicated Clock Buffer Loads (C_{EQCD})	0.7
I/O Clock Buffer Loads ($C_{EQCI)}$	0.9

To calculate the active power dissipated from the complete design, the switching frequency of each part of the logic must be known. EQ 5 shows a piece-wise linear summation over all components.

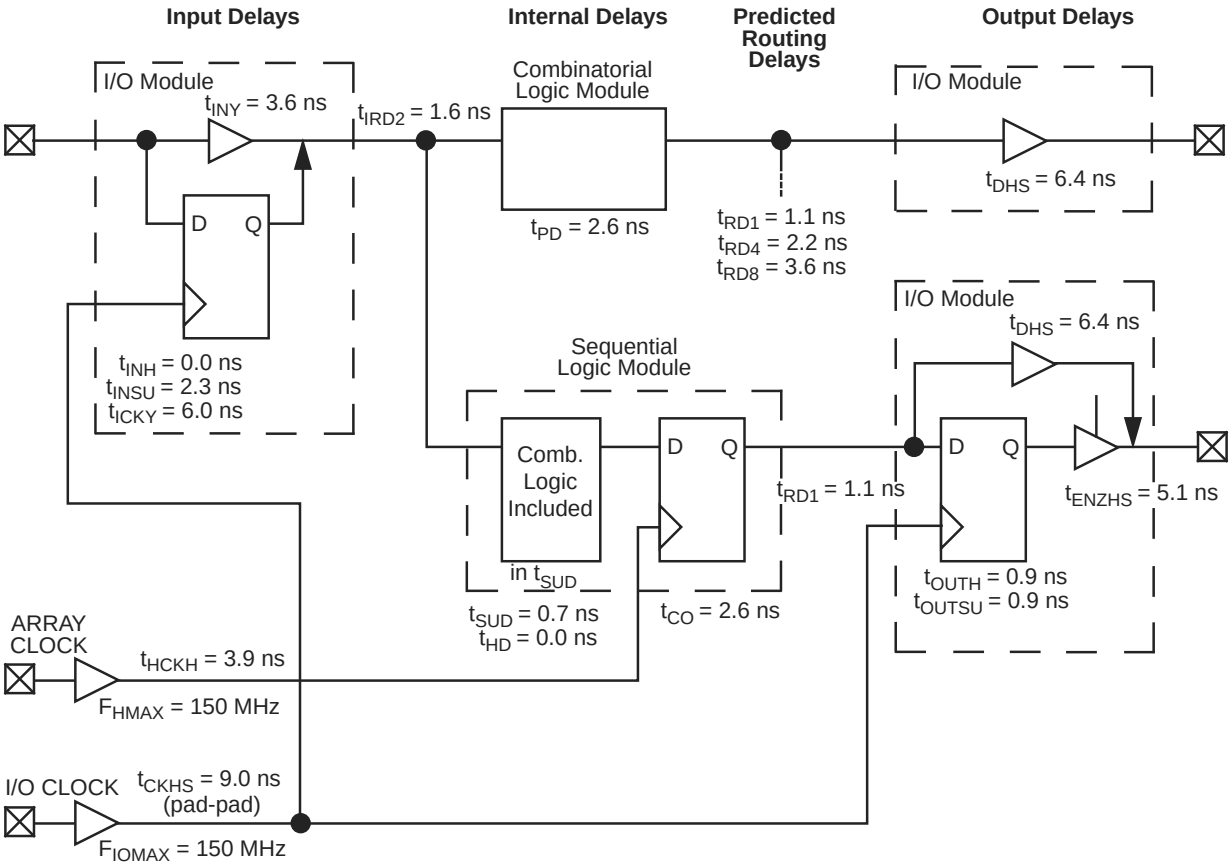
$$\text{Power} = VCC^2 * [(m * C_{EQM} * f_m)_{modules} + (n * C_{EQI} * f_n)_{inputs} + (p * (C_{EQO} + C_L) * fp)_{outputs} + 0.5 * (q1 * C_{EQCR} * f_{q1})_{routed\_Clk1} + (r1 * fq1)_{routed\_Clk1} + 0.5 * (q2 * C_{EQCR} * fq2)_{routed\_Clk2} + (r_2 * f_{q2})_{routed\_Clk2} + 0.5 * (s_1 * C_{EQCD} * f_{s1})_{dedicated\_Clk} + (s_2 * C_{EQCI} * f_{s2})_{IO\_Clk}]$$

EQ 5

Where:

m = Number of logic modules switching at f_m
n = Number of input buffers switching at f_n
p = Number of output buffers switching at f_p
q1 = Number of clock loads on the first routed array clock
q2 = Number of clock loads on the second routed array clock
r_1 = Fixed capacitance due to first routed array clock
r_2 = Fixed capacitance due to second routed array clock
s_1 = Fixed number of clock loads on the dedicated array clock
s_2 = Fixed number of clock loads on the dedicated I/O clock
C_{EQM} = Equivalent capacitance of logic modules in pF
C_{EQI} = Equivalent capacitance of input buffers in pF
C_{EQO} = Equivalent capacitance of output buffers in pF
C_{EQCR} = Equivalent capacitance of routed array clock in pF
C_{EQCD} = Equivalent capacitance of dedicated array clock in pF
C_{EQCI} = Equivalent capacitance of dedicated I/O clock in pF
C_L = Output lead capacitance in pF
f_m = Average logic module switching rate in MHz
f_n = Average input buffer switching rate in MHz
f_p = Average output buffer switching rate in MHz
f_{q1} = Average first routed array clock rate in MHz
f_{q2} = Average second routed array clock rate in MHz
f_{s1} = Average dedicated array clock rate in MHz
f_{s2} = Average dedicated I/O clock rate in MHz

ACT 3 Timing Model



Note: Values shown for A1425A –1 speed grade device.

Figure 2-10 • **Timing Model**

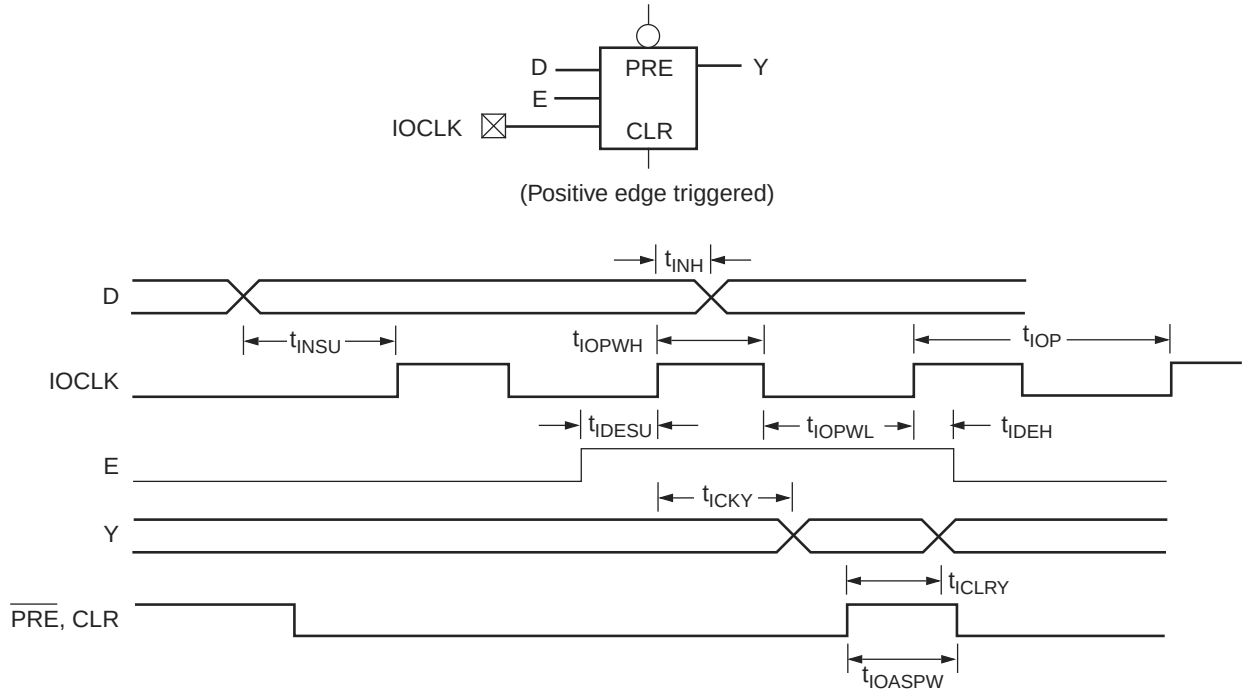


Figure 2-16 • **I/O Module: Sequential Input Timing Characteristics**

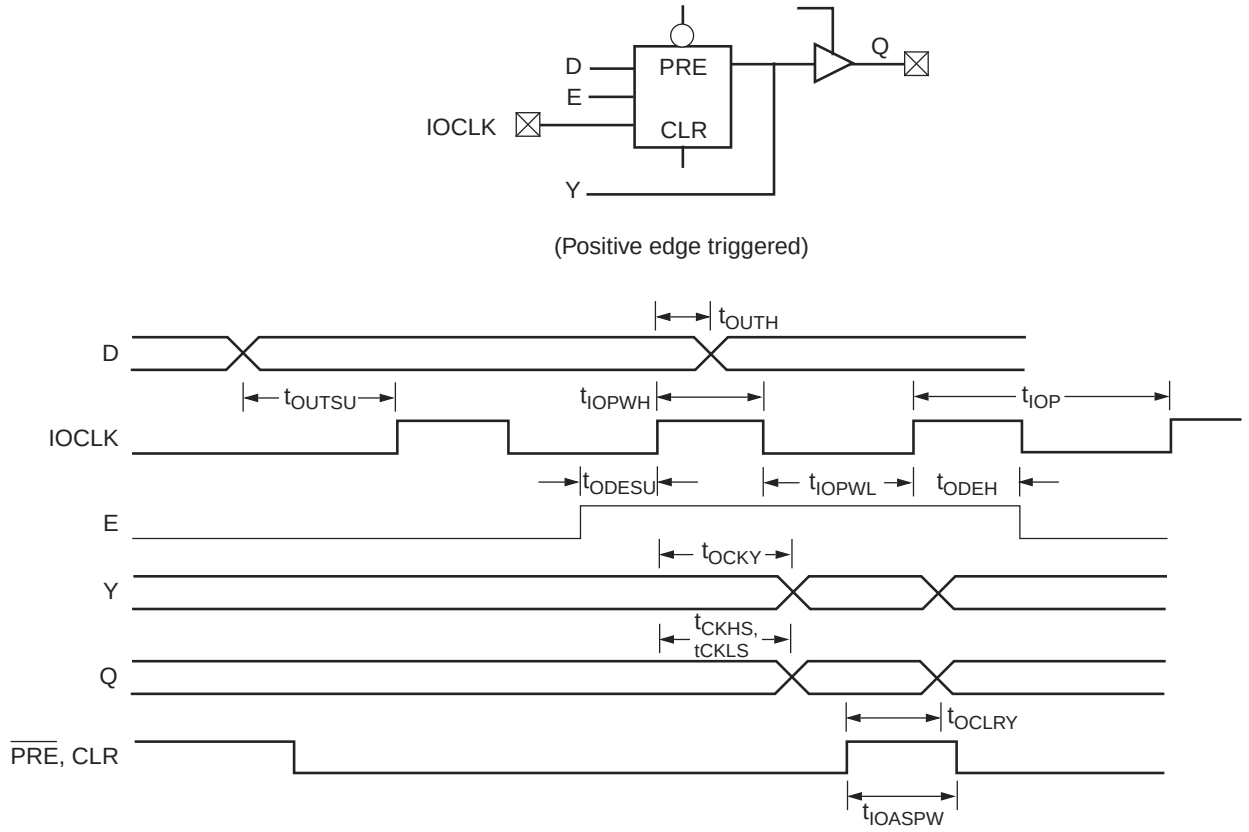


Figure 2-17 • **I/O Module: Sequential Output Timing Characteristics**

A1415A, A14V15A Timing Characteristics

Table 2-18 • A1415A, A14V15A Worst-Case Commercial Conditions, VCC = 4.75 V, T_J = 70°C[1]

Logic Module Propagation Delays[2]		–3 Speed[3]		–2 Speed[3]		–1 Speed		Std. Speed		3.3 V Speed[1]		Units
Parameter/Description		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t_{PD}	Internal Array Module		2.0		2.3		2.6		3.0		3.9	ns
t_{CO}	Sequential Clock to Q		2.0		2.3		2.6		3.0		3.9	ns
t_{CLR}	Asynchronous Clear to Q		2.0		2.3		2.6		3.0		3.9	ns
Predicted Routing Delays[4]												
t_{RD1}	FO = 1 Routing Delay		0.9		1.0		1.1		1.3		1.7	ns
t_{RD2}	FO = 2 Routing Delay		1.2		1.4		1.6		1.8		2.4	ns
t_{RD3}	FO = 3 Routing Delay		1.4		1.6		1.8		2.1		2.8	ns
t_{RD4}	FO = 4 Routing Delay		1.7		1.9		2.2		2.5		3.3	ns
t_{RD8}	FO = 8 Routing Delay		2.8		3.2		3.6		4.2		5.5	ns
Logic Module Sequential Timing												
t_{SUD}	Flip-Flop Data Input Setup	0.5		0.6		0.7		0.8		0.8		ns
t_{HD}	Flip-Flop Data Input Hold	0.0		0.0		0.0		0.0		0.0		ns
t_{SUD}	Latch Data Input Setup	0.5		0.6		0.7		0.8		0.8		ns
t_{HD}	Latch Data Input Hold	0.0		0.0		0.0		0.0		0.0		ns
t_{WASYN}	Asynchronous Pulse Width	1.9		2.4		3.2		3.8		4.8		ns
t_{WCLKA}	Flip-Flop Clock Pulse Width	1.9		2.4		3.2		3.8		4.8		ns
t_A	Flip-Flop Clock Input Period	4.0		5.0		6.8		8.0		10.0		ns
f_{MAX}	Flip-Flop Clock Frequency		250		200		150		125		100	MHz

Notes:

1. *VCC = 3.0 V for 3.3 V specifications.*
2. *For dual-module macros, use $t_{PD} + t_{RD1} + t_{PDn} + t_{CO} + t_{RD1} + t_{PDn}$ or $t_{PD1} + t_{RD1} + t_{SUD}$, whichever is appropriate.*
3. *The –2 and –3 speed grades have been discontinued. Please refer to the Product Discontinuation Notices (PDNs) listed below:*

   PDN March 2001
   PDN 0104
   PDN 0203
   PDN 0604
   PDN 1004
4. *Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual worst-case performance. Post-route timing is based on actual routing delay measurements performed on the device prior to shipment.*

A1415A, A14V15A Timing Characteristics (continued)

***Table 2-21* • A1415A, A14V15A Worst-Case Commercial Conditions, VCC = 4.75 V, T_J = 70°C**

Dedicated (hardwired) I/O Clock Network		–3 Speed		–2 Speed		–1 Speed		Std. Speed		3.3 V Speed[1]		Units
Parameter/Description		**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	
t_{IOCKH}	Input Low to High (pad to I/O module input)		2.0		2.3		2.6		3.0		3.5	ns
t_{IOPWH}	Minimum Pulse Width High	1.9		2.4		3.3		3.8		4.8		ns
t_{IPOWL}	Minimum Pulse Width Low	1.9		2.4		3.3		3.8		4.8		ns
t_{IOSAPW}	Minimum Asynchronous Pulse Width	1.9		2.4		3.3		3.8		4.8		ns
t_{IOCKSW}	Maximum Skew		0.4		0.4		0.4		0.4		0.4	ns
t_{IOP}	Minimum Period	4.0		5.0		6.8		8.0		10.0		ns
f_{IOMAX}	Maximum Frequency		250		200		150		125		100	MHz
Dedicated (hardwired) Array Clock												
t_{HCKH}	Input Low to High (pad to S-module input)		3.0		3.4		3.9		4.5		5.5	ns
t_{HCKL}	Input High to Low (pad to S-module input)		3.0		3.4		3.9		4.5		5.5	ns
t_{HPWH}	Minimum Pulse Width High	1.9		2.4		3.3		3.8		4.8		ns
t_{HPWL}	Minimum Pulse Width Low	1.9		2.4		3.3		3.8		4.8		ns
t_{HCKSW}	Delta High to Low, Low Slew		0.3		0.3		0.3		0.3		0.3	ns
t_{HP}	Minimum Period	4.0		5.0		6.8		8.0		10.0		ns
f_{HMAX}	Maximum Frequency		250		200		150		125		100	MHz
Routed Array Clock Networks												
t_{RCKH}	Input Low to High (FO = 64)		3.7		4.1		4.7		5.5		9.0	ns
t_{RCKL}	Input High to Low (FO = 64)		4.0		4.5		5.1		6.0		9.0	ns
t_{RPWH}	Min. Pulse Width High (FO = 64)	3.3		3.8		4.2		4.9		6.5		ns
t_{RPWL}	Min. Pulse Width Low (FO = 64)	3.3		3.8		4.2		4.9		6.5		ns
t_{RCKSW}	Maximum Skew (FO = 128)		0.7		0.8		0.9		1.0		1.0	ns
t_{RP}	Minimum Period (FO = 64)	6.8		8.0		8.7		10.0		13.4		ns
f_{RMAX}	Maximum Frequency (FO = 64)		150		125		115		100		75	MHz
Clock-to-Clock Skews												
$t_{IOHCKSW}$	I/O Clock to H-Clock Skew	0.0	1.7	0.0	1.8	0.0	2.0	0.0	2.2	0.0	3.0	ns
$t_{IORCKSW}$	I/O Clock to R-Clock Skew (FO = 64)	0.0	1.0	0.0	1.0	0.0	1.0	0.0	1.0	0.0	3.0	ns
t_{HRCKSW}	H-Clock to R-Clock Skew (FO = 64) (FO = 50% maximum)	0.0	1.0	0.0	1.0	0.0	1.0	0.0	1.0	0.0 0.0	3.0 3.0	ns

Notes:

1. *Delays based on 35 pF loading.*
2. *The –2 and –3 speed grades have been discontinued. Refer to PDN 0104, PDN 0203, PDN 0604, and PDN 1004 at http://www.microsemi.com/soc/support/notifications/default.aspx#pdn.*

A1425A, A14V25A Timing Characteristics

Table 2-22 • A1425A, A14V25A Worst-Case Commercial Conditions, VCC = 4.75 V, T_J = 70°C[1]

Logic Module Propagation Delays[2]		–3 Speed[3]		–2 Speed[3]		–1 Speed		Std. Speed		3.3 V Speed[1]		Units
Parameter/Description		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t_{PD}	Internal Array Module		2.0		2.3		2.6		3.0		3.9	ns
t_{CO}	Sequential Clock to Q		2.0		2.3		2.6		3.0		3.9	ns
t_{CLR}	Asynchronous Clear to Q		2.0		2.3		2.6		3.0		3.9	ns
Predicted Routing Delays[4]												
t_{RD1}	FO = 1 Routing Delay		0.9		1.0		1.1		1.3		1.7	ns
t_{RD2}	FO = 2 Routing Delay		1.2		1.4		1.6		1.8		2.4	ns
t_{RD3}	FO = 3 Routing Delay		1.4		1.6		1.8		2.1		2.8	ns
t_{RD4}	FO = 4 Routing Delay		1.7		1.9		2.2		2.5		3.3	ns
t_{RD8}	FO = 8 Routing Delay		2.8		3.2		3.6		4.2		5.5	ns
Logic Module Sequential Timing												
t_{SUD}	Flip-Flop Data Input Setup	0.5		0.6		0.7		0.8		0.8		ns
t_{HD}	Flip-Flop Data Input Hold	0.0		0.0		0.0		0.0		0.0		ns
t_{SUD}	Latch Data Input Setup	0.5		0.6		0.7		0.8		0.8		ns
t_{HD}	Latch Data Input Hold	0.0		0.0		0.0		0.0		0.0		ns
t_{WASYN}	Asynchronous Pulse Width	1.9		2.4		3.2		3.8		4.8		ns
t_{WCLKA}	Flip-Flop Clock Pulse Width	1.9		2.4		3.2		3.8		4.8		ns
t_A	Flip-Flop Clock Input Period	4.0		5.0		6.8		8.0		10.0		ns
f_{MAX}	Flip-Flop Clock Frequency		250		200		150		125		100	MHz

Notes:

1. *VCC = 3.0 V for 3.3 V specifications.*
2. *For dual-module macros, use $t_{PD} + t_{RD1} + t_{PDn} + t_{CO} + t_{RD1} + t_{PDn}$ or $t_{PD1} + t_{RD1} + t_{SUD}$, whichever is appropriate.*
3. *The –2 and –3 speed grades have been discontinued. Refer to PDN 0104, PDN 0203, PDN 0604, and PDN 1004 at http://www.microsemi.com/soc/support/notifications/default.aspx#pdn.*
4. *Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual worst-case performance. Post-route timing is based on actual routing delay measurements performed on the device prior to shipment.*

A1460A, A14V60A Timing Characteristics

Table 2-30 • A1460A, A14V60A Worst-Case Commercial Conditions, VCC = 4.75 V, T_J = 70°C[1]

Logic Module Propagation Delays[2]		–3 Speed[3]		–2 Speed [3]		–1 Speed		Std. Speed		3.3 V Speed[1]		Units
Parameter/Description		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t_{PD}	Internal Array Module		2.0		2.3		2.6		3.0		3.9	ns
t_{CO}	Sequential Clock to Q		2.0		2.3		2.6		3.0		3.9	ns
t_{CLR}	Asynchronous Clear to Q		2.0		2.3		2.6		3.0		3.9	ns
Predicted Routing Delays[4]												
t_{RD1}	FO = 1 Routing Delay		0.9		1.0		1.1		1.3		1.7	ns
t_{RD2}	FO = 2 Routing Delay		1.2		1.4		1.6		1.8		2.4	ns
t_{RD3}	FO = 3 Routing Delay		1.4		1.6		1.8		2.1		2.8	ns
t_{RD4}	FO = 4 Routing Delay		1.7		1.9		2.2		2.5		3.3	ns
t_{RD8}	FO = 8 Routing Delay		2.8		3.2		3.6		4.2		5.5	ns
Logic Module Sequential Timing												
t_{SUD}	Flip-Flop Data Input Setup	0.5		0.6		0.7		0.8		0.8		ns
t_{HD}	Flip-Flop Data Input Hold	0.0		0.0		0.0		0.0		0.0		ns
t_{SUD}	Latch Data Input Setup	0.5		0.6		0.7		0.8		0.8		ns
t_{HD}	Latch Data Input Hold	0.0		0.0		0.0		0.0		0.0		ns
t_{WASYN}	Asynchronous Pulse Width	2.4		3.2		3.8		4.8		6.5		ns
t_{WCLKA}	Flip-Flop Clock Pulse Width	2.4		3.2		3.8		4.8		6.5		ns
t_A	Flip-Flop Clock Input Period	5.0		6.8		8.0		10.0		13.4		ns
f_{MAX}	Flip-Flop Clock Frequency		200		150		125		100		75	MHz

Notes:

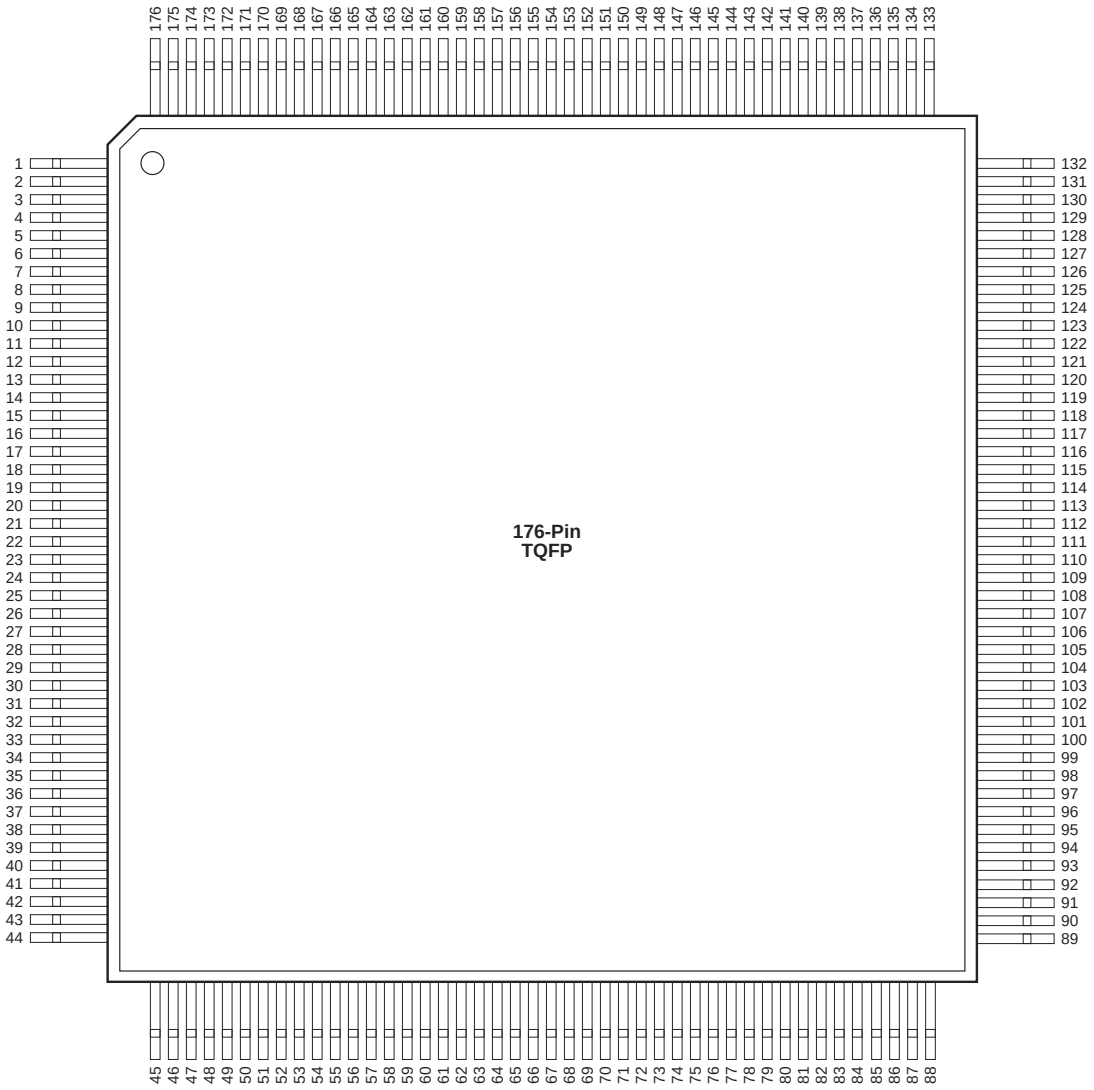
1. *VCC = 3.0 V for 3.3 V specifications.*
2. *For dual-module macros, use $t_{PD} + t_{RD1} + t_{PDn} + t_{CO} + t_{RD1} + t_{PDn}$ or $t_{PD1} + t_{RD1} + t_{SUD}$, whichever is appropriate.*
3. *The –2 and –3 speed grades have been discontinued. Refer to PDN 0104, PDN 0203, PDN 0604, and PDN 1004 at http://www.microsemi.com/soc/support/notifications/default.aspx#pdn.*
4. *Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual worst-case performance. Post-route timing is based on actual routing delay measurements performed on the device prior to shipment.*

PQ100		
Pin Number	**A1415 Function**	**A1425 Function**
2	IOCLK, I/O	IOCLK, I/O
14	CLKA, I/O	CLKA, I/O
15	CLKB, I/O	CLKB, I/O
16	VCC	VCC
17	GND	GND
18	VCC	VCC
19	GND	GND
20	PRA, I/O	PRA, I/O
27	DCLK, I/O	DCLK, I/O
28	GND	GND
29	SDI, I/O	SDI, I/O
34	MODE	MODE
35	VCC	VCC
36	GND	GND
47	GND	GND
48	VCC	VCC
61	PRB, I/O	PRB, I/O
62	GND	GND
63	VCC	VCC
64	GND	GND
65	VCC	VCC
67	HCLK, I/O	HCLK, I/O
77	SDO	SDO
78	IOPCL, I/O	IOPCL, I/O
79	GND	GND
85	VCC	VCC
86	VCC	VCC
87	GND	GND
96	VCC	VCC
97	GND	GND

Notes:

1. All unlisted pin numbers are user I/Os.
2. NC denotes no connection.
3. MODE should be terminated to GND through a 10K resistor to enable Actionprobe usage; otherwise it can be terminated directly to GND.

TQ176



Note: This is the top view.

Note

For Package Manufacturing and Environmental information, visit the Resource Center at http://www.microsemi.com/soc/products/solutions/package/docs.aspx

VQ100			
Pin Number	**A1415, A14V15 Function**	**A1425, A14V25 Function**	**A1440, A14V40 Function**
1	GND	GND	GND
2	SDI, I/O	SDI, I/O	SDI, I/O
7	MODE	MODE	MODE
8	VCC	VCC	VCC
9	GND	GND	GND
20	VCC	VCC	VCC
21	NC	I/O	I/O
34	PRB, I/O	PRB, I/O	PRB, I/O
35	VCC	VCC	VCC
36	GND	GND	GND
37	VCC	VCC	VCC
39	HCLK, I/O	HCLK, I/O	HCLK, I/O
49	SDO	SDO	SDO
50	IOPCL, I/O	IOPCL, I/O	IOPCL, I/O
51	GND	GND	GND
57	VCC	VCC	VCC
58	VCC	VCC	VCC
67	VCC	VCC	VCC
68	GND	GND	GND
69	GND	GND	GND
74	NC	I/O	I/O
75	IOCLK, I/O	IOCLK, I/O	IOCLK, I/O
87	CLKA, I/O	CLKA, I/O	CLKA, I/O
88	CLKB, I/O	CLKB, I/O	CLKB, I/O
89	VCC	VCC	VCC
90	VCC	VCC	VCC
91	GND	GND	GND
92	PRA, I/O	PRA, I/O	PRA, I/O
93	NC	I/O	I/O
100	DCLK, I/O	DCLK, I/O	DCLK, I/O

Notes:

1. All unlisted pin numbers are user I/Os.
2. NC denotes no connection.
3. MODE should be terminated to GND through a 10K resistor to enable Actionprobe usage; otherwise it can be terminated directly to GND.

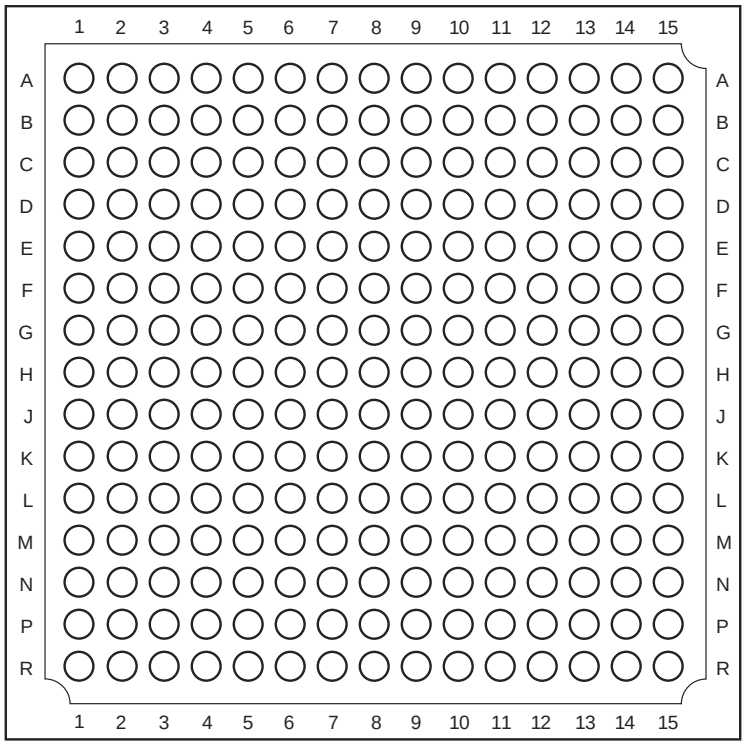
CQ132	
Pin Number	**A1425 Function**
1	NC
2	GND
3	SDI, I/O
9	MODE
10	GND
11	VCC
22	VCC
26	GND
27	VCC
34	NC
36	GND
42	GND
43	VCC
48	PRB, I/O
50	HCLK, I/O
58	GND
59	VCC
63	SDO
64	IOPCL, I/O
65	GND
66	NC

CQ132	
Pin Number	**A1425 Function**
67	NC
74	GND
75	VCC
78	VCC
89	VCC
90	GND
91	VCC
92	GND
98	IOCLK, I/O
99	NC
100	NC
101	GND
106	GND
107	VCC
116	CLKA, I/O
117	CLKB, I/O
118	PRA, I/O
122	GND
123	VCC
131	DCLK, I/O
132	NC

Notes:

1. All unlisted pin numbers are user I/Os.
2. NC denotes no connection.
3. MODE should be terminated to GND through a 10K resistor to enable Actionprobe usage; otherwise it can be terminated directly to GND.

BG225



Note: This is the top view.

Note

For Package Manufacturing and Environmental information, visit the Resource Center at http://www.microsemi.com/soc/products/solutions/package/docs.aspx

PG133	
A1425 Function	**Location**
CLKA or I/O	D7
CLKB or I/O	B6
DCLK or I/O	D4
GND	A2, C3, C7, C11, C12, F10, G3, G11, L3, L7, L11, M3, N12
HCLK or I/O	K7
IOCLK or I/O	C10
IOPCL or I/O	L10
MODE	E3
NC	A1, A7, A13, G1, G13, N1, N7, N13
PRA or I/O	A6
PRB or I/O	L6
SDI or I/O	C2
SDO	M11
VCC	B2, B7, B12, E11, G2, G12, J2, J12, M2, M7, M12

Notes:

1. All unlisted pin numbers are user I/Os.
2. NC denotes no connection.
3. MODE should be terminated to GND through a 10K resistor to enable Actionprobe usage; otherwise it can be terminated directly to GND.
4. The PG133 package has been discontinued.