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### Understanding [Embedded - FPGAs \(Field Programmable Gate Array\)](#)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

### Applications of Embedded - FPGAs

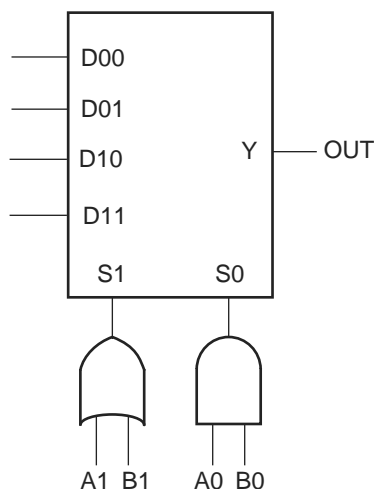
The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

#### Details

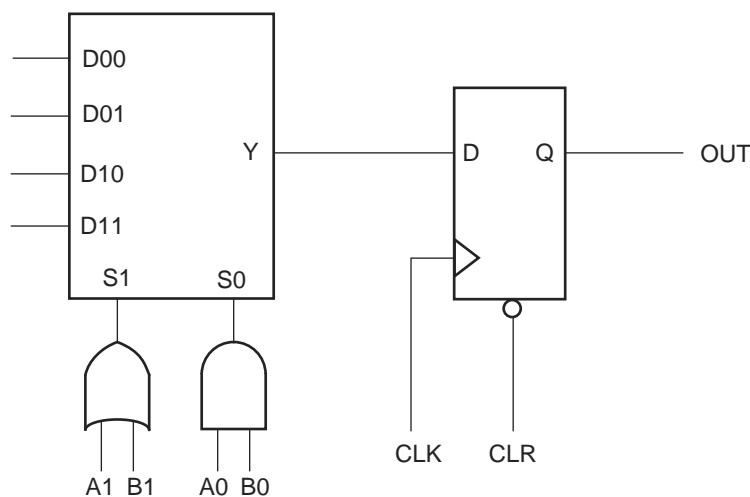
Product Status	Obsolete
Number of LABs/CLBs	310
Number of Logic Elements/Cells	-
Total RAM Bits	-
Number of I/O	100
Number of Gates	2500
Voltage - Supply	4.5V ~ 5.5V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 85°C (TA)
Package / Case	160-BQFP
Supplier Device Package	160-PQFP (28x28)
Purchase URL	<a href="https://www.e-xfl.com/product-detail/microsemi/a1425a-pq160i">https://www.e-xfl.com/product-detail/microsemi/a1425a-pq160i</a>

## Logic Modules

ACT 3 logic modules are enhanced versions of the 1200XL family logic modules. As in the 1200XL family, there are two types of modules: C-modules and S-modules (Figure 2-2 and Figure 2-3). The C-module is functionally equivalent to the 1200XL C-module and implements high fanin combinatorial macros, such as 5-input AND, 5-input OR, and so on. It is available for use as the CM8 hard macro. The S-module is designed to implement high-speed sequential functions within a single module.



**Figure 2-2 • C-Module Diagram**



**Figure 2-3 • S-Module Diagram**

S-modules consist of a full C-module driving a flip-flop, which allows an additional level of logic to be implemented without additional propagation delay. It is available for use as the DFM8A/B and DLM8A/B hard macros. C-modules and S-modules are arranged in pairs called module-pairs. Module-pairs are arranged in alternating patterns and make up the bulk of the array. This arrangement allows the placement software to support two-module macros of four types (CC, CS, SC, and SS). The C-module implements the following function:

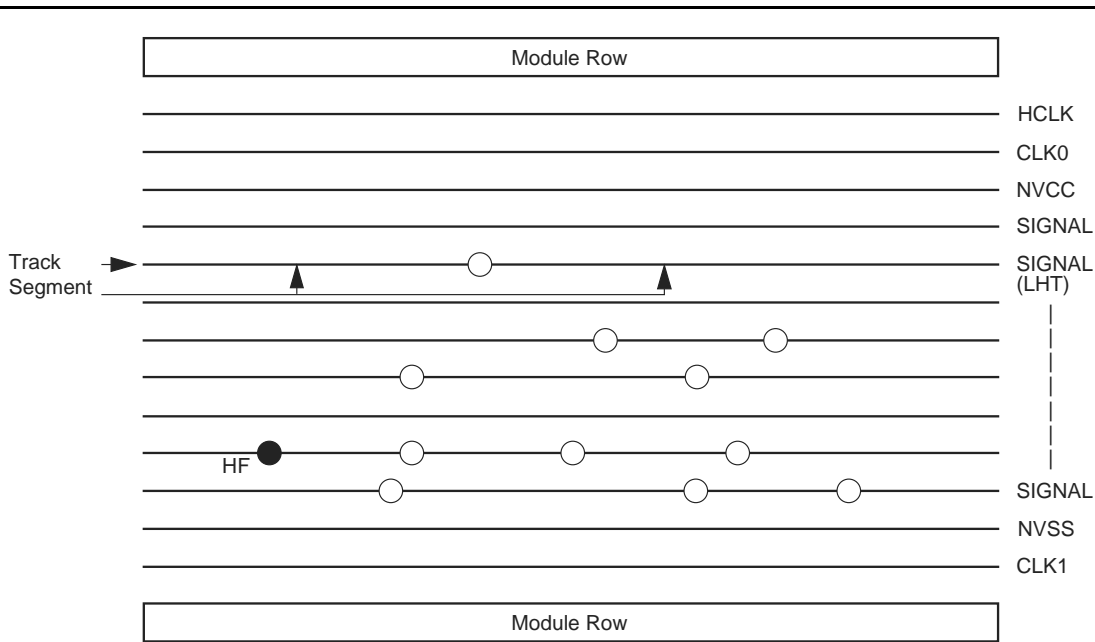
$$Y = !S1 * !S0 * D00 + !S1 * S0 * D01 + S1 * !S0 * D10 + S1 * S0 * D11$$

*EQ 1*

where:  $S0 = A0 * B0$  and  $S1 = A1 + B1$

## Horizontal Routing

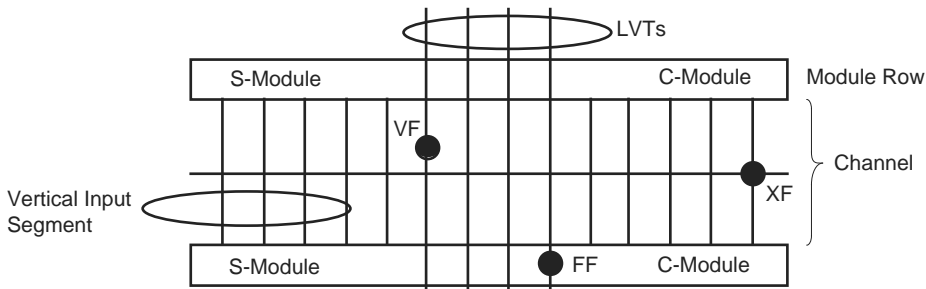
Horizontal channels are located between the rows of modules and are composed of several routing tracks. The horizontal routing tracks within the channel are divided into one or more segments. The minimum horizontal segment length is the width of a module-pair, and the maximum horizontal segment length is the full length of the channel. Any segment that spans more than one-third the row length is considered a long horizontal segment. A typical channel is shown in Figure 2-7. Undedicated horizontal routing tracks are used to route signal nets. Dedicated routing tracks are used for the global clock networks and for power and ground tie-off tracks.



**Figure 2-7 • Horizontal Routing Tracks and Segments**

## Vertical Routing

Other tracks run vertically through the modules. Vertical tracks are of three types: input, output, and long. Vertical tracks are also divided into one or more segments. Each segment in an input track is dedicated to the input of a particular module. Each segment in an output track is dedicated to the output of a particular module. Long segments are uncommitted and can be assigned during routing. Each output segment spans four channels (two above and two below), except near the top and bottom of the array where edge effects occur. LVTs contain either one or two segments. An example of vertical routing tracks and segments is shown in Figure 2-8.



**Figure 2-8 • Vertical Routing Tracks and Segments**

## Power Dissipation

$$P = [ICC_{\text{standby}} + I_{\text{active}}] * VCC * IOL * VOL * N + IOH * (VCC - VOH) * M$$

EQ 3

where:

ICC standby is the current flowing when no inputs or outputs are changing

Iactive is the current flowing due to CMOS switching.

IOL and IOH are TTL sink/source current.

VOL and VOH are TTL level output voltages.

N is the number of outputs driving TTL loads to VOL.

M equals the number of outputs driving TTL loads to VOH.

An accurate determination of N and M is problematical because their values depend on the design and on the system I/O. The power can be divided into two components: static and active.

## Static Power Component

Microsemi FPGAs have small static power components that result in lower power dissipation than PALs or PLDs. By integrating multiple PALs/PLDs into one FPGA, an even greater reduction in board-level power dissipation can be achieved.

The power due to standby current is typically a small component of the overall power. Standby power is calculated in Table 2-9 for commercial, worst case conditions.

**Table 2-9 • Standby Power Calculation**

ICC	VCC	Power
2 mA	5.25 V	10.5 mW

The static power dissipated by TTL loads depends on the number of outputs driving high or low and the DC load current. Again, this value is typically small. For instance, a 32-bit bus sinking 4 mA at 0.33 V will generate 42 mW with all outputs driving low, and 140 mW with all outputs driving high. The actual dissipation will average somewhere between as I/Os switch states with time.

## Active Power Component

Power dissipation in CMOS devices is usually dominated by the active (dynamic) power dissipation. This component is frequency dependent, a function of the logic and the external I/O. Active power dissipation results from charging internal chip capacitances of the interconnect, unprogrammed antifuses, module inputs, and module outputs, plus external capacitance due to PC board traces and load device inputs.

An additional component of the active power dissipation is the totem-pole current in CMOS transistor pairs. The net effect can be associated with an equivalent capacitance that can be combined with frequency and voltage to represent active power dissipation.

## Equivalent Capacitance

The power dissipated by a CMOS circuit can be expressed by EQ 4.

$$\text{Power } (\mu\text{W}) = C_{\text{EQ}} * VCC^2 * F$$

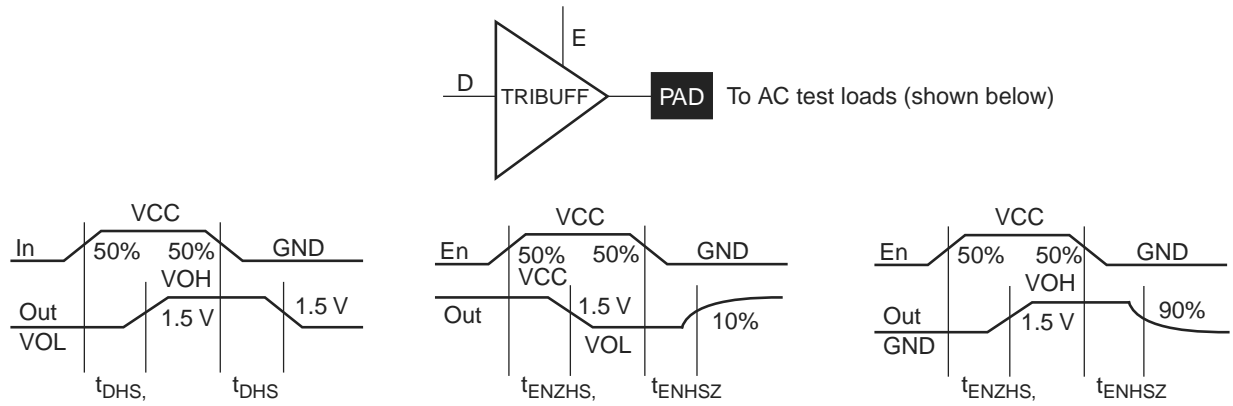
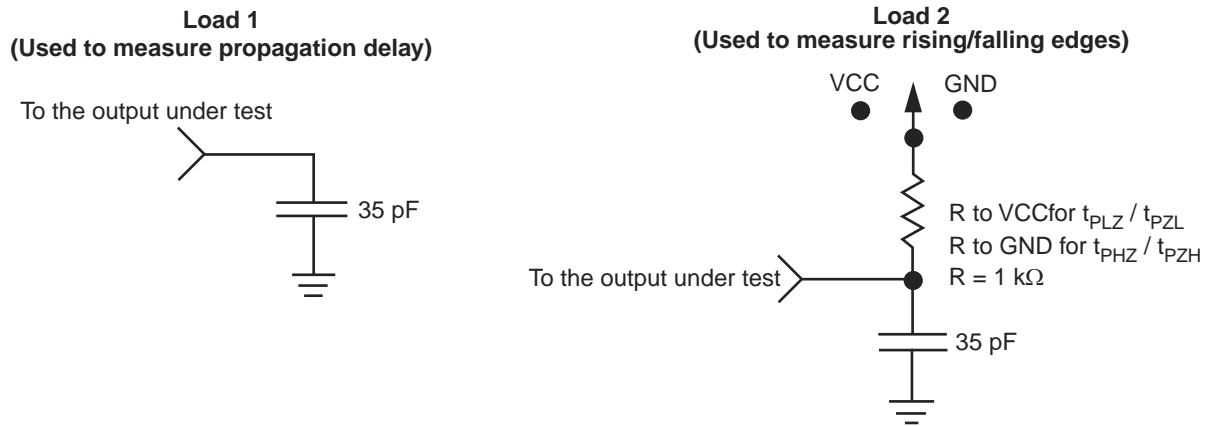
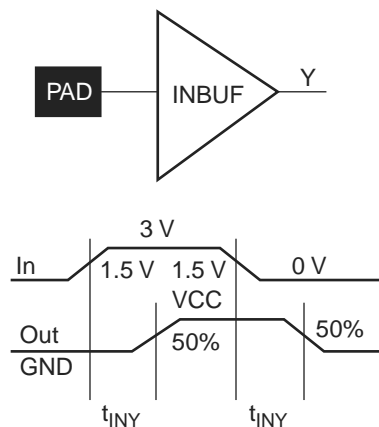
EQ 4

Where:

C<sub>EQ</sub> is the equivalent capacitance expressed in pF.

VCC is the power supply in volts.

F is the switching frequency in MHz.


**Figure 2-11 • Output Buffers**

**Figure 2-12 • AC Test Loads**

**Figure 2-13 • Input Buffer Delays**

## Timing Derating

ACT 3 devices are manufactured in a CMOS process. Therefore, device performance varies according to temperature, voltage, and process variations. Minimum timing parameters reflect maximum operating voltage, minimum operating temperature, and best-case processing. Maximum timing parameters reflect minimum operating voltage, maximum operating temperature, and worst-case processing.

**Table 2-15 • Timing Derating Factor (Temperature and Voltage)**

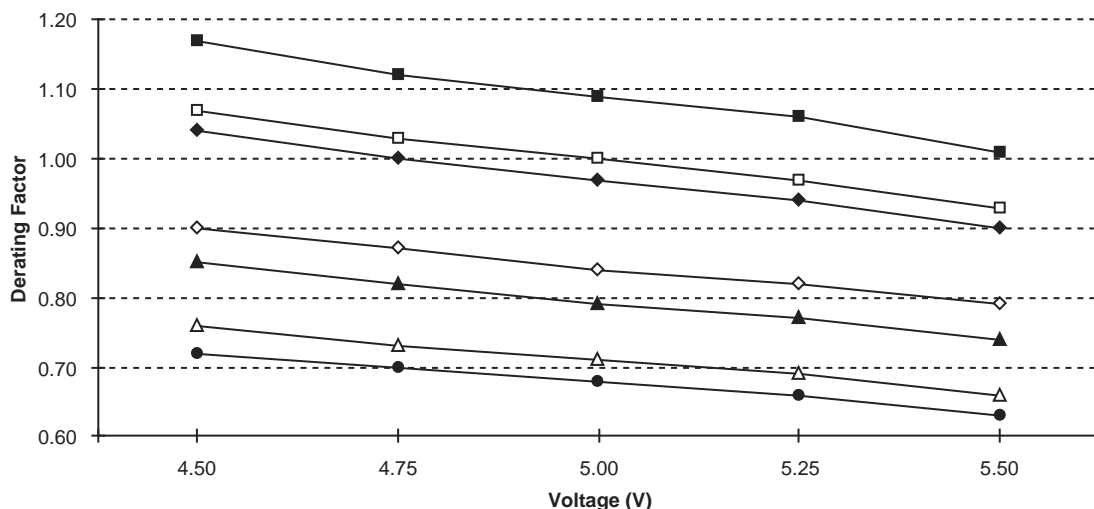
(Commercial Minimum/Maximum Specification) x	Industrial		Military	
	Min.	Max.	Min.	Max.
	0.66	1.07	0.63	1.17

**Table 2-16 • Timing Derating Factor for Designs at Typical Temperature ( $T_J = 25^\circ\text{C}$ ) and Voltage (5.0 V)**

(Commercial Maximum Specification) x	0.85
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**Table 2-17 • Temperature and Voltage Derating Factors (normalized to Worst-Case Commercial,  $T_J = 4.75\text{ V}$ ,  $70^\circ\text{C}$ )**

	-55	-40	0	25	70	85	125
<b>4.50</b>	0.72	0.76	0.85	0.90	1.04	1.07	1.117
<b>4.75</b>	0.70	0.73	0.82	0.87	1.00	1.03	1.12
<b>5.00</b>	0.68	0.71	0.79	0.84	0.97	1.00	1.09
<b>5.25</b>	0.66	0.69	0.77	0.82	0.94	0.97	1.06
<b>5.50</b>	0.63	0.66	0.74	0.79	0.90	0.93	1.01



Note: This derating factor applies to all routing and propagation delays.

**Figure 2-18 • Junction Temperature and Voltage Derating Curves (normalized to Worst-Case Commercial,  $T_J = 4.75\text{ V}$ ,  $70^\circ\text{C}$ )**

## A1415A, A14V15A Timing Characteristics (continued)

**Table 2-19 • A1415A, A14V15A Worst-Case Commercial Conditions, VCC = 4.75 V, T<sub>J</sub> = 70°C**

I/O Module Input Propagation Delays		–3 Speed <sup>1</sup>		–2 Speed <sup>1</sup>		–1 Speed		Std. Speed		3.3 V Speed <sup>2</sup>		Units
Parameter/Description		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t <sub>INY</sub>	Input Data Pad to Y		2.8		3.2		3.6		4.2		5.5	ns
t <sub>ICKY</sub>	Input Reg IOCLK Pad to Y		4.7		5.3		6.0		7.0		9.2	ns
t <sub>OCKY</sub>	Output Reg IOCLK Pad to Y		4.7		5.3		6.0		7.0		9.2	ns
t <sub>ICLRY</sub>	Input Asynchronous Clear to Y		4.7		5.3		6.0		7.0		9.2	ns
t <sub>OCLRY</sub>	Output Asynchronous Clear to Y		4.7		5.3		6.0		7.0		9.2	ns
<b>Predicted Input Routing Delays<sup>2</sup></b>												
t <sub>RD1</sub>	FO = 1 Routing Delay		0.9		1.0		1.1		1.3		1.7	ns
t <sub>RD2</sub>	FO = 2 Routing Delay		1.2		1.4		1.6		1.8		2.4	ns
t <sub>RD3</sub>	FO = 3 Routing Delay		1.4		1.6		1.8		2.1		2.8	ns
t <sub>RD4</sub>	FO = 4 Routing Delay		1.7		1.9		2.2		2.5		3.3	ns
t <sub>RD8</sub>	FO = 8 Routing Delay		2.8		3.2		3.6		4.2		5.5	ns
<b>I/O Module Sequential Timing (wrt IOCLK pad)</b>												
t <sub>INH</sub>	Input F-F Data Hold	0.0		0.0		0.0		0.0		0.0		ns
t <sub>INSU</sub>	Input F-F Data Setup	2.0		2.3		2.5		3.0		3.0		ns
t <sub>IDEH</sub>	Input Data Enable Hold	0.0		0.0		0.0		0.0		0.0		ns
t <sub>IDESU</sub>	Input Data Enable Setup	5.8		6.5		7.5		8.6		8.6		ns
t <sub>OUTH</sub>	Output F-F Data hold	0.7		0.8		0.9		1.0		1.0		ns
t <sub>OUTSU</sub>	Output F-F Data Setup	0.7		0.8		0.9		1.0		1.0		ns
t <sub>ODEH</sub>	Output Data Enable Hold	0.3		0.4		0.4		0.5		0.5		ns
f <sub>ODESU</sub>	Output Data Enable Setup	1.3		1.5		1.7		2.0		2.0		ns

**Notes:**

- The –2 and –3 speed grades have been discontinued. Please refer to the Product Discontinuation Notices (PDNs) listed below:  
PDN March 2001  
PDN 0104  
PDN 0203  
PDN 0604  
PDN 1004
- Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual worst-case performance. Post-route timing is based on actual routing delay measurements performed on the device prior to shipment.

## A1425A, A14V25A Timing Characteristics (continued)

**Table 2-23 • A1425A, A14V25A Worst-Case Commercial Conditions, VCC = 4.75 V, T<sub>J</sub> = 70°C**

I/O Module Input Propagation Delays		–3 Speed <sup>1</sup>		–2 Speed <sup>1</sup>		–1 Speed		Std. Speed		3.3 V Speed <sup>1</sup>		Units
Parameter/Description		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t <sub>INY</sub>	Input Data Pad to Y		2.8		3.2		3.6		4.2		5.5	ns
t <sub>ICKY</sub>	Input Reg IOCLK Pad to Y		4.7		5.3		6.0		7.0		9.2	ns
t <sub>OCKY</sub>	Output Reg IOCLK Pad to Y		4.7		5.3		6.0		7.0		9.2	ns
t <sub>ICLRY</sub>	Input Asynchronous Clear to Y		4.7		5.3		6.0		7.0		9.2	ns
t <sub>OCLRY</sub>	Output Asynchronous Clear to Y		4.7		5.3		6.0		7.0		9.2	ns
<b>Predicted Input Routing Delays<sup>2</sup></b>												
t <sub>RD1</sub>	FO = 1 Routing Delay		0.9		1.0		1.1		1.3		1.7	ns
t <sub>RD2</sub>	FO = 2 Routing Delay		1.2		1.4		1.6		1.8		2.4	ns
t <sub>RD3</sub>	FO = 3 Routing Delay		1.4		1.6		1.8		2.1		2.8	ns
t <sub>RD4</sub>	FO = 4 Routing Delay		1.7		1.9		2.2		2.5		3.3	ns
t <sub>RD8</sub>	FO = 8 Routing Delay		2.8		3.2		3.6		4.2		5.5	ns
<b>I/O Module Sequential Timing (wrt IOCLK pad)</b>												
t <sub>INH</sub>	Input F-F Data Hold	0.0		0.0		0.0		0.0		0.0		ns
t <sub>INSU</sub>	Input F-F Data Setup	1.8		2.0		2.3		2.7		3.0		ns
t <sub>IDEH</sub>	Input Data Enable Hold	0.0		0.0		0.0		0.0		0.0		ns
t <sub>IDESU</sub>	Input Data Enable Setup	5.8		6.5		7.5		8.6		8.6		ns
t <sub>OUTH</sub>	Output F-F Data hold	0.7		0.8		0.9		1.0		1.0		ns
t <sub>OUTSU</sub>	Output F-F Data Setup	0.7		0.8		0.9		1.0		1.0		ns
t <sub>ODEH</sub>	Output Data Enable Hold	0.3		0.4		0.4		0.5		0.5		ns
f <sub>ODESU</sub>	Output Data Enable Setup	1.3		1.5		1.7		2.0		2.0		ns

Notes: \*

1. The –2 and –3 speed grades have been discontinued. Refer to PDN 0104, PDN 0203, PDN 0604, and PDN 1004 at <http://www.microsemi.com/soc/support/notifications/default.aspx#pdn>.
2. Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual worst-case performance. Post-route timing is based on actual routing delay measurements performed on the device prior to shipment.



## A1425A, A14V25A Timing Characteristics (continued)

**Table 2-25 • A1425A, A14V25A Worst-Case Commercial Conditions, VCC = 4.75 V, T<sub>J</sub> = 70°C**

Dedicated (hardwired) I/O Clock Network		–3 Speed <sup>1</sup>		–2 Speed <sup>1</sup>		–1 Speed		Std. Speed		3.3 V Speed <sup>1</sup>		Units
Parameter/Description		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t <sub>ILOCKH</sub>	Input Low to High (pad to I/O module input)		2.0		2.3		2.6		3.0		3.5	ns
t <sub>IOPWH</sub>	Minimum Pulse Width High	1.9		2.4		3.3		3.8		4.8		ns
t <sub>IPOWL</sub>	Minimum Pulse Width Low	1.9		2.4		3.3		3.8		4.8		ns
t <sub>IOSAPW</sub>	Minimum Asynchronous Pulse Width	1.9		2.4		3.3		3.8		4.8		ns
t <sub>ILOCKSW</sub>	Maximum Skew		0.4		0.4		0.4		0.4		0.4	ns
t <sub>IOP</sub>	Minimum Period	4.0		5.0		6.8		8.0		10.0		ns
f <sub>IOMAX</sub>	Maximum Frequency		250		200		150		125		100	MHz
<b>Dedicated (hardwired) Array Clock</b>												
t <sub>HCKH</sub>	Input Low to High (pad to S-module input)		3.0		3.4		3.9		4.5		5.5	ns
t <sub>HCKL</sub>	Input High to Low (pad to S-module input)		3.0		3.4		3.9		4.5		5.5	ns
t <sub>HPWH</sub>	Minimum Pulse Width High	1.9		2.4		3.3		3.8		4.8		ns
t <sub>HPWL</sub>	Minimum Pulse Width Low	1.9		2.4		3.3		3.8		4.8		ns
t <sub>HCKSW</sub>	Delta High to Low, Low Slew		0.3		0.3		0.3		0.3		0.3	ns
t <sub>HP</sub>	Minimum Period	4.0		5.0		6.8		8.0		10.0		ns
f <sub>HMAX</sub>	Maximum Frequency		250		200		150		125		100	MHz
<b>Routed Array Clock Networks</b>												
t <sub>RCKH</sub>	Input Low to High (FO = 64)		3.7		4.1		4.7		5.5		9.0	ns
t <sub>RCKL</sub>	Input High to Low (FO = 64)		4.0		4.5		5.1		6.0		9.0	ns
t <sub>RPWH</sub>	Min. Pulse Width High (FO = 64)	3.3		3.8		4.2		4.9		6.5		ns
t <sub>RPWL</sub>	Min. Pulse Width Low (FO = 64)	3.3		3.8		4.2		4.9		6.5		ns
t <sub>RCKSW</sub>	Maximum Skew (FO = 128)		0.7		0.8		0.9		1.0		1.0	ns
t <sub>RP</sub>	Minimum Period (FO = 64)	6.8		8.0		8.7		10.0		13.4		ns
f <sub>RMAX</sub>	Maximum Frequency (FO = 64)		150		125		115		100		75	MHz
<b>Clock-to-Clock Skews</b>												
t <sub>IOHCKSW</sub>	I/O Clock to H-Clock Skew	0.0	1.7	0.0	1.8	0.0	2.0	0.0	2.2	0.0	3.0	ns
t <sub>IORCKSW</sub>	I/O Clock to R-Clock Skew (FO = 64) (FO = 80)	0.0	1.0	0.0	1.0	0.0	1.0	0.0	1.0	0.0	3.0	ns
		0.0	3.0	0.0	3.0	0.0	3.0	0.0	3.0	0.0	3.0	
t <sub>HRCKSW</sub>	H-Clock to R-Clock Skew (FO = 64) (FO = 80)	0.0	1.0	0.0	1.0	0.0	1.0	0.0	1.0	0.0	1.0	ns
		0.0	3.0	0.0	3.0	0.0	3.0	0.0	3.0	0.0	3.0	

**Notes:**

1. The –2 and –3 speed grades have been discontinued. Refer to PDN 0104, PDN 0203, PDN 0604, and PDN 1004 at <http://www.microsemi.com/soc/support/notifications/default.aspx#pdn>.
2. Delays based on 35 pF loading.

## A1440A, A14V40A Timing Characteristics (continued)

Table 2-28 • A1440A, A14V40A Worst-Case Commercial Conditions, VCC = 4.75 V, T<sub>J</sub> = 70°C

I/O Module – TTL Output Timing <sup>1</sup>		–3 Speed <sup>2</sup>		–2 Speed <sup>2</sup>		–1 Speed		Std. Speed		3.3 V Speed <sup>1</sup>		Units
Parameter/Description		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t <sub>DHS</sub>	Data to Pad, High Slew		5.0		5.6		6.4		7.5		9.8	ns
t <sub>DLS</sub>	Data to Pad, Low Slew		8.0		9.0		10.2		12.0		15.6	ns
t <sub>ENZHS</sub>	Enable to Pad, Z to H/L, High Slew		4.0		4.5		5.1		6.0		7.8	ns
t <sub>ENZLS</sub>	Enable to Pad, Z to H/L, Low Slew		7.4		8.3		9.4		11.0		14.3	ns
t <sub>ENHSZ</sub>	Enable to Pad, H/L to Z, High Slew		7.4		8.3		9.4		11.0		14.3	ns
t <sub>ENLSZ</sub>	Enable to Pad, H/L to Z, Low Slew		7.4		8.3		9.4		11.0		14.3	ns
t <sub>CKHS</sub>	IOCLK Pad to Pad H/L, High Slew		8.5		8.5		9.5		11.0		14.3	ns
t <sub>CKLS</sub>	IOCLK Pad to Pad H/L, Low Slew		11.3		11.3		13.5		15.0		19.5	ns
d <sub>TLHHS</sub>	Delta Low to High, High Slew		0.02		0.02		0.03		0.03		0.04	ns/pF
d <sub>TLHLS</sub>	Delta Low to High, Low Slew		0.05		0.05		0.06		0.07		0.09	ns/pF
d <sub>THLHS</sub>	Delta High to Low, High Slew		0.04		0.04		0.04		0.05		0.07	ns/pF
d <sub>THLLS</sub>	Delta High to Low, Low Slew		0.05		0.05		0.06		0.07		0.09	ns/pF
I/O Module – CMOS Output Timing <sup>1</sup>												
t <sub>DHS</sub>	Data to Pad, High Slew		6.2		7.0		7.9		9.3		12.1	ns
t <sub>DLS</sub>	Data to Pad, Low Slew		11.7		13.1		14.9		17.5		22.8	ns
t <sub>ENZHS</sub>	Enable to Pad, Z to H/L, High Slew		5.2		5.9		6.6		7.8		10.1	ns
t <sub>ENZLS</sub>	Enable to Pad, Z to H/L, Low Slew		8.9		10.0		11.3		13.3		17.3	ns
t <sub>ENHSZ</sub>	Enable to Pad, H/L to Z, High Slew		7.4		8.3		9.4		11.0		14.3	ns
t <sub>ENLSZ</sub>	Enable to Pad, H/L to Z, Low Slew		7.4		8.3		9.4		11.0		14.3	ns
t <sub>CKHS</sub>	IOCLK Pad to Pad H/L, High Slew		9.0		9.0		10.1		11.8		14.3	ns
t <sub>CKLS</sub>	IOCLK Pad to Pad H/L, Low Slew		13.0		13.0		15.6		17.3		22.5	ns
d <sub>TLHHS</sub>	Delta Low to High, High Slew		0.04		0.04		0.05		0.06		0.08	ns/pF
d <sub>TLHLS</sub>	Delta Low to High, Low Slew		0.07		0.08		0.09		0.11		0.14	ns/pF
d <sub>THLHS</sub>	Delta High to Low, High Slew		0.03		0.03		0.03		0.04		0.05	ns/pF
d <sub>THLLS</sub>	Delta High to Low, Low Slew		0.04		0.04		0.04		0.05		0.07	ns/pF

**Notes:**

1. Delays based on 35 pF loading.
2. The –2 and –3 speed grades have been discontinued. Refer to PDN 0104, PDN 0203, PDN 0604, and PDN 1004 at <http://www.microsemi.com/soc/support/notifications/default.aspx#pdn>.

## A1460A, A14V60A Timing Characteristics

**Table 2-30 • A1460A, A14V60A Worst-Case Commercial Conditions, VCC = 4.75 V, T<sub>J</sub> = 70°C<sup>1</sup>**

Logic Module Propagation Delays <sup>2</sup>		–3 Speed <sup>3</sup>		–2 Speed <sup>3</sup>		–1 Speed		Std. Speed		3.3 V Speed <sup>1</sup>		Units
Parameter/Description		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t <sub>PD</sub>	Internal Array Module		2.0		2.3		2.6		3.0		3.9	ns
t <sub>CO</sub>	Sequential Clock to Q		2.0		2.3		2.6		3.0		3.9	ns
t <sub>CLR</sub>	Asynchronous Clear to Q		2.0		2.3		2.6		3.0		3.9	ns
<b>Predicted Routing Delays<sup>4</sup></b>												
t <sub>RD1</sub>	FO = 1 Routing Delay		0.9		1.0		1.1		1.3		1.7	ns
t <sub>RD2</sub>	FO = 2 Routing Delay		1.2		1.4		1.6		1.8		2.4	ns
t <sub>RD3</sub>	FO = 3 Routing Delay		1.4		1.6		1.8		2.1		2.8	ns
t <sub>RD4</sub>	FO = 4 Routing Delay		1.7		1.9		2.2		2.5		3.3	ns
t <sub>RD8</sub>	FO = 8 Routing Delay		2.8		3.2		3.6		4.2		5.5	ns
<b>Logic Module Sequential Timing</b>												
t <sub>SUD</sub>	Flip-Flop Data Input Setup	0.5		0.6		0.7		0.8		0.8		ns
t <sub>HD</sub>	Flip-Flop Data Input Hold	0.0		0.0		0.0		0.0		0.0		ns
t <sub>SUD</sub>	Latch Data Input Setup	0.5		0.6		0.7		0.8		0.8		ns
t <sub>HD</sub>	Latch Data Input Hold	0.0		0.0		0.0		0.0		0.0		ns
t <sub>WASYN</sub>	Asynchronous Pulse Width	2.4		3.2		3.8		4.8		6.5		ns
t <sub>WCLKA</sub>	Flip-Flop Clock Pulse Width	2.4		3.2		3.8		4.8		6.5		ns
t <sub>A</sub>	Flip-Flop Clock Input Period	5.0		6.8		8.0		10.0		13.4		ns
f <sub>MAX</sub>	Flip-Flop Clock Frequency		200		150		125		100		75	MHz

**Notes:**

1. VCC = 3.0 V for 3.3 V specifications.
2. For dual-module macros, use t<sub>PD</sub> + t<sub>RD1</sub> + t<sub>PDn</sub> + t<sub>CO</sub> + t<sub>RD1</sub> + t<sub>PDn</sub> or t<sub>PD1</sub> + t<sub>RD1</sub> + t<sub>SUD</sub>, whichever is appropriate.
3. The –2 and –3 speed grades have been discontinued. Refer to PDN 0104, PDN 0203, PDN 0604, and PDN 1004 at <http://www.microsemi.com/soc/support/notifications/default.aspx#pdn>.
4. Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual worst-case performance. Post-route timing is based on actual routing delay measurements performed on the device prior to shipment.

## A1460A, A14V60A Timing Characteristics (continued)

**Table 2-33 • A1460A, A14V60A Worst-Case Commercial Conditions, VCC = 4.75 V, T<sub>J</sub> = 70°C**

Dedicated (hardwired) I/O Clock Network		–3 Speed <sup>1</sup>		–2 Speed <sup>1</sup>		–1 Speed		Std. Speed		3.3 V Speed <sup>1</sup>		Units
Parameter/Description		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t <sub>ILOCKH</sub>	Input Low to High (pad to I/O module input)		2.3		2.6		3.0		3.5		4.5	ns
t <sub>IOPWH</sub>	Minimum Pulse Width High	2.4		3.2		3.8		4.8		6.5		ns
t <sub>IPOWL</sub>	Minimum Pulse Width Low	2.4		3.2		3.8		4.8		6.5		ns
t <sub>IOSAPW</sub>	Minimum Asynchronous Pulse Width	2.4		3.2		3.8		4.8		6.5		ns
t <sub>ILOCKSW</sub>	Maximum Skew		0.6		0.6		0.6		0.6		0.6	ns
t <sub>IOP</sub>	Minimum Period	5.0		6.8		8.0		10.0		13.4		ns
f <sub>IOMAX</sub>	Maximum Frequency		200		150		125		100		75	MHz
<b>Dedicated (hardwired) Array Clock</b>												
t <sub>HCKH</sub>	Input Low to High (pad to S-module input)		3.7		4.1		4.7		5.5		7.0	ns
t <sub>HCKL</sub>	Input High to Low (pad to S-module input)		3.7		4.1		4.7		5.5		7.0	ns
t <sub>HPWH</sub>	Minimum Pulse Width High	2.4		3.2		3.8		4.8		6.5		ns
t <sub>HPWL</sub>	Minimum Pulse Width Low	2.4		3.2		3.8		4.8		6.5		ns
t <sub>HCKSW</sub>	Delta High to Low, Low Slew		0.6		0.6		0.6		0.6		0.6	ns
t <sub>HP</sub>	Minimum Period	5.0		6.8		8.0		10.0		13.4		ns
f <sub>HMAX</sub>	Maximum Frequency		200		150		125		100		75	MHz
<b>Routed Array Clock Networks</b>												
t <sub>RCKH</sub>	Input Low to High (FO = 64)		6.0		6.8		7.7		9.0		11.8	ns
t <sub>RCKL</sub>	Input High to Low (FO = 64)		6.0		6.8		7.7		9.0		11.8	ns
t <sub>RPWH</sub>	Min. Pulse Width High (FO = 64)	4.1		4.5		5.4		6.1		8.2		ns
t <sub>RPWL</sub>	Min. Pulse Width Low (FO = 64)	4.1		4.5		5.4		6.1		8.2		ns
t <sub>RCKSW</sub>	Maximum Skew (FO = 128)		1.2		1.4		1.6		1.8		1.8	ns
t <sub>RP</sub>	Minimum Period (FO = 64)	8.3		9.3		11.1		12.5		16.7		ns
f <sub>RMAX</sub>	Maximum Frequency (FO = 64)		120		105		90		80		60	MHz
<b>Clock-to-Clock Skews</b>												
t <sub>IOHCKSW</sub>	I/O Clock to H-Clock Skew	0.0	2.6	0.0	2.7	0.0	2.9	0.0	3.0	0.0	3.0	ns
t <sub>IORCKSW</sub>	I/O Clock to R-Clock Skew (FO = 64) (FO = 216)	0.0	1.7	0.0	1.7	0.0	1.7	0.0	1.7	0.0	5.0	ns
		0.0	5.0	0.0	5.0	0.0	5.0	0.0	5.0	0.0	5.0	
t <sub>HRCKSW</sub>	H-Clock to R-Clock Skew (FO = 64) (FO = 216)	0.0	1.3	0.0	1.0	0.0	1.0	0.0	1.0	0.0	1.0	ns
		0.0	3.0	0.0	3.0	0.0	3.0	0.0	3.0	0.0	3.0	

**Notes:**

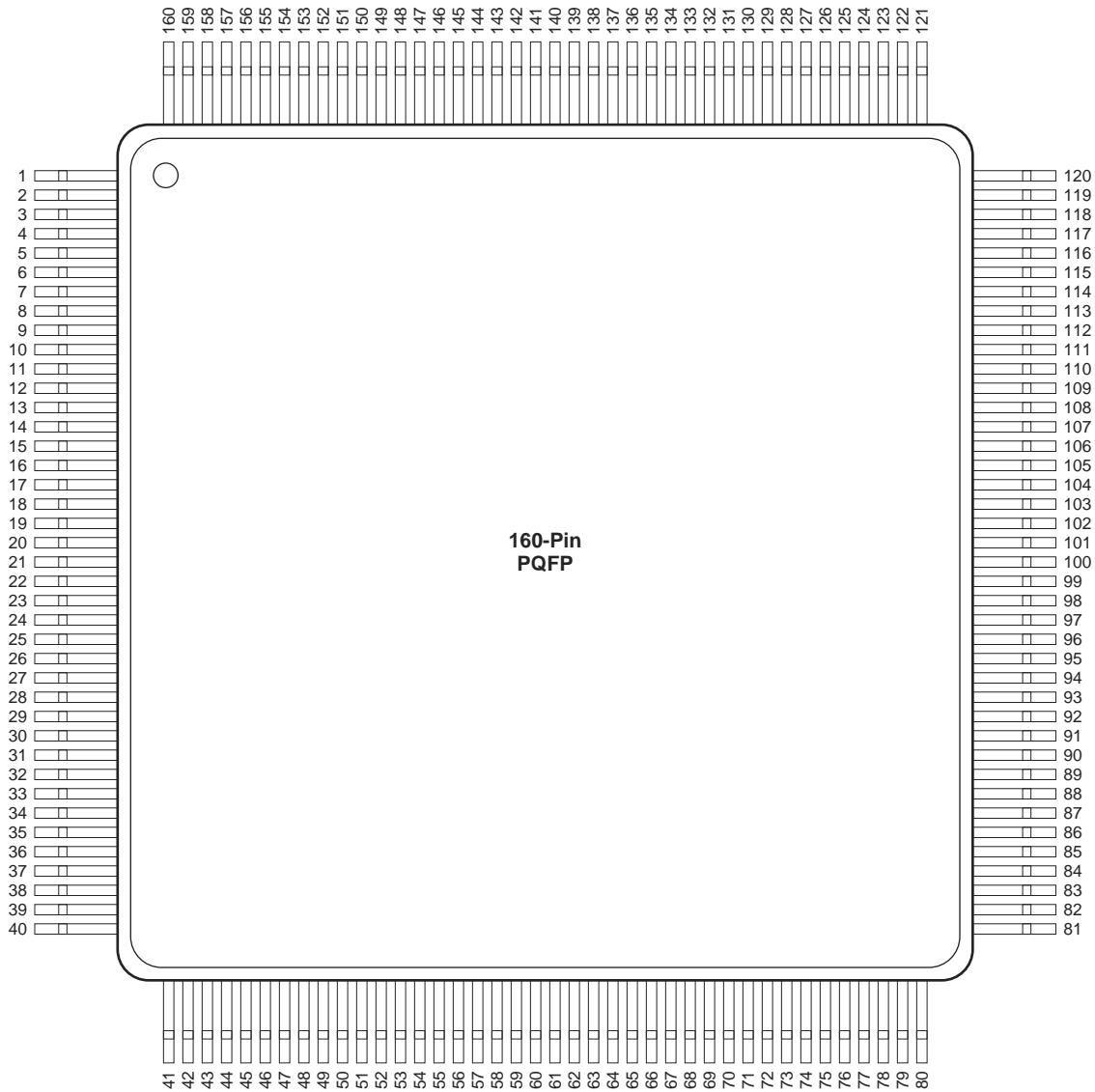
1. The –2 and –3 speed grades have been discontinued. Refer to PDN 0104, PDN 0203, PDN 0604, and PDN 1004 at <http://www.microsemi.com/soc/support/notifications/default.aspx#pdn>.
2. Delays based on 35 pF loading.

PL84			
Pin Number	A1415, A14V15 Function	A1425, A14V25 Function	A1440, A14V40 Function
1	VCC	VCC	VCC
2	GND	GND	GND
3	VCC	VCC	VCC
4	PRA, I/O	PRA, I/O	PRA, I/O
11	DCLK, I/O	DCLK, I/O	DCLK, I/O
12	SDI, I/O	SDI, I/O	SDI, I/O
16	MODE	MODE	MODE
27	GND	GND	GND
28	VCC	VCC	VCC
40	PRB, I/O	PRB, I/O	PRB, I/O
41	VCC	VCC	VCC
42	GND	GND	GND
43	VCC	VCC	VCC
45	HCLK, I/O	HCLK, I/O	HCLK, I/O
52	SDO	SDO	SDO
53	IOPCL, I/O	IOPCL, I/O	IOPCL, I/O
59	VCC	VCC	VCC
60	VCC	VCC	VCC
61	GND	GND	GND
68	VCC	VCC	VCC
69	GND	GND	GND
74	IOCLK, I/O	IOCLK, I/O	IOCLK, I/O
83	CLKA, I/O	CLKA, I/O	CLKA, I/O
84	CLKB, I/O	CLKB, I/O	CLKB, I/O

*Notes:*

1. All unlisted pin numbers are user I/Os.
2. NC denotes no connection.
3. MODE should be terminated to GND through a 10K resistor to enable Actionprobe usage; otherwise it can be terminated directly to GND.

## PQ160



*Note:* This is the top view of the package

### Note

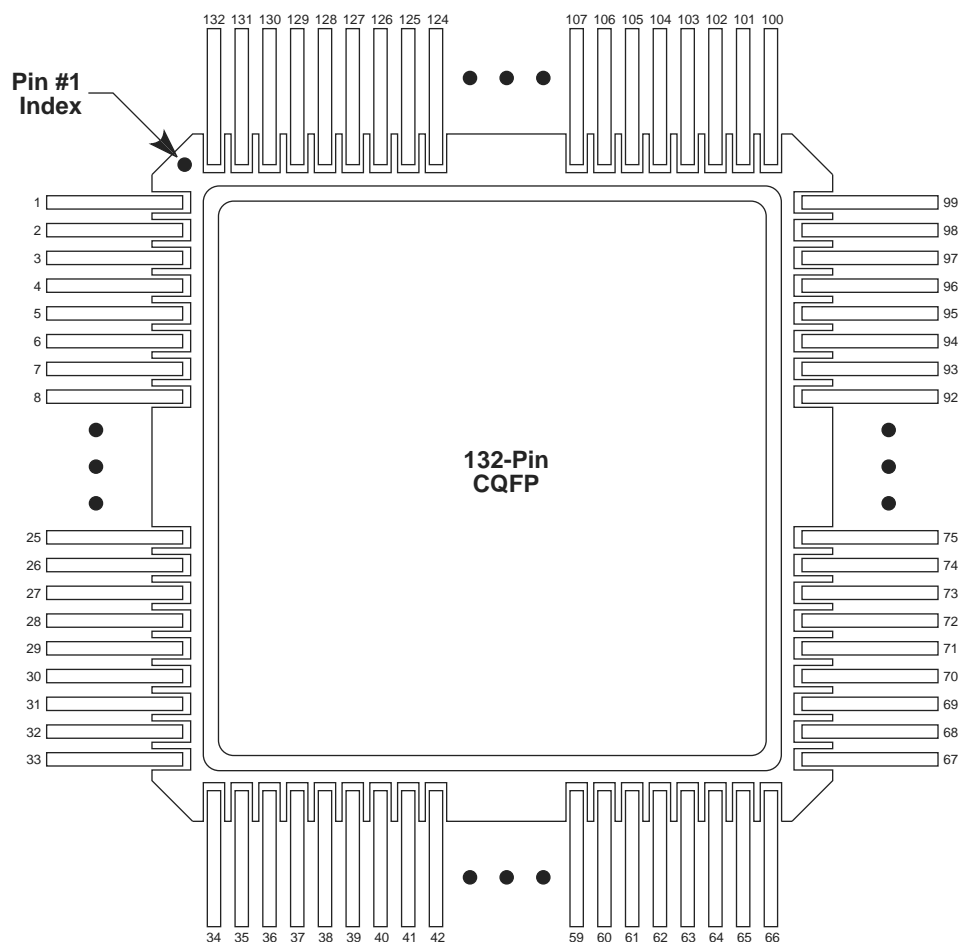
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PQ160			
Pin Number	A1425, A14V25 Function	A1440, A14V40 Function	A1460, A14V60 Function
92	NC	I/O	I/O
93	NC	I/O	I/O
98	GND	GND	GND
99	VCC	VCC	VCC
100	NC	I/O	I/O
103	GND	GND	GND
107	NC	I/O	I/O
109	NC	I/O	I/O
110	VCC	VCC	VCC
111	GND	GND	GND
112	VCC	VCC	VCC
113	NC	I/O	I/O
119	NC	I/O	I/O
120	IOCLK, I/O	IOCLK, I/O	IOCLK, I/O
121	GND	GND	GND
124	NC	I/O	I/O
127	NC	I/O	I/O
136	CLKA, I/O	CLKA, I/O	CLKA, I/O
137	CLKB, I/O	CLKB, I/O	CLKB, I/O
138	VCC	VCC	VCC
139	GND	GND	GND
140	VCC	VCC	VCC
141	GND	GND	GND
142	PRA, I/O	PRA, I/O	PRA, I/O
143	NC	I/O	I/O
145	NC	I/O	I/O
147	NC	I/O	I/O
149	NC	I/O	I/O
151	NC	I/O	I/O
153	NC	I/O	I/O
154	VCC	VCC	VCC
160	DCLK, I/O	DCLK, I/O	DCLK, I/O

**Notes:**

1. All unlisted pin numbers are user I/Os.
2. NC denotes no connection.
3. MODE should be terminated to GND through a 10K resistor to enable Actionprobe usage; otherwise it can be terminated directly to GND.

## CQ132



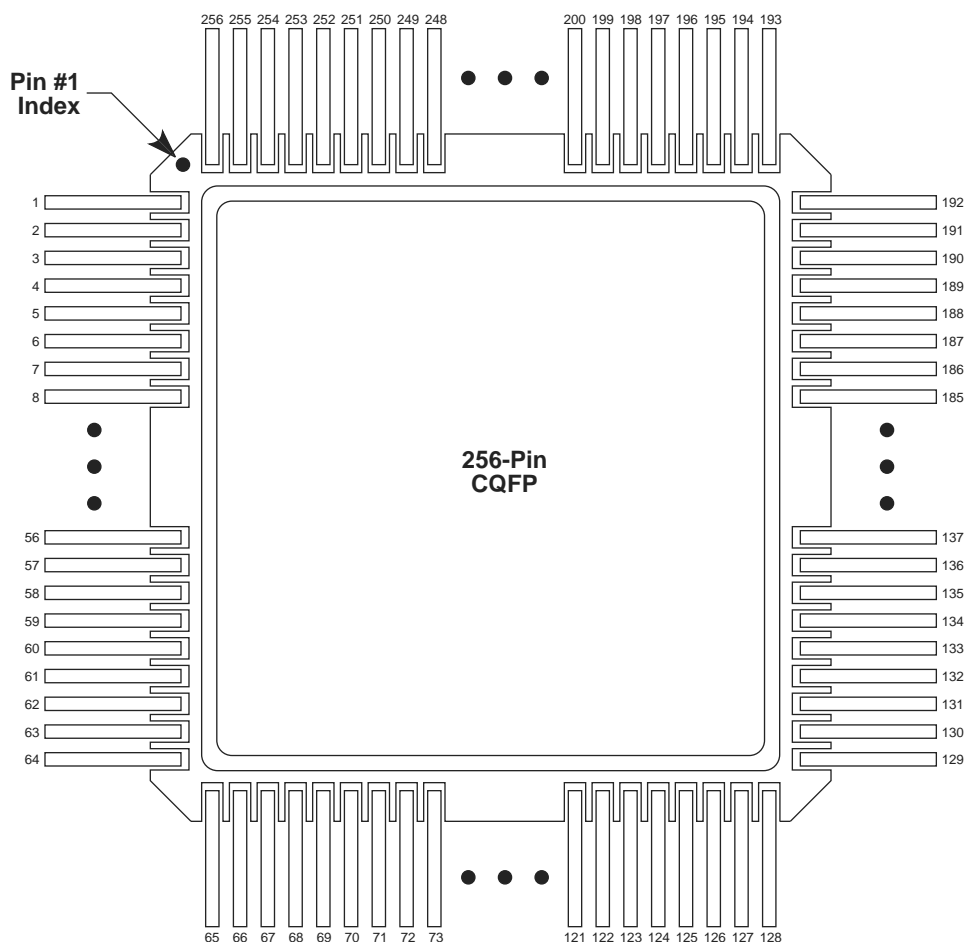
*Note:* This is the top view

### Note

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## CQ256

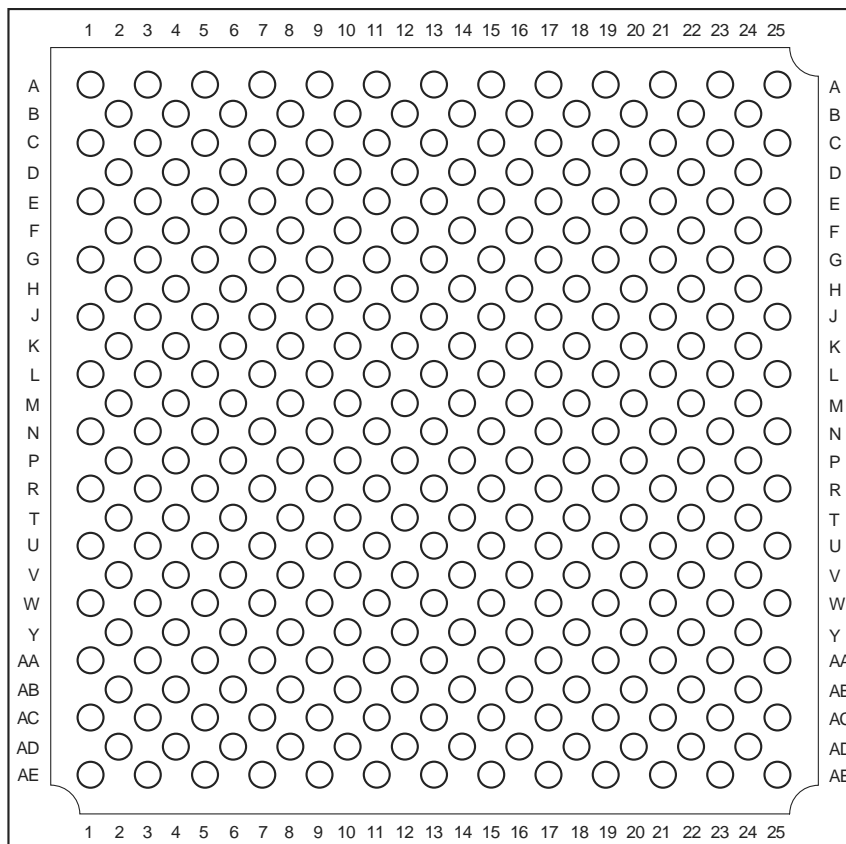


*Note: This is the top view.*

### Note

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## BG313



*Note: This is the top view.*

### Note

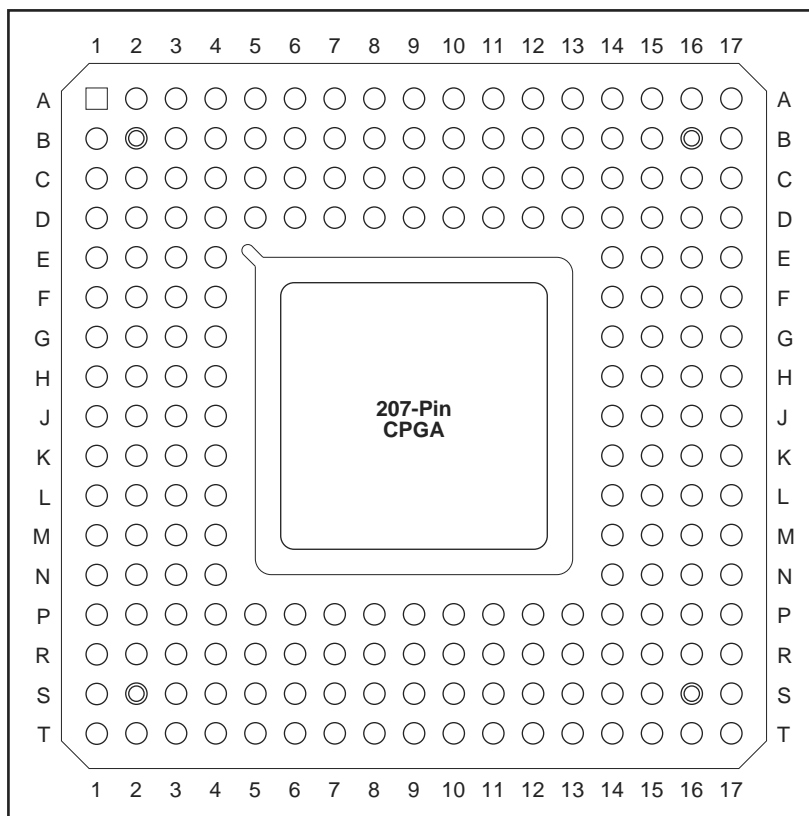
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PG133	
A1425 Function	Location
CLKA or I/O	D7
CLKB or I/O	B6
DCLK or I/O	D4
GND	A2, C3, C7, C11, C12, F10, G3, G11, L3, L7, L11, M3, N12
HCLK or I/O	K7
IOCLK or I/O	C10
IOPCL or I/O	L10
MODE	E3
NC	A1, A7, A13, G1, G13, N1, N7, N13
PRA or I/O	A6
PRB or I/O	L6
SDI or I/O	C2
SDO	M11
VCC	B2, B7, B12, E11, G2, G12, J2, J12, M2, M7, M12

*Notes:*

1. All unlisted pin numbers are user I/Os.
2. NC denotes no connection.
3. MODE should be terminated to GND through a 10K resistor to enable Actionprobe usage; otherwise it can be terminated directly to GND.
4. The PG133 package has been discontinued.

## PG207



*Note: This is the top view.*

### Note

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