# Microsemi Corporation - A1425A-PQG160I Datasheet



**Welcome to E-XFL.COM**

### Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

### Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications,

| Details | |
|---|---|
| Product Status | Obsolete |
| Number of LABs/CLBs | 310 |
| Number of Logic Elements/Cells | - |
| Total RAM Bits | - |
| Number of I/O | 100 |
| Number of Gates | 2500 |
| Voltage - Supply | 4.5V ~ 5.5V |
| Mounting Type | Surface Mount |
| Operating Temperature | -40°C ~ 85°C (TA) |
| Package / Case | 160-BQFP |
| Supplier Device Package | 160-PQFP (28x28) |
| Purchase URL | https://www.e-xfl.com/product-detail/microsemi/a1425a-pqg160i |

# Product Plan

| Device/Package | Speed Grade[1] | | | | Application[1] | | | |
|---|---|---|---|---|---|---|---|---|
| | Std. | –1 | –2 | –3 | C | I | M | B |
| **A1415A Device** | | | | | | | | |
| 84-Pin Plastic Leaded Chip Carrier (PLCC) | ✓ | ✓ | D | D | ✓ | ✓ | ✓ | – |
| 100-Pin Plastic Quad Flatpack (PQFP) | ✓ | ✓ | D | D | ✓ | ✓ | ✓ | – |
| 100-Pin Very Thin Quad Flatpack (VQFP) | ✓ | ✓ | D | D | ✓ | ✓ | ✓ | – |
| 100-Pin Ceramic Pin Grid Array (CPGA) | D | D | D | D | D | – | – | – |
| **A14V15A Device** | | | | | | | | |
| 84-Pin Plastic Leaded Chip Carrier (PLCC) | ✓ | – | – | – | ✓ | – | – | – |
| 100-Pin Very Thin Quad Flatpack (VQFP) | ✓ | – | – | – | ✓ | – | – | – |
| **A1425A Device** | | | | | | | | |
| 84-Pin Plastic Leaded Chip Carrier (PLCC) | ✓ | ✓ | D | D | ✓ | ✓ | | |
| 100-Pin Plastic Quad Flatpack (PQFP) | ✓ | ✓ | D | D | ✓ | ✓ | – | – |
| 100-Pin Very Thin Quad Flatpack (VQFP) | ✓ | ✓ | D | D | ✓ | ✓ | – | – |
| 132-Pin Ceramic Quad Flatpack (CQFP) | ✓ | ✓ | – | – | ✓ | – | ✓ | ✓ |
| 133-Pin Ceramic Pin Grid Array (CPGA) | D | D | D | D | D | – | D | D |
| 160-Pin Plastic Quad Flatpack (PQFP) | ✓ | ✓ | D | D | ✓ | ✓ | – | – |
| **A14V25A Device** | | | | | | | | |
| 84-Pin Plastic Leaded Chip Carrier (PLCC) | ✓ | – | – | – | ✓ | – | – | – |
| 100-Pin Very Thin Quad Flatpack (VQFP) | ✓ | – | – | – | ✓ | – | – | – |
| 160-Pin Plastic Quad Flatpack (PQFP) | ✓ | – | – | – | ✓ | – | – | – |
| **A1440A Device** | | | | | | | | |
| 84-Pin Plastic Leaded Chip Carrier (PLCC) | ✓ | ✓ | D | D | ✓ | ✓ | – | – |
| 100-Pin Very Thin Quad Flatpack (VQFP) | ✓ | ✓ | D | D | ✓ | ✓ | – | – |
| 160-Pin Plastic Quad Flatpack (PQFP) | ✓ | ✓ | D | D | ✓ | ✓ | – | – |
| 175-Pin Ceramic Pin Grid Array (CPGA) | D | D | D | D | D | – | – | – |
| 176-Pin Thin Quad Flatpack (TQFP) | ✓ | ✓ | D | D | ✓ | ✓ | – | – |

*Notes:*
1. *Applications:*
   *C = Commercial*
   *I = Industrial*
   *M = Military*
2. *Commercial only*

*Availability:*
*✓ = Available*
*P = Planned*
*– = Not planned*
*D = Discontinued*

*Speed Grade:*
*–1 = Approx. 15% faster than Std.*
*–2 = Approx. 25% faster than Std.*
*–3 = Approx. 35% faster than Std.*
*(–2 and –3 speed grades have been discontinued.)*

## Dedicated Clocks

Dedicated clock networks support high performance by providing sub-nanosecond skew and guaranteed performance. Dedicated clock networks contain no programming elements in the path from the I/O Pad Driver to the input of S-modules or I/O modules. There are two dedicated clock networks: one for the array registers (HCLK), and one for the I/O registers (IOCLK). The clock networks are accessed by special I/Os.

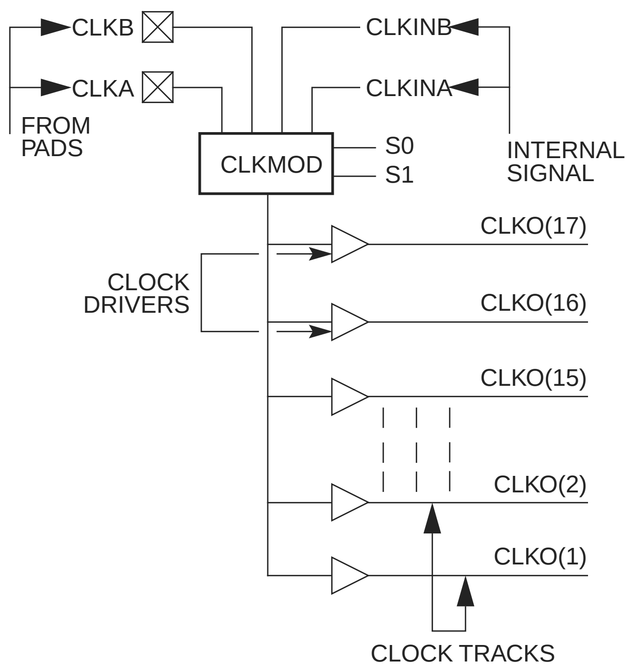



***Figure 2-6 •*** **Clock Networks**

The routed clock networks are referred to as CLK0 and CLK1. Each network is connected to a clock module (CLKMOD) that selects the source of the clock signal and may be driven as follows (Figure 2-6):

- Externally from the CLKA pad
- Externally from the CLKB pad
- Internally from the CLKINA input
- Internally from the CLKINB input

The clock modules are located in the top row of I/O modules. Clock drivers and a dedicated horizontal clock track are located in each horizontal routing channel. The function of the clock module is determined by the selection of clock macros from the macro library. The macro CLKBUF is used to connect one of the two external clock pins to a clock network, and the macro CLKINT is used to connect an internally generated clock signal to a clock network. Since both clock networks are identical, the user does not care whether CLK0 or CLK1 is being used. Routed clocks can also be used to drive high fanout nets like resets, output enables, or data enables. This saves logic modules and results in performance increases in some cases.

# Routing Structure

The ACT 3 architecture uses vertical and horizontal routing tracks to connect the various logic and I/O modules. These routing tracks are metal interconnects that may either be of continuous length or broken into segments. Segments can be joined together at the ends using antifuses to increase their lengths up to the full length of the track.

## Horizontal Routing

Horizontal channels are located between the rows of modules and are composed of several routing tracks. The horizontal routing tracks within the channel are divided into one or more segments. The minimum horizontal segment length is the width of a module-pair, and the maximum horizontal segment length is the full length of the channel. Any segment that spans more than one-third the row length is considered a long horizontal segment. A typical channel is shown in Figure 2-7. Undedicated horizontal routing tracks are used to route signal nets. Dedicated routing tracks are used for the global clock networks and for power and ground tie-off tracks.

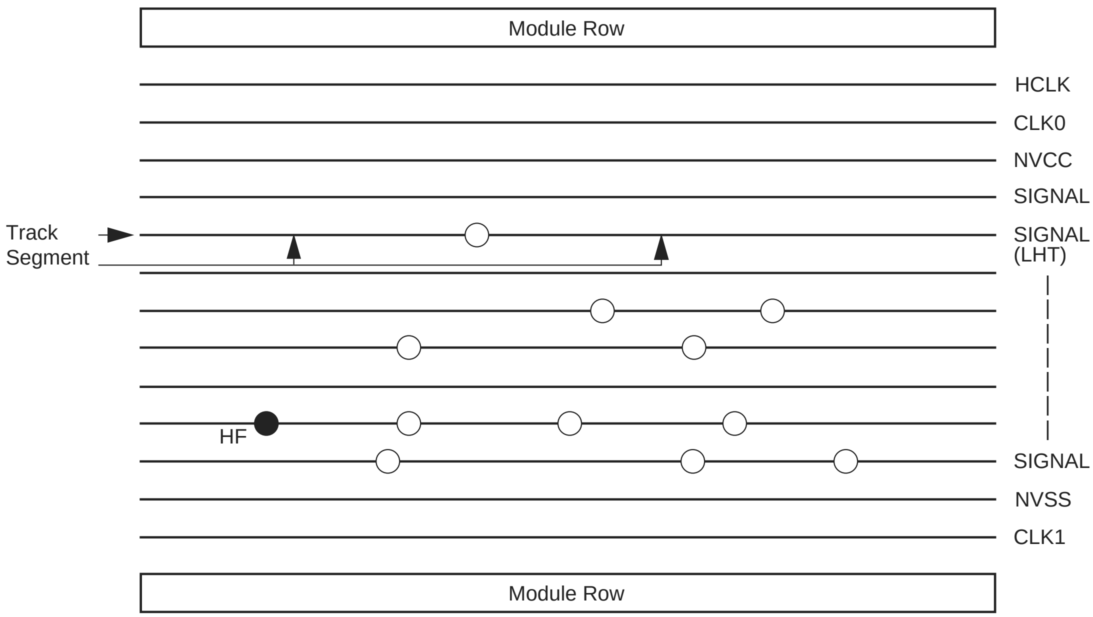



***Figure 2-7 •*** **Horizontal Routing Tracks and Segments**

## Vertical Routing

Other tracks run vertically through the modules. Vertical tracks are of three types: input, output, and long. Vertical tracks are also divided into one or more segments. Each segment in an input track is dedicated to the input of a particular module. Each segment in an output track is dedicated to the output of a particular module. Long segments are uncommitted and can be assigned during routing. Each output segment spans four channels (two above and two below), except near the top and bottom of the array where edge effects occur. LVTs contain either one or two segments. An example of vertical routing tracks and segments is shown in Figure 2-8.

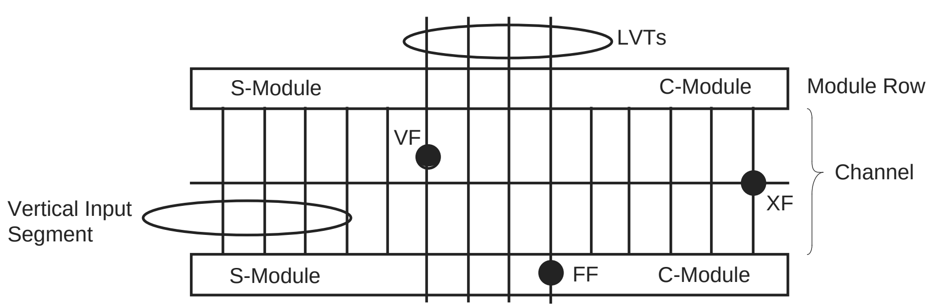



***Figure 2-8 •*** **Vertical Routing Tracks and Segments**

# Package Thermal Characteristics

The device junction to case thermal characteristic is θjc, and the junction to ambient air characteristic is θja. The thermal characteristics for θja are shown with two different air flow rates.

Maximum junction temperature is 150°C.

A sample calculation of the absolute maximum power dissipation allowed for a CPGA 175-pin package at commercial temperature and still air is as follows:

$$\frac{\text{Max. junction temp. (°C)} - \text{Max. ambient temp. (°C)}}{\theta_{ja}\text{°C/W}} = \frac{150\text{°C} - 70\text{°C}}{25\text{°C/W}} = 3.2\text{ W}$$

*EQ 2*

***Table 2-8* • Package Thermal Characteristics**

| Package Type* | Pin Count | $\theta_{jc}$ | $\theta_{ja}$ Still Air | $\theta_{ja}$ 300 ft./min. | Units |
|---|---|---|---|---|---|
| Ceramic Pin Grid Array | 100 | 20 | 35 | 17 | °C/W |
| | 133 | 20 | 30 | 15 | °C/W |
| | 175 | 20 | 25 | 14 | °C/W |
| | 207 | 20 | 22 | 13 | °C/W |
| | 257 | 20 | 15 | 8 | °C/W |
| Ceramic Quad Flatpack | 132 | 13 | 55 | 30 | °C/W |
| | 196 | 13 | 36 | 24 | °C/W |
| | 256 | 13 | 30 | 18 | °C/W |
| Plastic Quad Flatpack | 100 | 13 | 51 | 40 | °C/W |
| | 160 | 10 | 33 | 26 | °C/W |
| | 208 | 10 | 33 | 26 | °C/W |
| Very Thin Quad Flatpack | 100 | 12 | 43 | 35 | °C/W |
| Thin Quad Flatpack | 176 | 11 | 32 | 25 | °C/W |
| Power Quad Flatpack | 208 | 0.4 | 17 | 13 | °C/W |
| Plastic Leaded Chip Carrier | 84 | 12 | 37 | 28 | °C/W |
| Plastic Ball Grid Array | 225 | 10 | 25 | 19 | °C/W |
| | 313 | 10 | 23 | 17 | °C/W |

*Note: Maximum power dissipation in still air:*
*PQ160 = 2.4 W*
*PQ208 = 2.4 W*
*PQ100 = 1.6 W*
*VQ100 = 1.9 W*
*TQ176 = 2.5 W*
*PL84 = 2.2 W*
*RQ208 = 4.7 W*
*BG225 = 3.2 W*
*BG313 = 3.5 W*

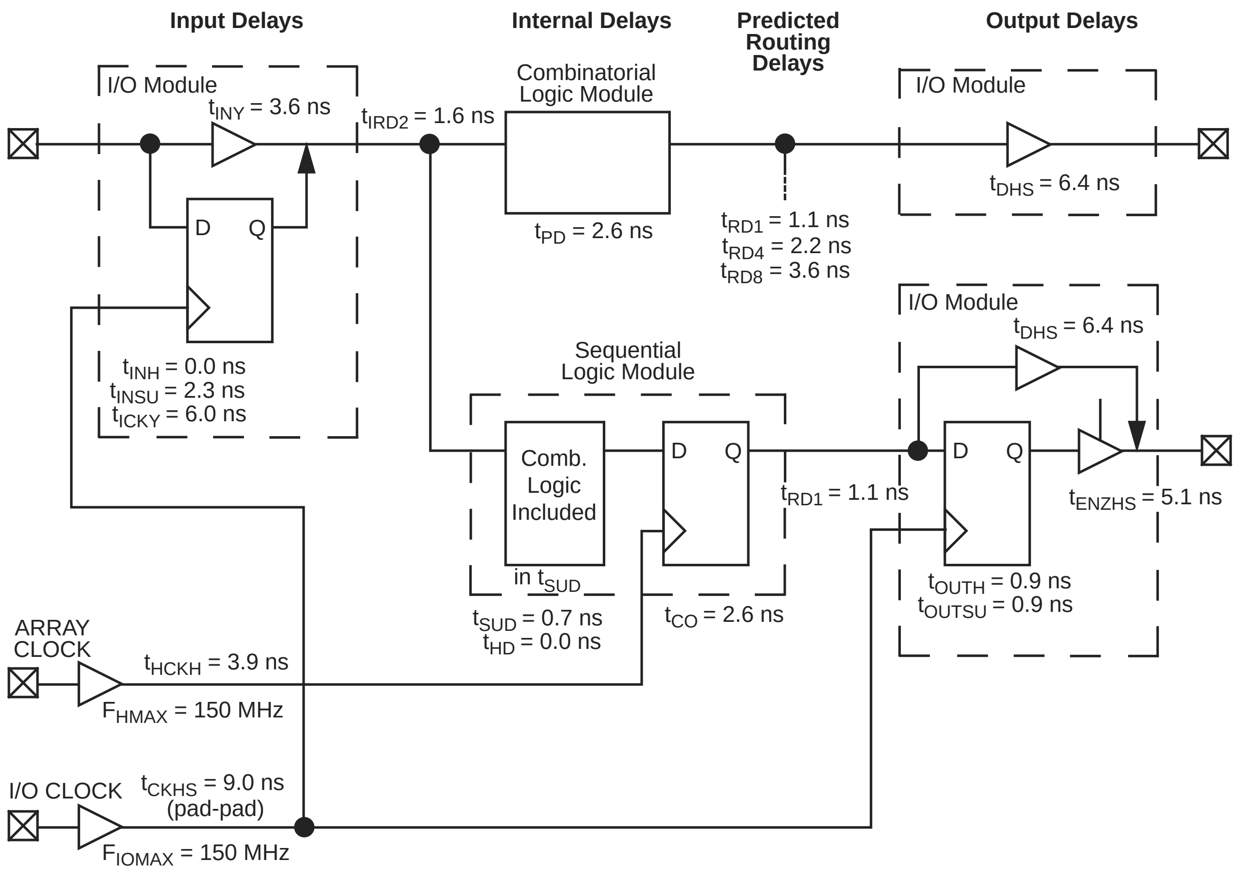
## Determining Average Switching Frequency

To determine the switching frequency for a design, you must have a detailed understanding of the data input values to the circuit. The following guidelines are meant to represent worst-case scenarios so that they can be generally used to predict the upper limits of power dissipation. These guidelines are as follows:

***Table 2-13*** **• Guidelines for Predicting Power Dissipation**

| Data | Value |
|---|---|
| Logic Modules (m) | 80% of modules |
| Inputs switching (n) | # inputs/4 |
| Outputs switching (p) | # output/4 |
| First routed array clock loads (q1) | 40% of sequential modules |
| Second routed array clock loads (q2) | 40% of sequential modules |
| Load capacitance (CL) | 35 pF |
| Average logic module switching rate (fm) | F/10 |
| Average input switching rate (fn) | F/5 |
| Average output switching rate (fp) | F/10 |
| Average first routed array clock rate (fq1) | F/2 |
| Average second routed array clock rate (fq2) | F/2 |
| Average dedicated array clock rate (fs1) | F |
| Average dedicated I/O clock rate (fs2) | F |

# ACT 3 Timing Model




*Note: Values shown for A1425A –1 speed grade device.*

***Figure 2-10* • Timing Model**

## A1425A, A14V25A Timing Characteristics (continued)

***Table 2-24*** **• A1425A, A14V25A Worst-Case Commercial Conditions, VCC = 4.75 V, $T_J$ = 70°C**

| I/O Module – TTL Output Timing[1] | | –3 Speed[2] | | –2 Speed[2] | | –1 Speed | | Std. Speed | | 3.3 V Speed[1] | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **Parameter/Description** | | **Min.** | **Max.** | **Min.** | **Max.** | **Min.** | **Max.** | **Min.** | **Max.** | **Min.** | **Max.** | |
| $t_{DHS}$ | Data to Pad, High Slew | | 5.0 | | 5.6 | | 6.4 | | 7.5 | | 9.8 | ns |
| $t_{DLS}$ | Data to Pad, Low Slew | | 8.0 | | 9.0 | | 10.2 | | 12.0 | | 15.6 | ns |
| $t_{ENZHS}$ | Enable to Pad, Z to H/L, High Slew | | 4.0 | | 4.5 | | 5.1 | | 6.0 | | 7.8 | ns |
| $t_{ENZLS}$ | Enable to Pad, Z to H/L, Low Slew | | 7.4 | | 8.3 | | 9.4 | | 11.0 | | 14.3 | ns |
| $t_{ENHSZ}$ | Enable to Pad, H/L to Z, High Slew | | 6.5 | | 7.5 | | 8.5 | | 10.0 | | 13.0 | ns |
| $t_{ENLSZ}$ | Enable to Pad, H/L to Z, Low Slew | | 6.5 | | 7.5 | | 8.5 | | 10.0 | | 13.0 | ns |
| $t_{CKHS}$ | IOCLK Pad to Pad H/L, High Slew | | 7.5 | | 7.5 | | 9.0 | | 10.0 | | 13.0 | ns |
| $t_{CKLS}$ | IOCLK Pad to Pad H/L, Low Slew | | 11.3 | | 11.3 | | 13.5 | | 15.0 | | 19.5 | ns |
| $d_{TLHHS}$ | Delta Low to High, High Slew | | 0.02 | | 0.02 | | 0.03 | | 0.03 | | 0.04 | ns/pF |
| $d_{TLHLS}$ | Delta Low to High, Low Slew | | 0.05 | | 0.05 | | 0.06 | | 0.07 | | 0.09 | ns/pF |
| $d_{THLHS}$ | Delta High to Low, High Slew | | 0.04 | | 0.04 | | 0.04 | | 0.05 | | 0.07 | ns/pF |
| $d_{THLLS}$ | Delta High to Low, Low Slew | | 0.05 | | 0.05 | | 0.06 | | 0.07 | | 0.09 | ns/pF |
| **I/O Module – CMOS Output Timing[1]** | | | | | | | | | | | | |
| $t_{DHS}$ | Data to Pad, High Slew | | 6.2 | | 7.0 | | 7.9 | | 9.3 | | 12.1 | ns |
| $t_{DLS}$ | Data to Pad, Low Slew | | 11.7 | | 13.1 | | 14.9 | | 17.5 | | 22.8 | ns |
| $t_{ENZHS}$ | Enable to Pad, Z to H/L, High Slew | | 5.2 | | 5.9 | | 6.6 | | 7.8 | | 10.1 | ns |
| $t_{ENZLS}$ | Enable to Pad, Z to H/L, Low Slew | | 8.9 | | 10.0 | | 11.3 | | 13.3 | | 17.3 | ns |
| $t_{ENHSZ}$ | Enable to Pad, H/L to Z, High Slew | | 6.7 | | 7.5 | | 8.5 | | 10.0 | | 13.0 | ns |
| $t_{ENLSZ}$ | Enable to Pad, H/L to Z, Low Slew | | 6.7 | | 7.5 | | 9.0 | | 10.0 | | 13.0 | ns |
| $t_{CKHS}$ | IOCLK Pad to Pad H/L, High Slew | | 8.9 | | 8.9 | | 10.7 | | 11.8 | | 15.3 | ns |
| $t_{CKLS}$ | IOCLK Pad to Pad H/L, Low Slew | | 13.0 | | 13.0 | | 15.6 | | 17.3 | | 22.5 | ns |
| $d_{TLHHS}$ | Delta Low to High, High Slew | | 0.04 | | 0.04 | | 0.05 | | 0.06 | | 0.08 | ns/pF |
| $d_{TLHLS}$ | Delta Low to High, Low Slew | | 0.07 | | 0.08 | | 0.09 | | 0.11 | | 0.14 | ns/pF |
| $d_{THLHS}$ | Delta High to Low, High Slew | | 0.03 | | 0.03 | | 0.03 | | 0.04 | | 0.05 | ns/pF |
| $d_{THLLS}$ | Delta High to Low, Low Slew | | 0.04 | | 0.04 | | 0.04 | | 0.05 | | 0.07 | ns/pF |

*Notes: **

1. *Delays based on 35 pF loading.*
2. *The –2 and –3 speed grades have been discontinued. Refer to PDN 0104, PDN 0203, PDN 0604, and PDN 1004 at http://www.microsemi.com/soc/support/notifications/default.aspx#pdn.*

## A14100A, A14V100A Timing Characteristics (continued)

*Table 2-35* • **A14100A, A14V100A Worst-Case Commercial Conditions, VCC = 4.75 V, $T_J$ = 70°C**

| I/O Module Input Propagation Delays | | –3 Speed[1] | | –2 Speed[1] | | –1 Speed | | Std. Speed | | 3.3 V Speed[1] | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **Parameter/Description** | | **Min.** | **Max.** | **Min.** | **Max.** | **Min.** | **Max.** | **Min.** | **Max.** | **Min.** | **Max.** | |
| $t_{INY}$ | Input Data Pad to Y | | 2.8 | | 3.2 | | 3.6 | | 4.2 | | 5.5 | ns |
| $t_{ICKY}$ | Input Reg IOCLK Pad to Y | | 4.7 | | 5.3 | | 6.0 | | 7.0 | | 9.2 | ns |
| $t_{OCKY}$ | Output Reg IOCLK Pad to Y | | 4.7 | | 5.3 | | 6.0 | | 7.0 | | 9.2 | ns |
| $t_{ICLRY}$ | Input Asynchronous Clear to Y | | 4.7 | | 5.3 | | 6.0 | | 7.0 | | 9.2 | ns |
| $t_{OCLRY}$ | Output Asynchronous Clear to Y | | 4.7 | | 5.3 | | 6.0 | | 7.0 | | 9.2 | ns |
| **Predicted Input Routing Delays[2]** | | | | | | | | | | | | |
| $t_{RD1}$ | FO = 1 Routing Delay | | 0.9 | | 1.0 | | 1.1 | | 1.3 | | 1.7 | ns |
| $t_{RD2}$ | FO = 2 Routing Delay | | 1.2 | | 1.4 | | 1.6 | | 1.8 | | 2.4 | ns |
| $t_{RD3}$ | FO = 3 Routing Delay | | 1.4 | | 1.6 | | 1.8 | | 2.1 | | 2.8 | ns |
| $t_{RD4}$ | FO = 4 Routing Delay | | 1.7 | | 1.9 | | 2.2 | | 2.5 | | 3.3 | ns |
| $t_{RD8}$ | FO = 8 Routing Delay | | 2.8 | | 3.2 | | 3.6 | | 4.2 | | 5.5 | ns |
| **I/O Module Sequential Timing (wrt IOCLK pad)** | | | | | | | | | | | | |
| $t_{INH}$ | Input F-F Data Hold | 0.0 | | 0.0 | | 0.0 | | 0.0 | | 0.0 | | ns |
| $t_{INSU}$ | Input F-F Data Setup | 1.2 | | 1.4 | | 1.5 | | 1.8 | | 1.8 | | ns |
| $t_{IDEH}$ | Input Data Enable Hold | 0.0 | | 0.0 | | 0.0 | | 0.0 | | 0.0 | | ns |
| $t_{IDESU}$ | Input Data Enable Setup | 5.8 | | 6.5 | | 7.5 | | 8.6 | | 8.6 | | ns |
| $t_{OUTH}$ | Output F-F Data hold | 0.7 | | 0.8 | | 1.0 | | 1.0 | | 1.0 | | ns |
| $t_{OUTSU}$ | Output F-F Data Setup | 0.7 | | 0.8 | | 1.0 | | 1.0 | | 1.0 | | ns |
| $t_{ODEH}$ | Output Data Enable Hold | 0.3 | | 0.4 | | 0.5 | | 0.5 | | 0.5 | | ns |
| $f_{ODESU}$ | Output Data Enable Setup | 1.3 | | 1.5 | | 2.0 | | 2.0 | | 2.0 | | ns |

*Notes: **

1. *The –2 and –3 speed grades have been discontinued. Refer to PDN 0104, PDN 0203, PDN 0604, and PDN 1004 at http://www.microsemi.com/soc/support/notifications/default.aspx#pdn.*
2. *Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual worst-case performance. Post-route timing is based on actual routing delay measurements performed on the device prior to shipment.*

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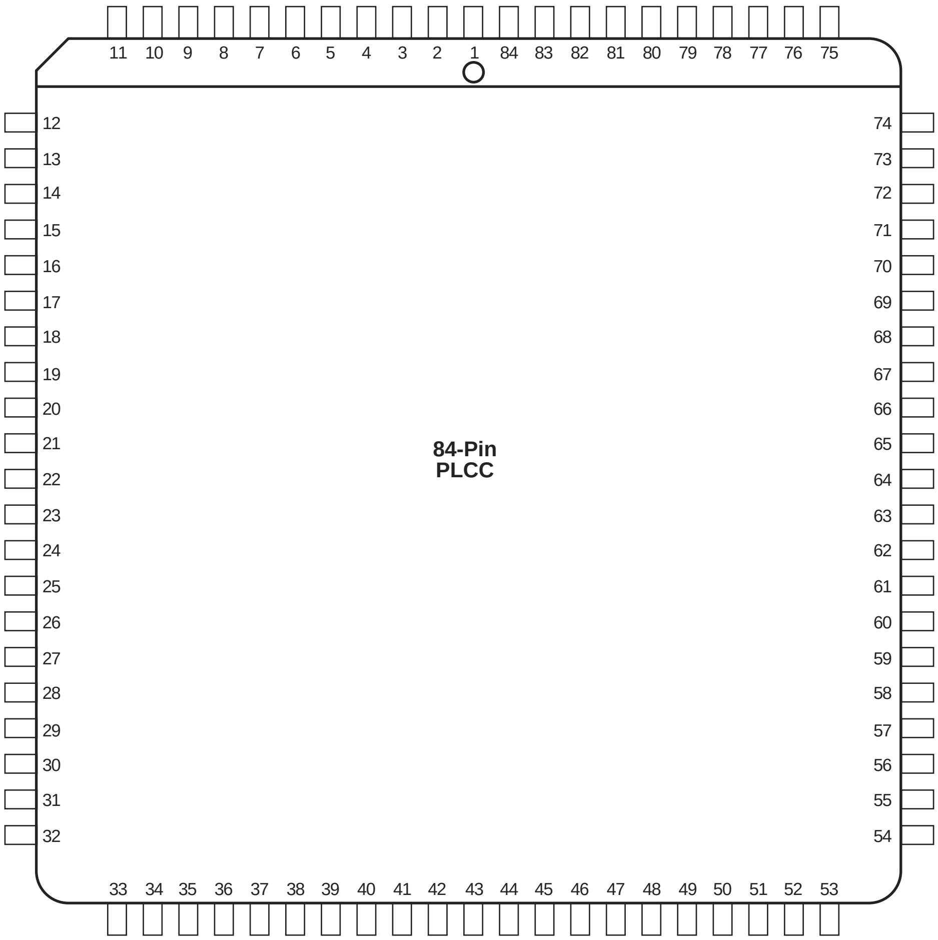
# 3 – Package Pin Assignments

## PL84

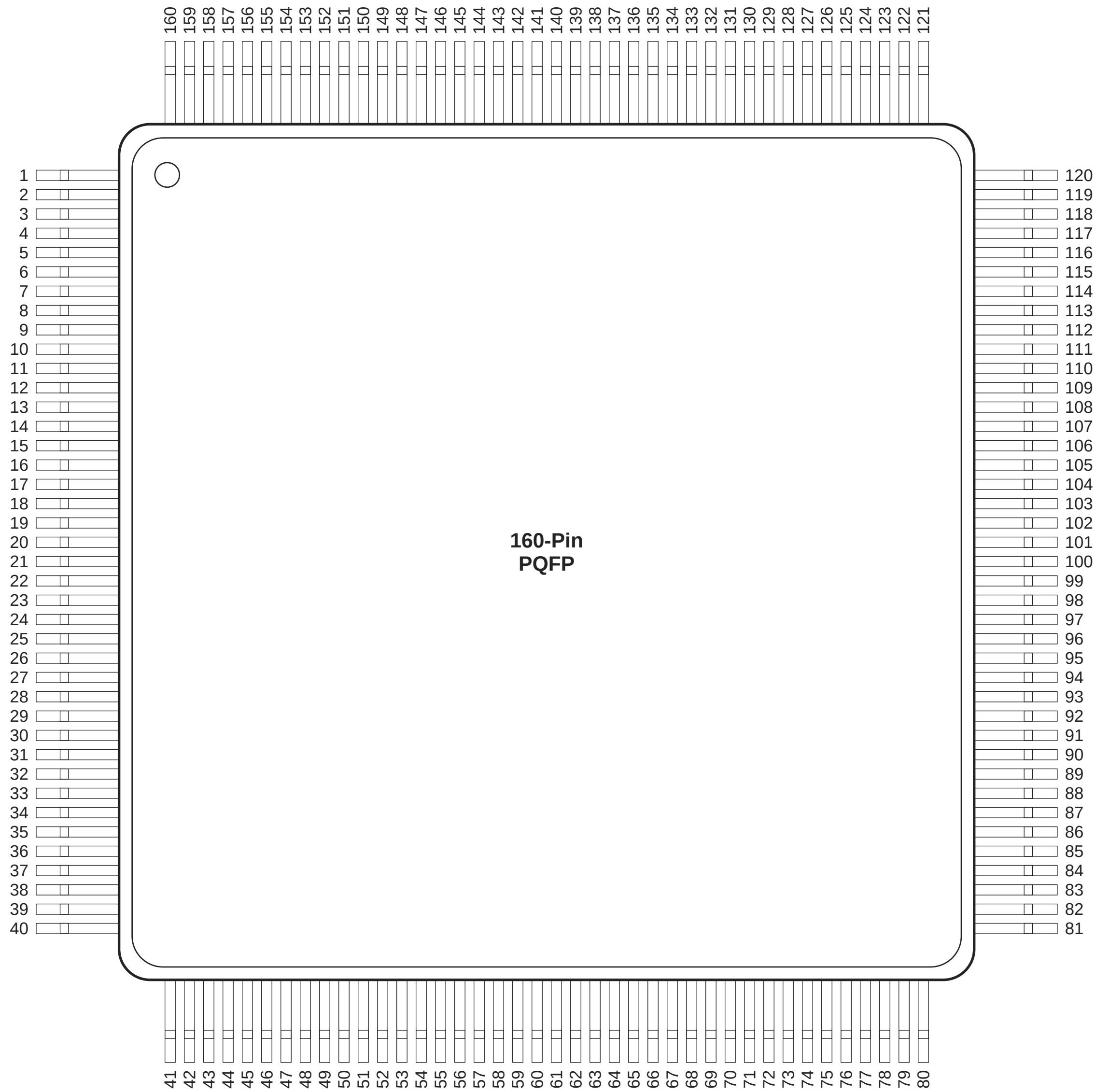



*Note: This is the top view of the package.*

### *Note*

For Package Manufacturing and Environmental information, visit the Resource Center at http://www.microsemi.com/soc/products/solutions/package/docs.aspx.

## PQ160

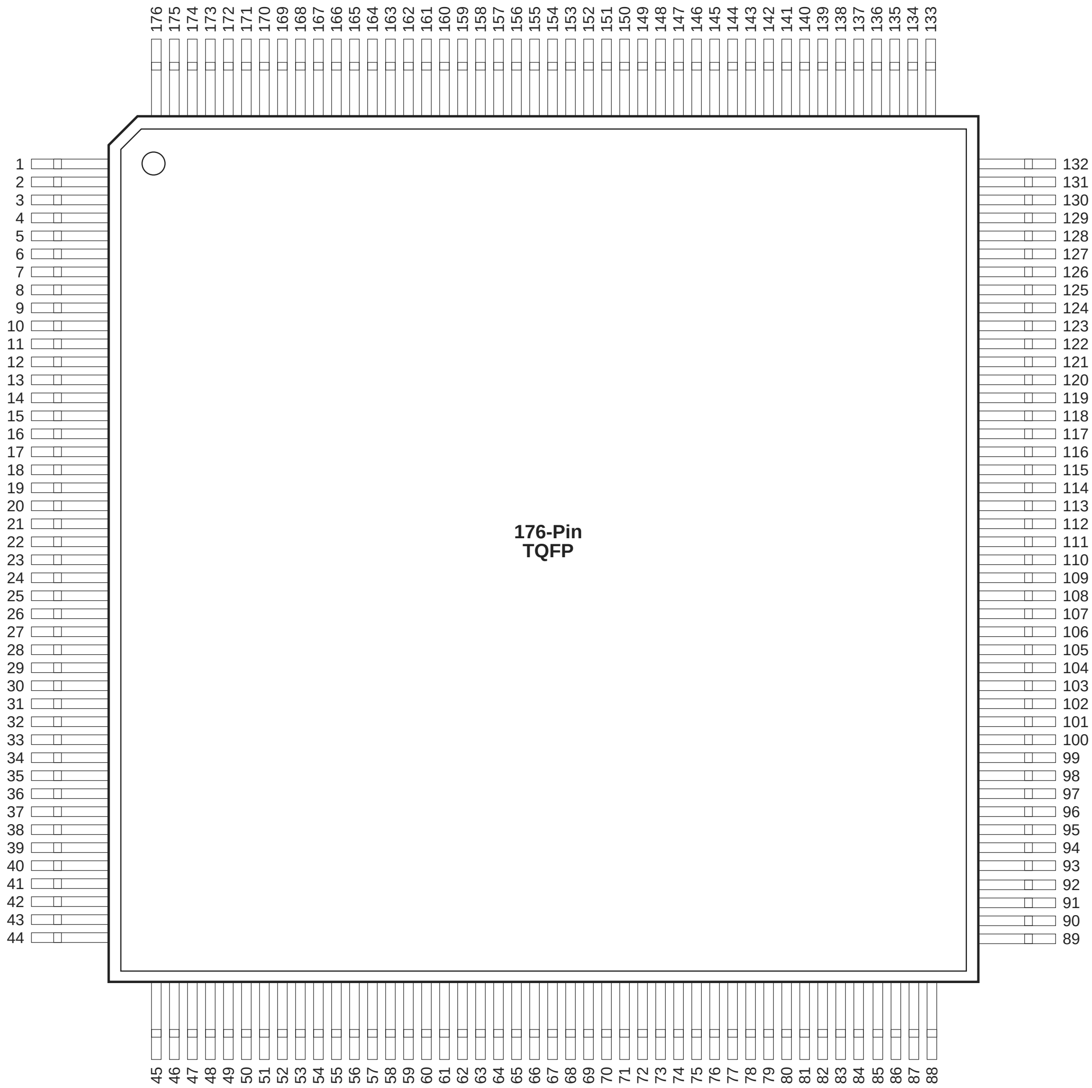



*Note: This is the top view of the package*

### *Note*

For Package Manufacturing and Environmental information, visit the Resource Center at http://www.microsemi.com/soc/products/solutions/package/docs.aspx

# TQ176

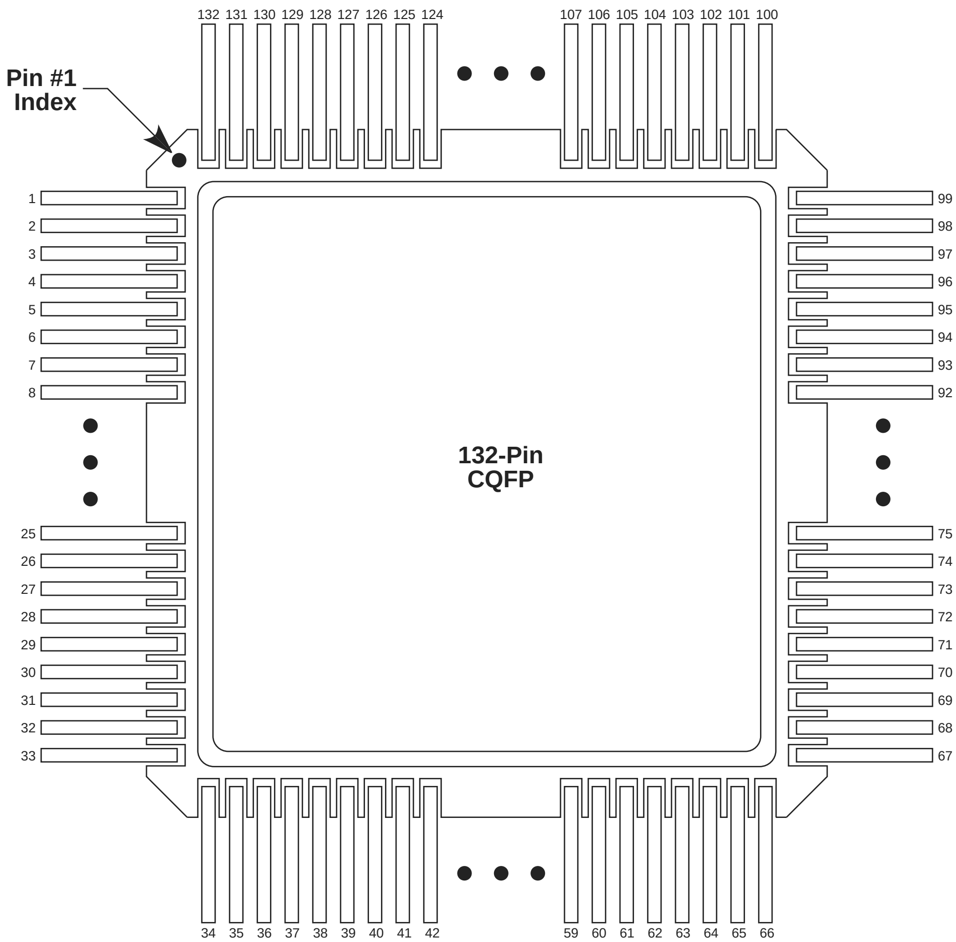



*Note: This is the top view.*

## Note

For Package Manufacturing and Environmental information, visit the Resource Center at http://www.microsemi.com/soc/products/solutions/package/docs.aspx

# CQ132

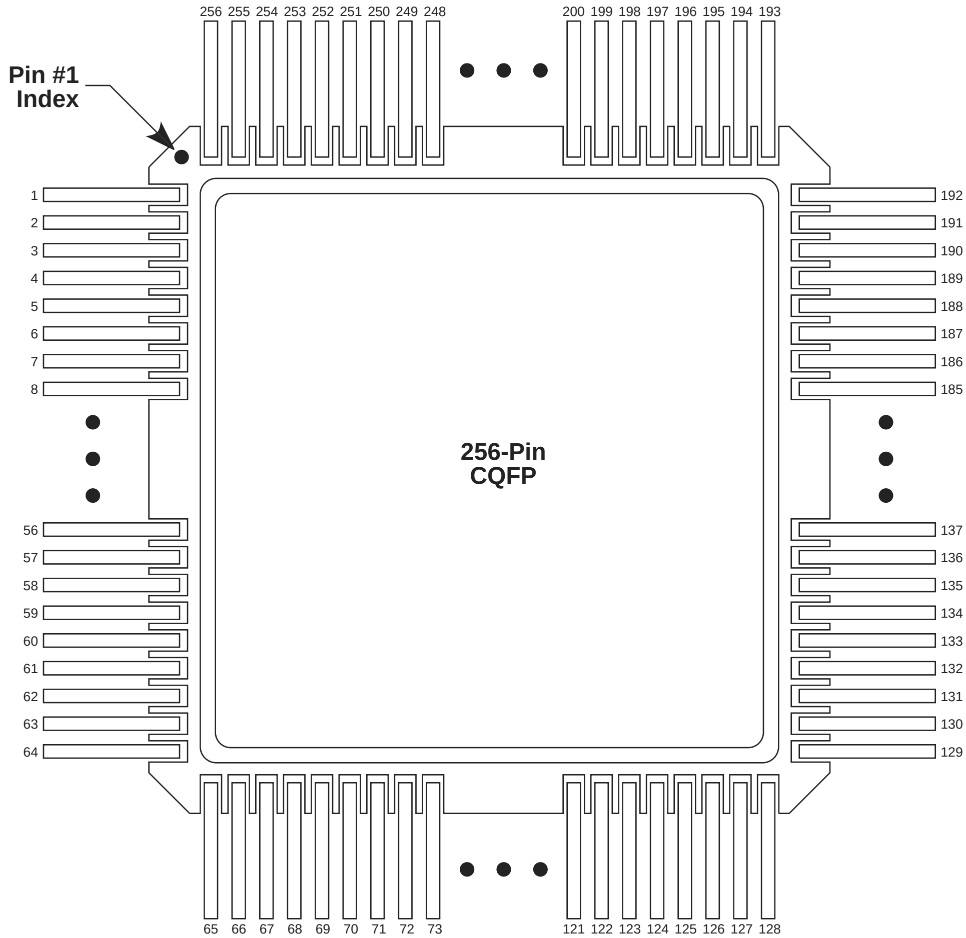



*Note: This is the top view*

## *Note*

For Package Manufacturing and Environmental information, visit the Resource Center at
http://www.microsemi.com/soc/products/solutions/package/docs.aspx

# CQ256

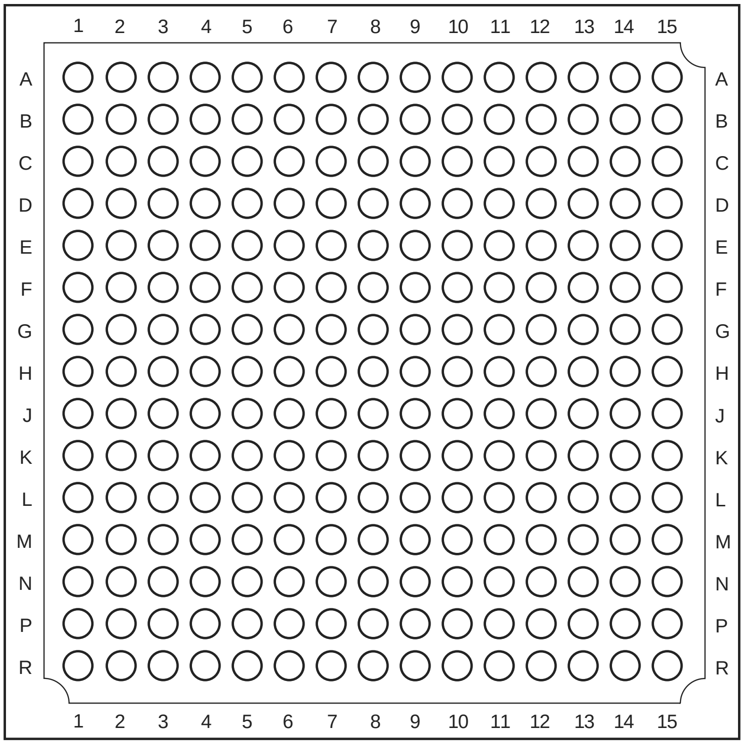



*Note: This is the top view.*

## *Note*

For Package Manufacturing and Environmental information, visit the Resource Center at http://www.microsemi.com/soc/products/solutions/package/docs.aspx

# BG225

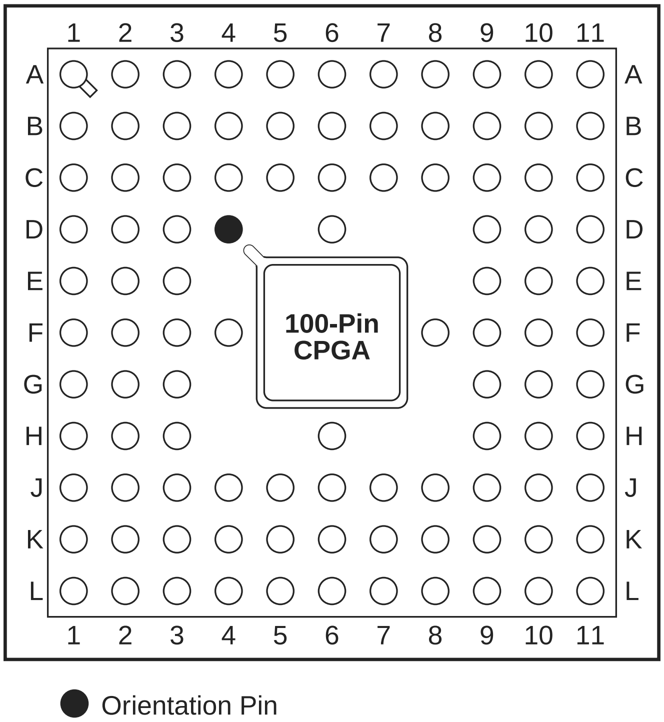



*Note: This is the top view.*

## *Note*

For Package Manufacturing and Environmental information, visit the Resource Center at http://www.microsemi.com/soc/products/solutions/package/docs.aspx

# PG100

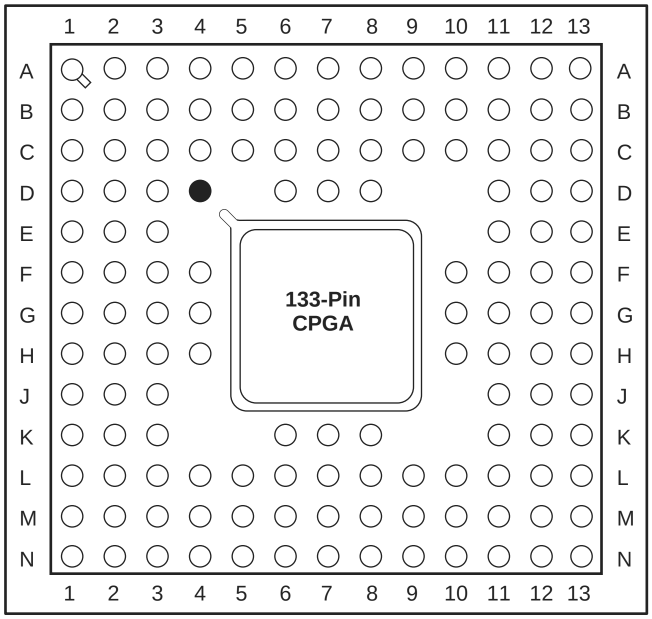



*Note: This is the top view.*

## *Note*

For Package Manufacturing and Environmental information, visit the Resource Center at http://www.microsemi.com/soc/products/solutions/package/docs.aspx

# PG133

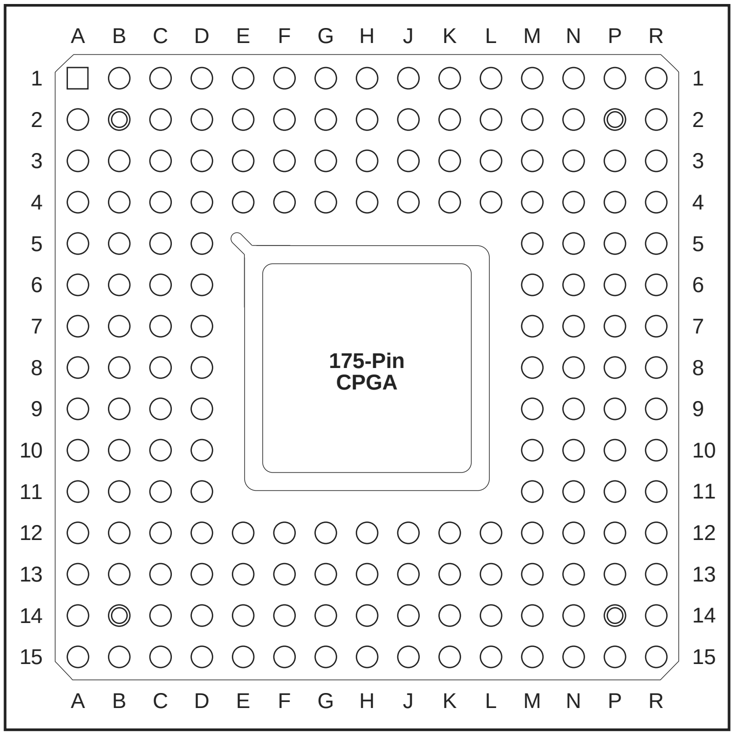



*Note: This is the top view.*

## *Note*

For Package Manufacturing and Environmental information, visit the Resource Center at http://www.microsemi.com/soc/products/solutions/package/docs.aspx

# PG175




*Note: This is the top view.*

## *Note*

For Package Manufacturing and Environmental information, visit the Resource Center at http://www.microsemi.com/soc/products/solutions/package/docs.aspx

| PG207 | |
|---|---|
| **A1460 Function** | **Location** |
| CLKA or I/O | K1 |
| CLKB or I/O | J3 |
| DCLK or I/O | E4 |
| GND | C14, D4, D5, D9, D14, J4, J14, P3, P4, P7, P9, P14, R15 |
| HCLK or I/O | J15 |
| IOCLK or I/O | P5 |
| IOPCL or I/O | N14 |
| MODE | D7 |
| NC | A1, A2, A16, A17, B1, B17, C1, C2, S1, S3, S17, T1, T2, T16, T17 |
| PRA or I/O | H1 |
| PRB or I/O | K16 |
| SDI or I/O | C3 |
| SDO | P15 |
| VCC | B2, B9, B16, D11, J2, J16, P12, S2, S9, S16, T5 |

*Notes:*

1. All unlisted pin numbers are user I/Os.
2. NC denotes no connection.
3. MODE should be terminated to GND through a 10K resistor to enable Actionprobe usage; otherwise it can be terminated directly to GND.

# Datasheet Categories

### *Categories*

In order to provide the latest information to designers, some datasheet parameters are published before data has been fully characterized from silicon devices. The data provided for a given device is designated as either "Product Brief," "Advance," "Preliminary," or "Production." The definitions of these categories are as follows:

### *Product Brief*

The product brief is a summarized version of a datasheet (advance or production) and contains general product information. This document gives an overview of specific device and family information.

### *Advance*

This version contains initial estimated information based on simulation, other products, devices, or speed grades. This information can be used as estimates, but not for production. This label only applies to the DC and Switching Characteristics chapter of the datasheet and will only be used when the data has not been fully characterized.

### *Preliminary*

The datasheet contains information based on simulation and/or initial characterization. The information is believed to be correct, but changes are possible.

### *Production*

This version contains information that is considered to be final.

## Export Administration Regulations (EAR)

The products described in this document are subject to the Export Administration Regulations (EAR). They could require an approved export license prior to export from the United States. An export includes release of product or disclosure of technology to a foreign national inside or outside the United States.

# Safety Critical, Life Support, and High-Reliability Applications Policy

The products described in this advance status document may not have completed the Microsemi qualification process. Products may be amended or enhanced during the product introduction and qualification process, resulting in changes in device functionality or performance. It is the responsibility of each customer to ensure the fitness of any product (but especially a new product) for a particular purpose, including appropriateness for safety-critical, life-support, and other high-reliability applications. Consult the Microsemi SoC Products Group Terms and Conditions for specific liability exclusions relating to life-support applications. A reliability report covering all of the SoC Products Group's products is available at http://www.microsemi.com/soc/documents/ORT_Report.pdf. Microsemi also offers a variety of enhanced qualification and lot acceptance screening procedures. Contact your local sales office for additional reliability information.