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Understanding <u>Embedded - FPGAs (Field</u> <u>Programmable Gate Array)</u>

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Details	
Product Status	Obsolete
Number of LABs/CLBs	564
Number of Logic Elements/Cells	-
Total RAM Bits	-
Number of I/O	70
Number of Gates	4000
Voltage - Supply	4.5V ~ 5.5V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 85°C (TA)
Package / Case	84-LCC (J-Lead)
Supplier Device Package	84-PLCC (29.31x29.31)
Purchase URL	https://www.e-xfl.com/product-detail/microsemi/a1440a-1pl84i

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

Accelerator Series FPGAs – ACT 3 Family

		Speed Grade ¹ Application ¹						
Device/Package	Std.	-1	-2	-3	С	I	м	В
A14V40A Device							•	
84-Pin Plastic Leaded Chip Carrier (PLCC)	1	-	-	_	1	_	_	_
100-Pin Very Thin Quad Flatpack (VQFP)	✓	-	-	-	1	-	-	-
160-Pin Plastic Quad Flatpack (PQFP)	~	-	-	-	✓	-	-	-
176-Pin Thin Quad Flatpack (TQFP)	✓	-	-	-	✓	-	-	-
A1460A Device		•		I			1	
160-Pin Plastic Quad Flatpack (PQFP)	✓	✓	D	D	1	~	-	-
176-Pin Thin Quad Flatpack (TQFP)	✓	~	D	D	✓	✓	-	-
196-Pin Ceramic Quad Flatpack (CQFP)	1	1	-	_	1	-	1	1
207-Pin Ceramic Pin Grid Array (CPGA)	1	1	D	D	1	-	1	1
208-Pin Plastic Quad Flatpack (PQFP)	1	 ✓ 	D	D	1	1	-	_
225-Pin Plastic Ball Grid Array (BGA)	D	D	D	D	D	-	-	-
A14V60A Device					-		-	
160-Pin Plastic Quad Flatpack (PQFP)	✓	-	-	_	~	-	_	-
176-Pin Thin Quad Flatpack (TQFP)	✓	-	-	-	1	-	-	-
208-Pin Plastic Quad Flatpack (PQFP)	✓	-	-	_	~	-	_	_
A14100A Device								
208-Pin Power Quad Flatpack (RQFP)	✓	~	D	D	~	~	_	_
257-Pin Ceramic Pin Grid Array (CPGA)	✓	~	D	D	~	-	~	~
313-Pin Plastic Ball Grid Array (BGA)	✓	~	D	D	~	-	_	-
256-Pin Ceramic Quad Flatpack (CQFP)	✓	~	-	_	~	-	~	~
A14V100A Device								
208-Pin Power Quad Flatpack (RQFP)	✓	_	_	_	1	_	_	_
313-Pin Plastic Ball Grid Array (BGA)	✓	-	-	-	1	-	-	-

Notes:

1. Applications: C = CommercialI = Industrial
M = Military
Commercial only

- Availability:
- ✓ = Available
- P = Planned- = Not planned
- D = Discontinued

Speed Grade:

-1 = Approx. 15% faster than Std. -2 = Approx. 25% faster than Std. -3 = Approx. 35% faster than Std. (-2 and -3 speed grades have been discontinued.)



ACT 3 Family Overview

Device and Speed Grade	t _{CKHS} (ns)	t _{TRACE} (ns)	t _{INSU} (ns)	Total (ns)	MHz
A1425A -3	7.5	1.0	1.8	10.3	97
A1460A -3	9.0	1.0	1.3	11.3	88
A1425A -2	7.5	1.0	2.0	10.5	95
A1460A -2	9.0	1.0	1.5	11.5	87
A1425A -1	9.0	1.0	2.3	12.3	81
A1460A -1	10.0	1.0	1.8	12.8	78
A1425A STD	10.0	1.0	2.7	13.7	73
A1460A STD	11.5	1.0	2.0	14.5	69

Table 1-1 • Chip-to-Chip Performance (worst-case commercial)

Note: The –2 and –3 speed grades have been discontinued. Refer to PDN 0104, PDN 0203, PDN 0604, and PDN 1004 at http://www.microsemi.com/soc/support/notifications/default.aspx#pdn.

Antifuse Connections

An antifuse is a "normally open" structure as opposed to the normally closed fuse structure used in PROMs or PALs. The use of antifuses to implement a programmable logic device results in highly testable structures as well as an efficient programming architecture. The structure is highly testable because there are no preexisting connections; temporary connections can be made using pass transistors. These temporary connections can isolate individual antifuses to be programmed as well as isolate individual circuit structures to be tested. This can be done both before and after programming. For example, all metal tracks can be tested for continuity and shorts between adjacent tracks, and the functionality of all logic modules can be verified.

Four types of antifuse connections are used in the routing structure of the ACT 3 array. (The physical structure of the antifuse is identical in each case; only the usage differs.)

Table 2-1 shows four types of antifuses.

Table 2-1 •	Antifuse	Types
-------------	----------	-------

Туре	Description
XF	Horizontal-to-vertical connection
HF	Horizontal-to-horizontal connection
VF	Vertical-to-vertical connection
FF	"Fast" vertical connection

Examples of all four types of connections are shown in Figure 2-7 on page 2-6 and Figure 2-8 on page 2-6.

Module Interface

Connections to Logic and I/O modules are made through vertical segments that connect to the module inputs and outputs. These vertical segments lie on vertical tracks that span the entire height of the array.

Module Input Connections

The tracks dedicated to module inputs are segmented by pass transistors in each module row. During normal user operation, the pass transistors are inactive, which isolates the inputs of a module from the inputs of the module directly above or below it. During certain test modes, the pass transistors are active to verify the continuity of the metal tracks. Vertical input segments span only the channel above or the channel below. The logic modules are arranged such that half of the inputs are connected to the channel above and half of the inputs to segments in the channel below, as shown in Figure 2-9.



Figure 2-9 • Logic Module Routing Interface



Power Dissipation

P = [ICC standby + lactive] * VCC * IOL * VOL * N + IOH* (VCC - VOH) * M

where:

EQ 3

ICC standby is the current flowing when no inputs or outputs are changing

lactive is the current flowing due to CMOS switching.

IOL and IOH are TTL sink/source current.

VOL and VOH are TTL level output voltages.

N is the number of outputs driving TTL loads to VOL.

M equals the number of outputs driving TTL loads to VOH.

An accurate determination of N and M is problematical because their values depend on the design and on the system I/O. The power can be divided into two components: static and active.

Static Power Component

Microsemi FPGAs have small static power components that result in lower power dissipation than PALs or PLDs. By integrating multiple PALs/PLDs into one FPGA, an even greater reduction in board-level power dissipation can be achieved.

The power due to standby current is typically a small component of the overall power. Standby power is calculated in Table 2-9 for commercial, worst case conditions.

Table 2-9 • Standby Power Calculation

ICC	VCC	Power
2 mA	5.25 V	10.5 mW

The static power dissipated by TTL loads depends on the number of outputs driving high or low and the DC load current. Again, this value is typically small. For instance, a 32-bit bus sinking 4 mA at 0.33 V will generate 42 mW with all outputs driving low, and 140 mW with all outputs driving high. The actual dissipation will average somewhere between as I/Os switch states with time.

Active Power Component

Power dissipation in CMOS devices is usually dominated by the active (dynamic) power dissipation. This component is frequency dependent, a function of the logic and the external I/O. Active power dissipation results from charging internal chip capacitances of the interconnect, unprogrammed antifuses, module inputs, and module outputs, plus external capacitance due to PC board traces and load device inputs.

An additional component of the active power dissipation is the totem-pole current in CMOS transistor pairs. The net effect can be associated with an equivalent capacitance that can be combined with frequency and voltage to represent active power dissipation.

Equivalent Capacitance

The power dissipated by a CMOS circuit can be expressed by EQ 4.

Power (μ W) = C_{EQ} * VCC² * F

EQ 4

Where:

 C_{EQ} is the equivalent capacitance expressed in pF.

VCC is the power supply in volts.

F is the switching frequency in MHz.



Table 2-11 • Fixed Capacitance Values for Microsemi FPGAs

Device Type	r1, routed_Clk1	r2, routed_Clk2
A1415A	60	60
A14V15A	57	57
A1425A	75	75
A14V25A	72	72
A1440A	105	105
A14V40A	100	100
A1440B	105	105
A1460A	165	165
A14V60A	157	157
A1460B	165	165
A14100A	195	195
A14V100A	185	185
A14100B	195	195

Table 2-12 • Fixed Clock Loads (s1/s2)

Device Type	s1, Clock Loads on Dedicated Array Clock	s2, Clock Loads on Dedicated I/O Clock
A1415A	104	80
A14V15A	104	80
A1425A	160	100
A14V25A	160	100
A1440A	288	140
A14V40A	288	140
A1440B	288	140
A1460A	432	168
A14V60A	432	168
A1460B	432	168
A14100A	697	228
A14V100A	697	228
A14100B	697	228







Figure 2-14 • Module Delays



Figure 2-15 • Sequential Module Timing Characteristics



A1415A, A14V15A Timing Characteristics

Table 2-18 • A1415A, A14V15A Worst-Case Commercial Conditions, VCC = 4.75 V, T_J = 70°C¹

Logic Module Propagation Delays ²		–3 S	peed ³	-2 S	beed ³	-1 Speed		Std. Speed		3.3 V Speed ¹		Units
Parame	eter/Description	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t _{PD}	Internal Array Module		2.0		2.3		2.6		3.0		3.9	ns
t _{CO}	Sequential Clock to Q		2.0		2.3		2.6		3.0		3.9	ns
t _{CLR}	Asynchronous Clear to Q		2.0		2.3		2.6		3.0		3.9	ns
Predict	ed Routing Delays ⁴			-								
t _{RD1}	FO = 1 Routing Delay		0.9		1.0		1.1		1.3		1.7	ns
t _{RD2}	FO = 2 Routing Delay		1.2		1.4		1.6		1.8		2.4	ns
t _{RD3}	FO = 3 Routing Delay		1.4		1.6		1.8		2.1		2.8	ns
t _{RD4}	FO = 4 Routing Delay		1.7		1.9		2.2		2.5		3.3	ns
t _{RD8}	FO = 8 Routing Delay		2.8		3.2		3.6		4.2		5.5	ns
Logic N	Iodule Sequential Timing			-			-		-	-		-
t _{SUD}	Flip-Flop Data Input Setup	0.5		0.6		0.7		0.8		0.8		ns
t _{HD}	Flip-Flop Data Input Hold	0.0		0.0		0.0		0.0		0.0		ns
t _{SUD}	Latch Data Input Setup	0.5		0.6		0.7		0.8		0.8		ns
t _{HD}	Latch Data Input Hold	0.0		0.0		0.0		0.0		0.0		ns
t _{WASYN}	Asynchronous Pulse Width	1.9		2.4		3.2		3.8		4.8		ns
t _{WCLKA}	Flip-Flop Clock Pulse Width	1.9		2.4		3.2		3.8		4.8		ns
t _A	Flip-Flop Clock Input Period	4.0		5.0		6.8		8.0		10.0		ns
f _{MAX}	Flip-Flop Clock Frequency		250		200		150		125		100	MHz

Notes:

1. VCC = 3.0 V for 3.3 V specifications.

2. For dual-module macros, use $t_{PD} + t_{RD1} + t_{PDn} + t_{CO} + t_{RD1} + t_{PDn}$ or $t_{PD1} + t_{RD1} + t_{SUD}$, whichever is appropriate.

3. The –2 and –3 speed grades have been discontinued. Please refer to the Product Discontinuation Notices (PDNs) listed below:

PDN March 2001 PDN 0104 PDN 0203 PDN 0604 PDN 1004

4. Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual worst-case performance. Post-route timing is based on actual routing delay measurements performed on the device prior to shipment.

A1425A, A14V25A Timing Characteristics (continued)

Table 2-23 • A1425A.	A14V25A Worst-Case	Commercial Conditions.	$VCC = 4.75 V. T_1 = 70^{\circ}C$
TUDICE ED ATTEORY	ATTE CA TOTOL OUDO	oomanionola oomaniono,	100 - 110 1, 13 - 10 0

I/O Module Input Propagation Delays		-3 Sp	beed ¹	-2 Sp	beed ¹	–1 S	peed	Std. Speed		3.3 V Speed ¹		Units
Parameter/Description		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t _{INY}	Input Data Pad to Y		2.8		3.2		3.6		4.2		5.5	ns
t _{ICKY}	Input Reg IOCLK Pad to Y		4.7		5.3		6.0		7.0		9.2	ns
t _{OCKY}	Output Reg IOCLK Pad to Y		4.7		5.3		6.0		7.0		9.2	ns
t _{ICLRY}	Input Asynchronous Clear to Y		4.7		5.3		6.0		7.0		9.2	ns
t _{OCLRY}	Output Asynchronous Clear to Y		4.7		5.3		6.0		7.0		9.2	ns
Predict	ed Input Routing Delays ²			•								
t _{RD1}	FO = 1 Routing Delay		0.9		1.0		1.1		1.3		1.7	ns
t _{RD2}	FO = 2 Routing Delay		1.2		1.4		1.6		1.8		2.4	ns
t _{RD3}	FO = 3 Routing Delay		1.4		1.6		1.8		2.1		2.8	ns
t _{RD4}	FO = 4 Routing Delay		1.7		1.9		2.2		2.5		3.3	ns
t _{RD8}	FO = 8 Routing Delay		2.8		3.2		3.6		4.2		5.5	ns
I/O Mod	dule Sequential Timing (wrt IOCLK	pad)		•								
t _{INH}	Input F-F Data Hold	0.0		0.0		0.0		0.0		0.0		ns
t _{INSU}	Input F-F Data Setup	1.8		2.0		2.3		2.7		3.0		ns
t _{IDEH}	Input Data Enable Hold	0.0		0.0		0.0		0.0		0.0		ns
t _{IDESU}	Input Data Enable Setup	5.8		6.5		7.5		8.6		8.6		ns
t _{OUTH}	Output F-F Data hold	0.7		0.8		0.9		1.0		1.0		ns
t _{OUTSU}	Output F-F Data Setup	0.7		0.8		0.9		1.0		1.0		ns
t _{ODEH}	Output Data Enable Hold	0.3		0.4		0.4		0.5		0.5		ns
f _{ODESU}	Output Data Enable Setup	1.3		1.5		1.7		2.0		2.0		ns

Notes: *

1. The –2 and –3 speed grades have been discontinued. Refer to PDN 0104, PDN 0203, PDN 0604, and PDN 1004 at http://www.microsemi.com/soc/support/notifications/default.aspx#pdn.

 Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual worst-case performance. Post-route timing is based on actual routing delay measurements performed on the device prior to shipment.



A1460A, A14V60A Timing Characteristics

Table 2-30 • A1460A, A14V60A Worst-Case Commercial Conditions, VCC = 4.75 V, T_J = 70°C¹

Logic Module Propagation Delays ²		-3 S	peed ³	–2 Sp	beed ³	-1 Speed		Std. Speed		3.3 V Speed ¹		Units
Parame	eter/Description	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t _{PD}	Internal Array Module		2.0		2.3		2.6		3.0		3.9	ns
t _{CO}	Sequential Clock to Q		2.0		2.3		2.6		3.0		3.9	ns
t _{CLR}	Asynchronous Clear to Q		2.0		2.3		2.6		3.0		3.9	ns
Predict	ed Routing Delays ⁴	-									-	
t _{RD1}	FO = 1 Routing Delay		0.9		1.0		1.1		1.3		1.7	ns
t _{RD2}	FO = 2 Routing Delay		1.2		1.4		1.6		1.8		2.4	ns
t _{RD3}	FO = 3 Routing Delay		1.4		1.6		1.8		2.1		2.8	ns
t _{RD4}	FO = 4 Routing Delay		1.7		1.9		2.2		2.5		3.3	ns
t _{RD8}	FO = 8 Routing Delay		2.8		3.2		3.6		4.2		5.5	ns
Logic N	Nodule Sequential Timing	-									-	
t _{SUD}	Flip-Flop Data Input Setup	0.5		0.6		0.7		0.8		0.8		ns
t _{HD}	Flip-Flop Data Input Hold	0.0		0.0		0.0		0.0		0.0		ns
t _{SUD}	Latch Data Input Setup	0.5		0.6		0.7		0.8		0.8		ns
t _{HD}	Latch Data Input Hold	0.0		0.0		0.0		0.0		0.0		ns
t _{WASYN}	Asynchronous Pulse Width	2.4		3.2		3.8		4.8		6.5		ns
t _{WCLKA}	Flip-Flop Clock Pulse Width	2.4		3.2		3.8		4.8		6.5		ns
t _A	Flip-Flop Clock Input Period	5.0		6.8		8.0		10.0		13.4		ns
f _{MAX}	Flip-Flop Clock Frequency		200		150		125		100		75	MHz

Notes:

1. VCC = 3.0 V for 3.3 V specifications.

2. For dual-module macros, use $t_{PD} + t_{RD1} + t_{PDn} + t_{CO} + t_{RD1} + t_{PDn}$ or $t_{PD1} + t_{RD1} + t_{SUD}$, whichever is appropriate.

3. The –2 and –3 speed grades have been discontinued. Refer to PDN 0104, PDN 0203, PDN 0604, and PDN 1004 at http://www.microsemi.com/soc/support/notifications/default.aspx#pdn.

4. Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual worst-case performance. Post-route timing is based on actual routing delay measurements performed on the device prior to shipment.

PQ160



Note: This is the top view of the package

Note



Package Pin Assignments

TQ176



Note: This is the top view.

Note

Accelerator Series FPGAs – ACT 3 Family

	VQ100				
Pin Number	A1415, A14V15 Function	A1425, A14V25 Function	A1440, A14V40 Function		
1	GND	GND	GND		
2	SDI, I/O	SDI, I/O	SDI, I/O		
7	MODE	MODE	MODE		
8	VCC	VCC	VCC		
9	GND	GND	GND		
20	VCC	VCC	VCC		
21	NC	I/O	I/O		
34	PRB, I/O	PRB, I/O	PRB, I/O		
35	VCC	VCC	VCC		
36	GND	GND	GND		
37	VCC	VCC	VCC		
39	HCLK, I/O	HCLK, I/O	HCLK, I/O		
49	SDO	SDO	SDO		
50	IOPCL, I/O	IOPCL, I/O	IOPCL, I/O		
51	GND	GND	GND		
57	VCC	VCC	VCC		
58	VCC	VCC	VCC		
67	VCC	VCC	VCC		
68	GND	GND	GND		
69	GND	GND	GND		
74	NC	I/O	I/O		
75	IOCLK, I/O	IOCLK, I/O	IOCLK, I/O		
87	CLKA, I/O	CLKA, I/O	CLKA, I/O		
88	CLKB, I/O	CLKB, I/O	CLKB, I/O		
89	VCC	VCC	VCC		
90	VCC	VCC	VCC		
91	GND	GND	GND		
92	PRA, I/O	PRA, I/O	PRA, I/O		
93	NC	I/O	I/O		
100	DCLK, I/O	DCLK, I/O	DCLK, I/O		

- 1. All unlisted pin numbers are user I/Os.
- 2. NC denotes no connection.
- 3. MODE should be terminated to GND through a 10K resistor to enable Actionprobe usage; otherwise it can be terminated directly to GND.

Accelerator Series FPGAs - ACT 3 Family

CQ132			CQ132	
Pin Number	A1425 Function	Pin Number	A1425 Function	
1	NC	67	NC	
2	GND	74	GND	
3	SDI, I/O	75	VCC	
9	MODE	78	VCC	
10	GND	89	VCC	
11	VCC	90	GND	
22	VCC	91	VCC	
26	GND	92	GND	
27	VCC	98	IOCLK, I/O	
34	NC	99	NC	
36	GND	100	NC	
42	GND	101	GND	
43	VCC	106	GND	
48	PRB, I/O	107	VCC	
50	HCLK, I/O	116	CLKA, I/O	
58	GND	117	CLKB, I/O	
59	VCC	118	PRA, I/O	
63	SDO	122	GND	
64	IOPCL, I/O	123	VCC	
65	GND	131	DCLK, I/O	
66	NC	132	NC	

- 1. All unlisted pin numbers are user I/Os.
- 2. NC denotes no connection.
- 3. MODE should be terminated to GND through a 10K resistor to enable Actionprobe usage; otherwise it can be terminated directly to GND.

Package Pin Assignments

BG225



Note: This is the top view.

Note

Accelerator Series FPGAs – ACT 3 Family

PG100		
A1415 Function	Location	
CLKA or I/O	C7	
CLKB or I/O	D6	
DCLK or I/O	C4	
GND	C3, C6, C9, E9, F3, F9, J3, J6, J8, J9	
HCLK or I/O	H6	
IOCLK or I/O	C10	
IOPCL or I/O	К9	
MODE	C2	
PRA or I/O	A6	
PRB or I/O	L3	
SDI or I/O	B3	
SDO	L9	
VCC	B6, B10, E11, F2, F10, G2, K2, K6, K10	

- 1. All unlisted pin numbers are user I/Os.
- 2. NC denotes no connection.
- 3. MODE should be terminated to GND through a 10K resistor to enable Actionprobe usage; otherwise it can be terminated directly to GND.
- 4. The PG100 package has been discontinued.



Package Pin Assignments

PG175



Note: This is the top view.

Note

Accelerator Series FPGAs – ACT 3 Family

PG175		
A1440 Function	Location	
CLKA or I/O	C9	
CLKB or I/O	A9	
DCLK or I/O	D5	
GND	D4, D8, D11, D12, E4, E14, H4, H12, L4, L12, M4, M8, M12	
HCLK or I/O	R8	
IOCLK or I/O	E12	
IOPCL or I/O	P13	
MODE	F3	
NC	A1, A2, A15, B2, B3, P2, P14, R1, R2, R14, R15	
PRA or I/O	B8	
PRB or I/O	R7	
SDI or I/O	D3	
SDO	N12	
VCC	C3, C8, C13, E15, H3, H13, L1, L14, N3, N8, N13	

- 1. All unlisted pin numbers are user I/Os.
- 2. NC denotes no connection.
- 3. MODE should be terminated to GND through a 10K resistor to enable Actionprobe usage; otherwise it can be terminated directly to GND.
- 4. The PG175 package has been discontinued.

4 – Datasheet Information

List of Changes

The following table lists critical changes that were made in each version of the datasheet.

Revision	Changes	Page
Revision 3 (January 2012)	The description for SDO pins had earlier been removed from the datasheet and has now been included again, in the "Pin Descriptions" section (SAR 35820).	
	SDO pin numbers had earlier been removed from package pin assignment tables in the datasheet, and have now been restored to the pin tables (SAR 35820).	3-1
Revision 2 (September 2011)	The ACT 3 datasheet was formatted newly in the style used for current datasheets. The same information is present (other than noted in the list of changes for this revision) but divided into chapters.	N/A
	The datasheet was revised to note in multiple places that speed grades -2 and -3 have been discontinued. The following device/package combinations have been discontinued for all speed grades and temperatures (SAR 33872): A1415 PG100 A1425 PG133 A1440 PG175 A1460 BG225 Refer to PDN 0104, PDN 0203, PDN 0604, and PDN 1004.	l and others
	The "Features" section was revised to state the clock-to-ouput time and on-chip performance for -1 speed grade as 9.0 ns and 186 MHz. The "General Description" section was revised in accordance (SAR 33872).	I
	The maximum performance values were updated in Table 1 \cdot ACT 3 Family Product Information, and now reflect worst-case commercial for the -1 speed grade (SAR 33872).	I
	The "Product Plan" table was updated as follows to conform to current offerings (SAR 33872): The A1415A device is offered in PL84, PG100, and VQ100 packages for Military application. The A1440A device is offered in TQ176 and VQ100 packages for Industrial application.	Ξ
	Table 1-1 • Chip-to-Chip Performance (worst-case commercial) was updated to include data for all speed grades instead of only –3 (SAR 33872).	1-2
	Figure 1-1 • Predictable Performance (worst-case commercial, –1 speed grade) was revised to reflect values for the –1 speed grade (SAR 33872).	1-1
	Figure 2-10 • Timing Model was updated to show data for the -1 speed grade instead of -3 (SAR 33872).	2-16
	Table 2-14 • Logic Module and Routing Delay by Fanout (ns); Worst-Case Commercial Conditions was updated to include data for all speed grades instead of only –3 (SAR 33872).	2-20
	Package names used in the "Package Pin Assignments" section and throughout the document were revised to match standards given in <i>Package Mechanical Drawings</i> (SAR 27395).	3-1

Datasheet Categories

Categories

In order to provide the latest information to designers, some datasheet parameters are published before data has been fully characterized from silicon devices. The data provided for a given device is designated as either "Product Brief," "Advance," "Preliminary," or "Production." The definitions of these categories are as follows:

Product Brief

The product brief is a summarized version of a datasheet (advance or production) and contains general product information. This document gives an overview of specific device and family information.

Advance

This version contains initial estimated information based on simulation, other products, devices, or speed grades. This information can be used as estimates, but not for production. This label only applies to the DC and Switching Characteristics chapter of the datasheet and will only be used when the data has not been fully characterized.

Preliminary

The datasheet contains information based on simulation and/or initial characterization. The information is believed to be correct, but changes are possible.

Production

This version contains information that is considered to be final.

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