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Understanding <u>Embedded - FPGAs (Field</u> <u>Programmable Gate Array)</u>

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

2 0 0 0 0 0	
Product Status	Obsolete
Number of LABs/CLBs	564
Number of Logic Elements/Cells	-
Total RAM Bits	-
Number of I/O	100
Number of Gates	4000
Voltage - Supply	4.5V ~ 5.5V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 70°C (TA)
Package / Case	160-BQFP
Supplier Device Package	160-PQFP (28x28)
Purchase URL	https://www.e-xfl.com/product-detail/microsemi/a1440a-1pq160c

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

Microsemi

Accelerator Series FPGAs – ACT 3 Family

		Speed	Grade ¹		Application ¹				
Device/Package	Std.	-1	-2	-3	С	I	м	В	
A14V40A Device							•		
84-Pin Plastic Leaded Chip Carrier (PLCC)	1	-	-	_	1	_	_	_	
100-Pin Very Thin Quad Flatpack (VQFP)	1	-	-	-	1	-	-	-	
160-Pin Plastic Quad Flatpack (PQFP)	~	-	-	-	✓	-	-	-	
176-Pin Thin Quad Flatpack (TQFP)	✓	-	-	-	✓	-	-	-	
A1460A Device		•		I			1		
160-Pin Plastic Quad Flatpack (PQFP)	✓	✓	D	D	1	~	-	-	
176-Pin Thin Quad Flatpack (TQFP)	✓	~	D	D	✓	✓	-	-	
196-Pin Ceramic Quad Flatpack (CQFP)	1	1	-	_	1	-	1	1	
207-Pin Ceramic Pin Grid Array (CPGA)	1	1	D	D	1	-	1	1	
208-Pin Plastic Quad Flatpack (PQFP)	1	 ✓ 	D	D	1	1	-	_	
225-Pin Plastic Ball Grid Array (BGA)	D	D	D	D	D	-	-	-	
A14V60A Device					-		-		
160-Pin Plastic Quad Flatpack (PQFP)	~	-	-	_	~	-	_	-	
176-Pin Thin Quad Flatpack (TQFP)	✓	-	-	-	1	-	-	-	
208-Pin Plastic Quad Flatpack (PQFP)	✓	-	-	_	~	-	_	_	
A14100A Device									
208-Pin Power Quad Flatpack (RQFP)	✓	~	D	D	~	~	_	_	
257-Pin Ceramic Pin Grid Array (CPGA)	✓	~	D	D	~	-	~	~	
313-Pin Plastic Ball Grid Array (BGA)	✓	~	D	D	~	-	_	-	
256-Pin Ceramic Quad Flatpack (CQFP)	✓	~	-	_	~	-	~	~	
A14V100A Device									
208-Pin Power Quad Flatpack (RQFP)	\checkmark	_	_	_	1	_	_	_	
313-Pin Plastic Ball Grid Array (BGA)	✓	-	-	-	1	-	-	-	

Notes:

1. Applications: C = CommercialI = Industrial
M = Military
Commercial only

- Availability:
- ✓ = Available
- P = Planned- = Not planned
- D = Discontinued

Speed Grade:

-1 = Approx. 15% faster than Std. -2 = Approx. 25% faster than Std. -3 = Approx. 35% faster than Std. (-2 and -3 speed grades have been discontinued.)

1 – ACT 3 Family Overview

General Description

Microsemi's ACT 3 Accelerator Series of FPGAs offers the industry's fastest high-capacity programmable logic device. ACT 3 FPGAs offer a high performance, PCI compliant programmable solution capable of 186 MHz on-chip performance and 9.0 nanosecond clock-to-output (-1 speed grade), with capacities spanning from 1,500 to 10,000 gate array equivalent gates.

The ACT 3 family builds on the proven two-module architecture consisting of combinatorial and sequential logic modules used in Microsemi's 3200DX and 1200XL families. In addition, the ACT 3 I/O modules contain registers which deliver 9.0 nanosecond clock-to-out times (-1 speed grade). The devices contain four clock distribution networks, including dedicated array and I/O clocks, supporting very fast synchronous and asynchronous designs. In addition, routed clocks can be used to drive high fanout signals such as flip-flop resets and output.

The ACT 3 family is supported by Microsemi's Designer Series Development System which offers automatic placement and routing (with automatic or fixed pin assignments), static timing analysis, user programming, and debug and diagnostic probe capabilities.



Figure 1-1 • Predictable Performance (worst-case commercial, –1 speed grade)

System Performance Model



This section of the datasheet is meant to familiarize the user with the architecture of the ACT 3 family of FPGA devices. A generic description of the family will be presented first, followed by a detailed description of the logic blocks, the routing structure, the antifuses, and the special function circuits. The on-chip circuitry required to program the devices is not covered.

Topology

The ACT 3 family architecture is composed of six key elements: Logic modules, I/O modules, I/O Pad Drivers, Routing Tracks, Clock Networks, and Programming and Test Circuits. The basic structure is similar for all devices in the family, differing only in the number of rows, columns, and I/Os. The array itself consists of alternating rows of modules and channels. The logic modules and channels are in the center of the array; the I/O modules are located along the array periphery. A simplified floor plan is depicted in Figure 2-1.



Figure 2-1 • Generalized Floor Plan of ACT 3 Device



Logic Modules

ACT 3 logic modules are enhanced versions of the 1200XL family logic modules. As in the 1200XL family, there are two types of modules: C-modules and S-modules (Figure 2-2 and Figure 2-3). The C-module is functionally equivalent to the 1200XL C-module and implements high fanin combinatorial macros, such as 5-input AND, 5-input OR, and so on. It is available for use as the CM8 hard macro. The S-module is designed to implement high-speed sequential functions within a single module.







Figure 2-3 • S-Module Diagram

S-modules consist of a full C-module driving a flip-flop, which allows an additional level of logic to be implemented without additional propagation delay. It is available for use as the DFM8A/B and DLM8A/B hard macros. C-modules and S-modules are arranged in pairs called module-pairs. Module-pairs are arranged in alternating patterns and make up the bulk of the array. This arrangement allows the placement software to support two-module macros of four types (CC, CS, SC, and SS). The C-module implements the following function:

EQ 1

where: S0 = A0 * B0 and S1 = A1 + B1

Accelerator Series FPGAs – ACT 3 Family

Equivalent capacitance is calculated by measuring ICC active at a specified frequency and voltage for each circuit component of interest. Measurements have been made over a range of frequencies at a fixed value of VCC. Equivalent capacitance is frequency independent so that the results may be used over a wide range of operating conditions. Equivalent capacitance values are shown in Figure 2-10.

Item	CEQ Value
Modules (C _{EQM})	6.7
Input Buffers (C _{EQI})	7.2
Output Buffers (C _{EQO})	10.4
Routed Array Clock Buffer Loads (C _{EQCR})	1.6
Dedicated Clock Buffer Loads (C _{EQCD})	0.7
I/O Clock Buffer Loads (C _{EQCI)}	0.9

To calculate the active power dissipated from the complete design, the switching frequency of each part of the logic must be known. EQ 5 shows a piece-wise linear summation over all components.

Power =VCC² * [(m * C_{EQM} * f_m)_{modules} + (n * C_{EQI} * f_n) inputs

+ ($p * (C_{EQO} + C_L) * f_p$)outputs

+ 0.5 * (q1 * C_{EQCR} * f_{q1})_{routed_Clk1} + (r1 * fq1)_{routed_Clk1}

+ 0.5 * (q2 * C_{EQCR} * fq2)_{routed_Clk2}

+ $(r_2 * f_{q2})_{routed_Clk2}$ + 0.5 * $(s_1 * C_{EQCD} * f_{s1})_{dedicated_Clk}$

+ (s₂ * C_{EQCI} * f_{s2})_{IO_CIk}]

Where: m = Number of logic modules switching at fm n = Number of input buffers switching at fn p = Number of output buffers switching at f_p q1 = Number of clock loads on the first routed array clock q2 = Number of clock loads on the second routed array clock r_1 = Fixed capacitance due to first routed array clock r₂ = Fixed capacitance due to second routed array clock s₁ = Fixed number of clock loads on the dedicated array clock s2 = Fixed number of clock loads on the dedicated I/O clock C_{FOM} = Equivalent capacitance of logic modules in pF C_{EQI} = Equivalent capacitance of input buffers in pF C_{EOO} = Equivalent capacitance of output buffers in pF C_{EOCR} = Equivalent capacitance of routed array clock in pF C_{EQCD} = Equivalent capacitance of dedicated array clock in pF C_{EOCI} = Equivalent capacitance of dedicated I/O clock in pF C₁ = Output lead capacitance in pF f_m = Average logic module switching rate in MHz fn = Average input buffer switching rate in MHz f_p = Average output buffer switching rate in MHz f_{q1} = Average first routed array clock rate in MHz $f_{\alpha 2}$ = Average second routed array clock rate in MHz f_{s1} = Average dedicated array clock rate in MHz f_{s2} = Average dedicated I/O clock rate in MHz

EQ 5

Determining Average Switching Frequency

To determine the switching frequency for a design, you must have a detailed understanding of the data input values to the circuit. The following guidelines are meant to represent worst-case scenarios so that they can be generally used to predict the upper limits of power dissipation. These guidelines are as follows:

Tahle	2-13	Guidelines	for	Predicting	Power	Dissination
lable	2-13	Ouldennes	101	rieuleung	I OWEI	Dissipation

Data	Value
Logic Modules (m)	80% of modules
Inputs switching (n)	# inputs/4
Outputs switching (p)	# output/4
First routed array clock loads (q1)	40% of sequential modules
Second routed array clock loads (q2)	40% of sequential modules
Load capacitance (CL)	35 pF
Average logic module switching rate (fm)	F/10
Average input switching rate (fn)	F/5
Average output switching rate (fp)	F/10
Average first routed array clock rate (fq1)	F/2
Average second routed array clock rate (fq2)	F/2
Average dedicated array clock rate (fs1)	F
Average dedicated I/O clock rate (fs2)	F



ACT 3 Timing Model



Note: Values shown for A1425A –1 speed grade device.

Figure 2-10 • Timing Model







Figure 2-14 • Module Delays



Figure 2-15 • Sequential Module Timing Characteristics

Accelerator Series FPGAs – ACT 3 Family







Figure 2-17 • I/O Module: Sequential Output Timing Characteristics

Timing Derating

ACT 3 devices are manufactured in a CMOS process. Therefore, device performance varies according to temperature, voltage, and process variations. Minimum timing parameters reflect maximum operating voltage, minimum operating temperature, and best-case processing. Maximum timing parameters reflect minimum operating voltage, maximum operating temperature, and worst-case processing.

Table 2-15 • Timing Derating Factor (Temperature and Voltage)

(Commercial Minimum/Maximum Specification) x	Indus	strial	Mili	tary
	Min.	Max.	Min.	Max.
	0.66	1.07	0.63	1.17

Table 2-16 • Timing Derating Factor for Designs at Typical Temperature ($T_J = 25^{\circ}C$) and Voltage (5.0 V)

(Commercial Maximum Specification) x	0.85

Table 2-17 • Temperature and Voltage Derating Factors

(normalized to Worst-Case Commercial, TJ = 4.75 V, 70°C)

	-55	-40	0	25	70	85	125
4.50	0.72	0.76	0.85	0.90	1.04	1.07	1.117
4.75	0.70	0.73	0.82	0.87	1.00	1.03	1.12
5.00	0.68	0.71	0.79	0.84	0.97	1.00	1.09
5.25	0.66	0.69	0.77	0.82	0.94	0.97	1.06
5.50	0.63	0.66	0.74	0.79	0.90	0.93	1.01



Note: This derating factor applies to all routing and propagation delays.



A1415A, A14V15A Timing Characteristics (continued)

Table 2-21 • A1415A, A14V15A Worst-Case Commercial Conditions, VCC = 4.75 V, T_J = 70°C

Dedicated (hardwired) I/O Clock Network		-3 Speed		-2 Speed		-1 Speed		Std. Speed		3.3 V Speed ¹		Units
Paramete	er/Description	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t _{IOCKH}	Input Low to High (pad to I/O module input)		2.0		2.3		2.6		3.0		3.5	ns
t _{IOPWH}	Minimum Pulse Width High	1.9		2.4		3.3		3.8		4.8		ns
t _{IPOWL}	Minimum Pulse Width Low	1.9		2.4		3.3		3.8		4.8		ns
t _{IOSAPW}	Minimum Asynchronous Pulse Width	1.9		2.4		3.3		3.8		4.8		ns
t _{IOCKSW}	Maximum Skew		0.4		0.4		0.4		0.4		0.4	ns
t _{IOP}	Minimum Period	4.0		5.0		6.8		8.0		10.0		ns
f _{IOMAX}	Maximum Frequency		250		200		150		125		100	MHz
Dedicate	d (hardwired) Array Clock			•			•					
^t нскн	Input Low to High (pad to S-module input)		3.0		3.4		3.9		4.5		5.5	ns
t _{HCKL}	Input High to Low (pad to S-module input)		3.0		3.4		3.9		4.5		5.5	ns
t _{HPWH}	Minimum Pulse Width High	1.9		2.4		3.3		3.8		4.8		ns
t _{HPWL}	Minimum Pulse Width Low	1.9		2.4		3.3		3.8		4.8		ns
t _{HCKSW}	Delta High to Low, Low Slew		0.3		0.3		0.3		0.3		0.3	ns
t _{HP}	Minimum Period	4.0		5.0		6.8		8.0		10.0		ns
f _{HMAX}	Maximum Frequency		250		200		150		125		100	MHz
Routed A	rray Clock Networks			-								
t _{RCKH}	Input Low to High (FO = 64)		3.7		4.1		4.7		5.5		9.0	ns
t _{RCKL}	Input High to Low (FO = 64)		4.0		4.5		5.1		6.0		9.0	ns
t _{RPWH}	Min. Pulse Width High (FO = 64)	3.3		3.8		4.2		4.9		6.5		ns
t _{RPWL}	Min. Pulse Width Low (FO = 64)	3.3		3.8		4.2		4.9		6.5		ns
t _{RCKSW}	Maximum Skew (FO = 128)		0.7		0.8		0.9		1.0		1.0	ns
t _{RP}	Minimum Period (FO = 64)	6.8		8.0		8.7		10.0		13.4		ns
f _{RMAX}	Maximum Frequency (FO = 64)		150		125		115		100		75	MHz
Clock-to-Clock Skews												
t _{IOHCKSW}	I/O Clock to H-Clock Skew	0.0	1.7	0.0	1.8	0.0	2.0	0.0	2.2	0.0	3.0	ns
t _{IORCKS} W	I/O Clock to R-Clock Skew (FO = 64)	0.0	1.0	0.0	1.0	0.0	1.0	0.0	1.0	0.0	3.0	ns
t _{HRCKSW}	H-Clock to R-Clock Skew (FO = 64) (FO = 50% maximum)	0.0	1.0	0.0	1.0	0.0	1.0	0.0	1.0	0.0 0.0	3.0 3.0	ns

Notes:

1. Delays based on 35 pF loading.

2. The –2 and –3 speed grades have been discontinued. Refer to PDN 0104, PDN 0203, PDN 0604, and PDN 1004 at http://www.microsemi.com/soc/support/notifications/default.aspx#pdn.

A1425A, A14V25A Timing Characteristics (continued)

Table 2-25 • A1425A	414V254 W	lorst-Case (Conditions	VCC - 4 75 \	/ T 70°C
<i>Table 2-25 • A</i> 1425A,	AI4VZJA W	UISI-Case C	Jonnierciai	conunons,	VCC = 4.75	, ij = 70 C

Dedicated (hardwired) I/O Clock Network		-3 Speed ¹		–2 Speed ¹		-1 Speed		Std. Speed		3.3 V Speed ¹		Units
Paramete	er/Description	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t _{IOCKH}	Input Low to High (pad to I/O module input)		2.0		2.3		2.6		3.0		3.5	ns
t _{IOPWH}	Minimum Pulse Width High	1.9		2.4		3.3		3.8		4.8		ns
t _{IPOWL}	Minimum Pulse Width Low	1.9		2.4		3.3		3.8		4.8		ns
t _{IOSAPW}	Minimum Asynchronous Pulse Width	1.9		2.4		3.3		3.8		4.8		ns
t _{IOCKSW}	Maximum Skew		0.4		0.4		0.4		0.4		0.4	ns
t _{IOP}	Minimum Period	4.0		5.0		6.8		8.0		10.0		ns
f _{IOMAX}	Maximum Frequency		250		200		150		125		100	MHz
Dedicate	d (hardwired) Array Clock							-				
t _{нскн}	Input Low to High (pad to S-module input)		3.0		3.4		3.9		4.5		5.5	ns
t _{HCKL}	Input High to Low (pad to S-module input)		3.0		3.4		3.9		4.5		5.5	ns
t _{HPWH}	Minimum Pulse Width High	1.9		2.4		3.3		3.8		4.8		ns
t _{HPWL}	Minimum Pulse Width Low	1.9		2.4		3.3		3.8		4.8		ns
t _{HCKSW}	Delta High to Low, Low Slew		0.3		0.3		0.3		0.3		0.3	ns
t _{HP}	Minimum Period	4.0		5.0		6.8		8.0		10.0		ns
f _{HMAX}	Maximum Frequency		250		200		150		125		100	MHz
Routed A	rray Clock Networks			•			•	•				
t _{RCKH}	Input Low to High (FO = 64)		3.7		4.1		4.7		5.5		9.0	ns
t _{RCKL}	Input High to Low (FO = 64)		4.0		4.5		5.1		6.0		9.0	ns
t _{RPWH}	Min. Pulse Width High (FO = 64)	3.3		3.8		4.2		4.9		6.5		ns
t _{RPWL}	Min. Pulse Width Low (FO = 64)	3.3		3.8		4.2		4.9		6.5		ns
t _{RCKSW}	Maximum Skew (FO = 128)		0.7		0.8		0.9		1.0		1.0	ns
t _{RP}	Minimum Period (FO = 64)	6.8		8.0		8.7		10.0		13.4		ns
f _{RMAX}	Maximum Frequency (FO = 64)		150		125		115		100		75	MHz
Clock-to-	Clock Skews							-				
t _{IOHCKSW}	I/O Clock to H-Clock Skew	0.0	1.7	0.0	1.8	0.0	2.0	0.0	2.2	0.0	3.0	ns
t _{IORCKSW}	I/O Clock to R-Clock Skew (FO = 64) (FO = 80)	0.0 0.0	1.0 3.0	0.0 0.0	1.0 3.0	0.0 0.0	1.0 3.0	0.0 0.0	1.0 3.0	0.0 0.0	3.0 3.0	ns
t _{HRCKSW}	H-Clock to R-Clock Skew (FO = 64) (FO = 80)	0.0 0.0	1.0 3.0	0.0 0.0	1.0 3.0	0.0 0.0	1.0 3.0	0.0 0.0	1.0 3.0	0.0 0.0	1.0 3.0	ns

Notes:

1. The -2 and -3 speed grades have been discontinued. Refer to PDN 0104, PDN 0203, PDN 0604, and PDN 1004 at http://www.microsemi.com/soc/support/notifications/default.aspx#pdn.

2. Delays based on 35 pF loading.



A1460A, A14V60A Timing Characteristics (continued)

Table 2-32 • A1460A, A14V60A Worst-Case Commercial Conditions, VCC = 4.75 V, T_J = 70°C

I/O Module – TTL Output Timing ¹		-3 Speed ² -		–2 Speed ²		-1 Speed		Std. Speed		3.3 V Speed ¹		Units
Parameter/Description		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t _{DHS}	Data to Pad, High Slew		5.0		5.6		6.4		7.5		9.8	ns
t _{DLS}	Data to Pad, Low Slew		8.0		9.0		10.2		12.0		15.6	ns
t _{ENZHS}	Enable to Pad, Z to H/L, High Slew		4.0		4.5		5.1		6.0		7.8	ns
t _{ENZLS}	Enable to Pad, Z to H/L, Low Slew		7.4		8.3		9.4		11.0		14.3	ns
t _{ENHSZ}	Enable to Pad, H/L to Z, High Slew		7.8		8.7		9.9		11.6		15.1	ns
t _{ENLSZ}	Enable to Pad, H/L to Z, Low Slew		7.4		8.3		9.4		11.0		14.3	ns
t _{CKHS}	IOCLK Pad to Pad H/L, High Slew		9.0		9.0		10.0		11.5		15.0	ns
t _{CKLS}	IOCLK Pad to Pad H/L, Low Slew		12.8		12.8		15.3		17.0		22.1	ns
d _{TLHHS}	Delta Low to High, High Slew		0.02		0.02		0.03		0.03		0.04	ns/pF
d _{TLHLS}	Delta Low to High, Low Slew		0.05		0.05		0.06		0.07		0.09	ns/pF
d _{THLHS}	Delta High to Low, High Slew		0.04		0.04		0.04		0.05		0.07	ns/pF
d _{THLLS}	Delta High to Low, Low Slew		0.05		0.05		0.06		0.07		0.09	ns/pF
I/O Mod	I/O Module – CMOS Output Timing ¹											
t _{DHS}	Data to Pad, High Slew		6.2		7.0		7.9		9.3		12.1	ns
t _{DLS}	Data to Pad, Low Slew		11.7		13.1		14.9		17.5		22.8	ns
t _{ENZHS}	Enable to Pad, Z to H/L, High Slew		5.2		5.9		6.6		7.8		10.1	ns
t _{ENZLS}	Enable to Pad, Z to H/L, Low Slew		8.9		10.0		11.3		13.3		17.3	ns
t _{ENHSZ}	Enable to Pad, H/L to Z, High Slew		7.4		8.3		9.4		11.0		14.3	ns
t _{ENLSZ}	Enable to Pad, H/L to Z, Low Slew		7.4		8.3		9.4		11.0		14.3	ns
t _{CKHS}	IOCLK Pad to Pad H/L, High Slew		10.4		10.4		12.1		13.8		17.9	ns
t _{CKLS}	IOCLK Pad to Pad H/L, Low Slew		14.5		14.5		17.4		19.3		25.1	ns
d _{TLHHS}	Delta Low to High, High Slew		0.04		0.04		0.05		0.06		0.08	ns/pF
d _{TLHLS}	Delta Low to High, Low Slew		0.07		0.08		0.09		0.11		0.14	ns/pF
d _{THLHS}	Delta High to Low, High Slew		0.03		0.03		0.03		0.04		0.05	ns/pF
d _{THLLS}	Delta High to Low, Low Slew		0.04		0.04		0.04		0.05		0.07	ns/pF

Notes:

1. Delays based on 35 pF loading.

2. The –2 and –3 speed grades have been discontinued. Refer to PDN 0104, PDN 0203, PDN 0604, and PDN 1004 at http://www.microsemi.com/soc/support/notifications/default.aspx#pdn.



A14100A, A14V100A Timing Characteristics

Logic N	-3 Speed ³		-2 Speed ³		-1 Speed		Std. Speed		3.3 V Speed ¹		Units	
Parameter/Description		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t _{PD}	Internal Array Module		2.0		2.3		2.6		3.0		3.9	ns
t _{CO}	Sequential Clock to Q		2.0		2.3		2.6		3.0		3.9	ns
t _{CLR}	Asynchronous Clear to Q		2.0		2.3		2.6		3.0		3.9	ns
Predict	Predicted Routing Delays ⁴											
t _{RD1}	FO = 1 Routing Delay		0.9		1.0		1.1		1.3		1.7	ns
t _{RD2}	FO = 2 Routing Delay		1.2		1.4		1.6		1.8		2.4	ns
t _{RD3}	FO = 3 Routing Delay		1.4		1.6		1.8		2.1		2.8	ns
t _{RD4}	FO = 4 Routing Delay		1.7		1.9		2.2		2.5		3.3	ns
t _{RD8}	FO = 8 Routing Delay		2.8		3.2		3.6		4.2		5.5	ns
Logic N	Logic Module Sequential Timing											
t _{SUD}	Flip-Flop Data Input Setup	0.5		0.6		0.8		0.8		0.8		ns
t _{HD}	Flip-Flop Data Input Hold	0.0		0.0		0.5		0.5		0.5		ns
t _{SUD}	Latch Data Input Setup	0.5		0.6		0.8		0.8		0.8		ns
t _{HD}	Latch Data Input Hold	0.0		0.0		0.5		0.5		0.5		ns
t _{WASYN}	Asynchronous Pulse Width	2.4		3.2		3.8		4.8		6.5		ns
t _{WCLKA}	Flip-Flop Clock Pulse Width	2.4		3.2		3.8		4.8		6.5		ns
t _A	Flip-Flop Clock Input Period	5.0		6.8		8.0		10.0		13.4		ns
f _{MAX}	Flip-Flop Clock Frequency		200		150		125		100		75	MHz

Notes:

1. VCC = 3.0 V for 3.3 V specifications.

2. For dual-module macros, use $t_{PD} + t_{RD1} + t_{PDn} + t_{CO} + t_{RD1} + t_{PDn}$ or $t_{PD1} + t_{RD1} + t_{SUD}$, whichever is appropriate.

3. The –2 and –3 speed grades have been discontinued. Refer to PDN 0104, PDN 0203, PDN 0604, and PDN 1004 at http://www.microsemi.com/soc/support/notifications/default.aspx#pdn.

4. Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual worst-case performance. Post-route timing is based on actual routing delay measurements performed on the device prior to shipment.



Package Pin Assignments

CQ196



Note: This is the top view.

Note

For Package Manufacturing and Environmental information, visit the Resource Center at http://www.microsemi.com/soc/products/solutions/package/docs.aspx

Microsemi

Accelerator Series FPGAs - ACT 3 Family

	CQ196	CQ196				
Pin Number	A1460 Function	Pin Number	A1460 Function			
1	GND	101	GND			
2	SDI, I/O	110	VCC			
11	MODE	111	VCC			
12	VCC	112	GND			
13	GND	137	VCC			
37	GND	138	GND			
38	VCC	139	GND			
39	VCC	140	VCC			
51	GND	148	IOCLK, I/O			
52	GND	149	GND			
59	VCC	155	VCC			
64	GND	162	GND			
77	HCLK, I/O	172	CLKA, I/O			
79	PRB, I/O	173	CLKB, I/O			
86	GND	174	PRA, I/O			
94	VCC	183	GND			
98	GND	189	VCC			
99	SDO	193	GND			
100	IOPCL, I/O	196	DCLK, I/O			

Notes:

- 1. All unlisted pin numbers are user I/Os.
- 2. NC denotes no connection.
- 3. MODE should be terminated to GND through a 10K resistor to enable Actionprobe usage; otherwise it can be terminated directly to GND.

Microsemi.

Package Pin Assignments

BG225



Note: This is the top view.

Note

For Package Manufacturing and Environmental information, visit the Resource Center at http://www.microsemi.com/soc/products/solutions/package/docs.aspx



Package Pin Assignments

PG133



Note: This is the top view.

Note

For Package Manufacturing and Environmental information, visit the Resource Center at http://www.microsemi.com/soc/products/solutions/package/docs.aspx

Microsemi

Accelerator Series FPGAs – ACT 3 Family

PG175				
A1440 Function	Location			
CLKA or I/O	C9			
CLKB or I/O	A9			
DCLK or I/O	D5			
GND	D4, D8, D11, D12, E4, E14, H4, H12, L4, L12, M4, M8, M12			
HCLK or I/O	R8			
IOCLK or I/O	E12			
IOPCL or I/O	P13			
MODE	F3			
NC	A1, A2, A15, B2, B3, P2, P14, R1, R2, R14, R15			
PRA or I/O	B8			
PRB or I/O	R7			
SDI or I/O	D3			
SDO	N12			
VCC	C3, C8, C13, E15, H3, H13, L1, L14, N3, N8, N13			

Notes:

- 1. All unlisted pin numbers are user I/Os.
- 2. NC denotes no connection.
- 3. MODE should be terminated to GND through a 10K resistor to enable Actionprobe usage; otherwise it can be terminated directly to GND.
- 4. The PG175 package has been discontinued.