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Understanding **Embedded - FPGAs (Field Programmable Gate Array)**

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications,

Details	
Product Status	Obsolete
Number of LABs/CLBs	564
Number of Logic Elements/Cells	-
Total RAM Bits	-
Number of I/O	140
Number of Gates	4000
Voltage - Supply	4.5V ~ 5.5V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 70°C (TA)
Package / Case	176-LQFP
Supplier Device Package	176-TQFP (24x24)
Purchase URL	https://www.e-xfl.com/product-detail/microsemi/a1440a-1tq176c

Product Plan

Device/Package	Speed Grade[1]				Application[1]			
	Std.	–1	–2	–3	C	I	M	B
A1415A Device								
84-Pin Plastic Leaded Chip Carrier (PLCC)	✓	✓	D	D	✓	✓	✓	–
100-Pin Plastic Quad Flatpack (PQFP)	✓	✓	D	D	✓	✓	✓	–
100-Pin Very Thin Quad Flatpack (VQFP)	✓	✓	D	D	✓	✓	✓	–
100-Pin Ceramic Pin Grid Array (CPGA)	D	D	D	D	D	–	–	–
A14V15A Device								
84-Pin Plastic Leaded Chip Carrier (PLCC)	✓	–	–	–	✓	–	–	–
100-Pin Very Thin Quad Flatpack (VQFP)	✓	–	–	–	✓	–	–	–
A1425A Device								
84-Pin Plastic Leaded Chip Carrier (PLCC)	✓	✓	D	D	✓	✓		
100-Pin Plastic Quad Flatpack (PQFP)	✓	✓	D	D	✓	✓	–	–
100-Pin Very Thin Quad Flatpack (VQFP)	✓	✓	D	D	✓	✓	–	–
132-Pin Ceramic Quad Flatpack (CQFP)	✓	✓	–	–	✓	–	✓	✓
133-Pin Ceramic Pin Grid Array (CPGA)	D	D	D	D	D	–	D	D
160-Pin Plastic Quad Flatpack (PQFP)	✓	✓	D	D	✓	✓	–	–
A14V25A Device								
84-Pin Plastic Leaded Chip Carrier (PLCC)	✓	–	–	–	✓	–	–	–
100-Pin Very Thin Quad Flatpack (VQFP)	✓	–	–	–	✓	–	–	–
160-Pin Plastic Quad Flatpack (PQFP)	✓	–	–	–	✓	–	–	–
A1440A Device								
84-Pin Plastic Leaded Chip Carrier (PLCC)	✓	✓	D	D	✓	✓	–	–
100-Pin Very Thin Quad Flatpack (VQFP)	✓	✓	D	D	✓	✓	–	–
160-Pin Plastic Quad Flatpack (PQFP)	✓	✓	D	D	✓	✓	–	–
175-Pin Ceramic Pin Grid Array (CPGA)	D	D	D	D	D	–	–	–
176-Pin Thin Quad Flatpack (TQFP)	✓	✓	D	D	✓	✓	–	–

Notes:

1. *Applications:*
   C = Commercial
   I = Industrial
   M = Military
2. *Commercial only*

Availability:
✓ = Available
P = Planned
– = Not planned
D = Discontinued

Speed Grade:
–1 = Approx. 15% faster than Std.
–2 = Approx. 25% faster than Std.
–3 = Approx. 35% faster than Std.
(–2 and –3 speed grades have been discontinued.)

Table 1-1 • **Chip-to-Chip Performance (worst-case commercial)**

Device and Speed Grade	t_{CKHS} (ns)	t_{TRACE} (ns)	t_{INSU} (ns)	Total (ns)	MHz
A1425A -3	7.5	1.0	1.8	10.3	97
A1460A -3	9.0	1.0	1.3	11.3	88
A1425A -2	7.5	1.0	2.0	10.5	95
A1460A -2	9.0	1.0	1.5	11.5	87
A1425A -1	9.0	1.0	2.3	12.3	81
A1460A -1	10.0	1.0	1.8	12.8	78
A1425A STD	10.0	1.0	2.7	13.7	73
A1460A STD	11.5	1.0	2.0	14.5	69

Note: The –2 and –3 speed grades have been discontinued. Refer to PDN 0104, PDN 0203, PDN 0604, and PDN 1004 at http://www.microsemi.com/soc/support/notifications/default.aspx#pdn.

2 – Detailed Specifications

This section of the datasheet is meant to familiarize the user with the architecture of the ACT 3 family of FPGA devices. A generic description of the family will be presented first, followed by a detailed description of the logic blocks, the routing structure, the antifuses, and the special function circuits. The on-chip circuitry required to program the devices is not covered.

Topology

The ACT 3 family architecture is composed of six key elements: Logic modules, I/O modules, I/O Pad Drivers, Routing Tracks, Clock Networks, and Programming and Test Circuits. The basic structure is similar for all devices in the family, differing only in the number of rows, columns, and I/Os. The array itself consists of alternating rows of modules and channels. The logic modules and channels are in the center of the array; the I/O modules are located along the array periphery. A simplified floor plan is depicted in Figure 2-1.
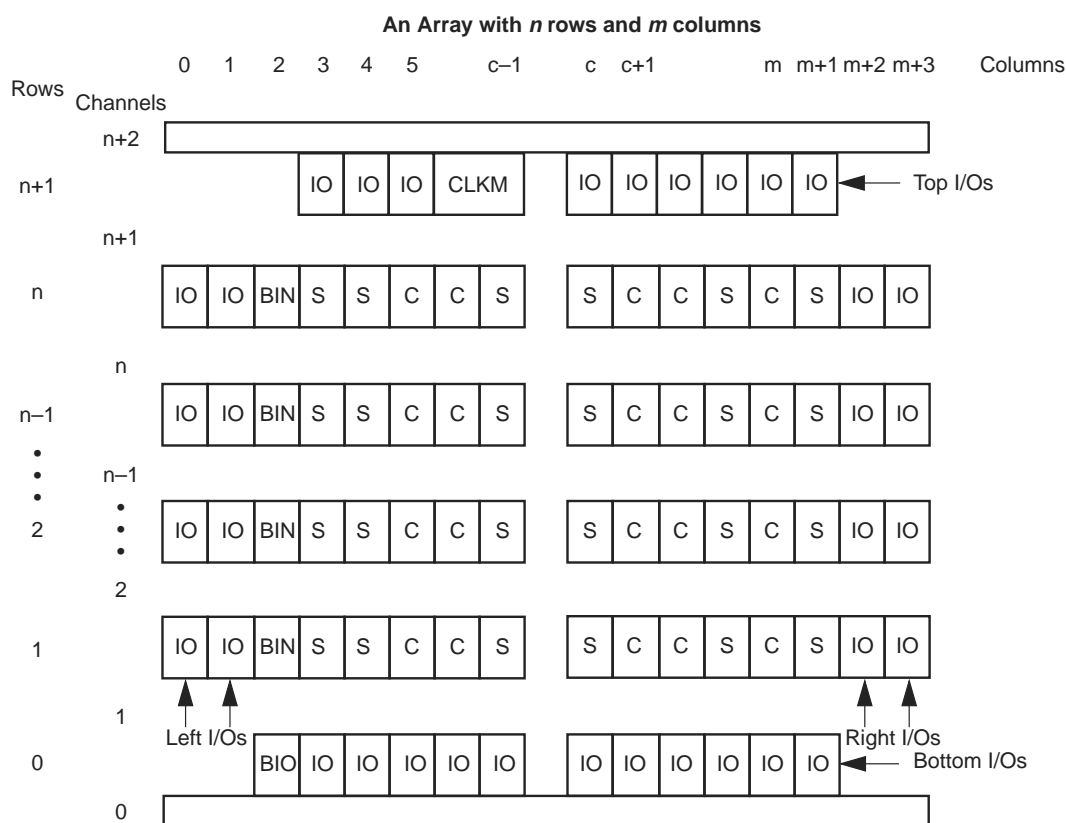

Figure 2-1 • **Generalized Floor Plan of ACT 3 Device**

The I/O module output Y is used to bring Pad signals into the array or to feed the output register back into the array. This allows the output register to be used in high-speed state machine applications. Side I/O modules have a dedicated output segment for Y extending into the routing channels above and below (similar to logic modules). Top/Bottom I/O modules have no dedicated output segment. Signals coming into the chip from the top or bottom are routed using F-fuses and LVTs (F-fuses and LVTs are explained in detail in the routing section).

I/O Pad Drivers

All pad drivers are capable of being tristate. Each buffer connects to an associated I/O module with four signals: OE (Output Enable), IE (Input Enable), DataOut, and DataIn. Certain special signals used only during programming and test also connect to the pad drivers: OUTEN (global output enable), INEN (global input enable), and SLEW (individual slew selection). See Figure 2-5.
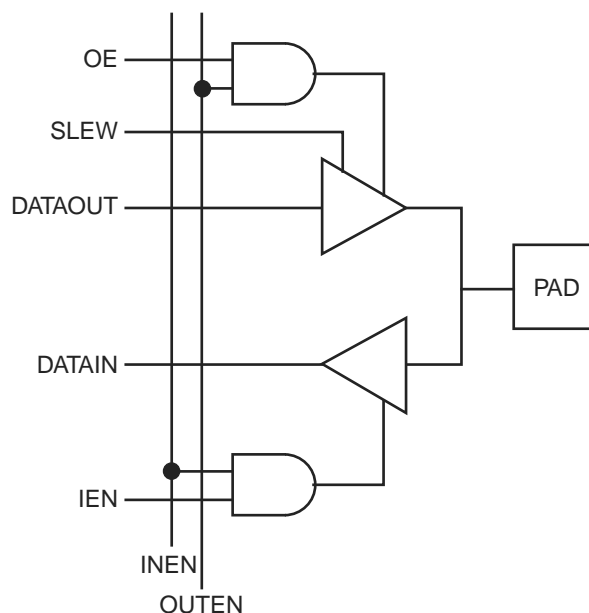

Figure 2-5 • **Function Diagram for I/O Pad Driver**

Special I/Os

The special I/Os are of two types: temporary and permanent. Temporary special I/Os are used during programming and testing. They function as normal I/Os when the MODE pin is inactive. Permanent special I/Os are user programmed as either normal I/Os or special I/Os. Their function does not change once the device has been programmed. The permanent special I/Os consist of the array clock input buffers (CLKA and CLKB), the hard-wired array clock input buffer (HCLK), the hard-wired I/O clock input buffer (IOCLK), and the hard-wired I/O register preset/clear input buffer (IOPCL). Their function is determined by the I/O macros selected.

Clock Networks

The ACT 3 architecture contains four clock networks: two high-performance dedicated clock networks and two general purpose routed networks. The high-performance networks function up to 200 MHz, while the general purpose routed networks function up to 150 MHz.

Package Thermal Characteristics

The device junction to case thermal characteristic is θjc, and the junction to ambient air characteristic is θja. The thermal characteristics for θja are shown with two different air flow rates.

Maximum junction temperature is 150°C.

A sample calculation of the absolute maximum power dissipation allowed for a CPGA 175-pin package at commercial temperature and still air is as follows:

$$\frac{\text{Max. junction temp. (°C)} - \text{Max. ambient temp. (°C)}}{\theta_{ja}\text{°C/W}} = \frac{150\text{°C} - 70\text{°C}}{25\text{°C/W}} = 3.2 \text{ W}$$

EQ 2

Table 2-8 • **Package Thermal Characteristics**

Package Type*	Pin Count	θ_{jc}	θ_{ja} Still Air	θ_{ja} 300 ft./min.	Units
Ceramic Pin Grid Array	100	20	35	17	°C/W
	133	20	30	15	°C/W
	175	20	25	14	°C/W
	207	20	22	13	°C/W
	257	20	15	8	°C/W
Ceramic Quad Flatpack	132	13	55	30	°C/W
	196	13	36	24	°C/W
	256	13	30	18	°C/W
Plastic Quad Flatpack	100	13	51	40	°C/W
	160	10	33	26	°C/W
	208	10	33	26	°C/W
Very Thin Quad Flatpack	100	12	43	35	°C/W
Thin Quad Flatpack	176	11	32	25	°C/W
Power Quad Flatpack	208	0.4	17	13	°C/W
Plastic Leaded Chip Carrier	84	12	37	28	°C/W
Plastic Ball Grid Array	225	10	25	19	°C/W
	313	10	23	17	°C/W

Note: Maximum power dissipation in still air:
PQ160 = 2.4 W
PQ208 = 2.4 W
PQ100 = 1.6 W
VQ100 = 1.9 W
TQ176 = 2.5 W
PL84 = 2.2 W
RQ208 = 4.7 W
BG225 = 3.2 W
BG313 = 3.5 W

Power Dissipation

P = [ICC standby + Iactive] * VCC * IOL * VOL * N + IOH* (VCC – VOH) * M

EQ 3

where:

ICC standby is the current flowing when no inputs or outputs are changing

Iactive is the current flowing due to CMOS switching.

IOL and IOH are TTL sink/source current.

VOL and VOH are TTL level output voltages.

N is the number of outputs driving TTL loads to VOL.

M equals the number of outputs driving TTL loads to VOH.

An accurate determination of N and M is problematic because their values depend on the design and on the system I/O. The power can be divided into two components: static and active.

Static Power Component

Microsemi FPGAs have small static power components that result in lower power dissipation than PALs or PLDs. By integrating multiple PALs/PLDs into one FPGA, an even greater reduction in board-level power dissipation can be achieved.

The power due to standby current is typically a small component of the overall power. Standby power is calculated in Table 2-9 for commercial, worst case conditions.

Table 2-9 • **Standby Power Calculation**

ICC	VCC	Power
2 mA	5.25 V	10.5 mW

The static power dissipated by TTL loads depends on the number of outputs driving high or low and the DC load current. Again, this value is typically small. For instance, a 32-bit bus sinking 4 mA at 0.33 V will generate 42 mW with all outputs driving low, and 140 mW with all outputs driving high. The actual dissipation will average somewhere between as I/Os switch states with time.

Active Power Component

Power dissipation in CMOS devices is usually dominated by the active (dynamic) power dissipation. This component is frequency dependent, a function of the logic and the external I/O. Active power dissipation results from charging internal chip capacitances of the interconnect, unprogrammed antifuses, module inputs, and module outputs, plus external capacitance due to PC board traces and load device inputs.

An additional component of the active power dissipation is the totem-pole current in CMOS transistor pairs. The net effect can be associated with an equivalent capacitance that can be combined with frequency and voltage to represent active power dissipation.

Equivalent Capacitance

The power dissipated by a CMOS circuit can be expressed by EQ 4.

Power (μW) = C_{EQ} * VCC^2 * F

EQ 4

Where:

C_{EQ} is the equivalent capacitance expressed in pF.

VCC is the power supply in volts.

F is the switching frequency in MHz.

A1415A, A14V15A Timing Characteristics (continued)

Table 2-20 • **A1415A, A14V15A Worst-Case Commercial Conditions, VCC = 4.75 V, T$_J$ = 70°C**

I/O Module – TTL Output Timing[1]		–3 Speed[2]		–2 Speed[2]		–1 Speed		Std. Speed		3.3 V Speed[1]		Units
Parameter/Description		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t$_{DHS}$	Data to Pad, High Slew		5.0		5.6		6.4		7.5		9.8	ns
t$_{DLS}$	Data to Pad, Low Slew		8.0		9.0		10.2		12.0		15.6	ns
t$_{ENZHS}$	Enable to Pad, Z to H/L, High Slew		4.0		4.5		5.1		6.0		7.8	ns
t$_{ENZLS}$	Enable to Pad, Z to H/L, Low Slew		7.4		8.3		9.4		11.0		14.3	ns
t$_{ENHSZ}$	Enable to Pad, H/L to Z, High Slew		6.5		7.5		8.5		10.0		13.0	ns
t$_{ENLSZ}$	Enable to Pad, H/L to Z, Low Slew		6.5		7.5		8.5		10.0		13.0	ns
t$_{CKHS}$	IOCLK Pad to Pad H/L, High Slew		7.5		7.5		9.0		10.0		13.0	ns
t$_{CKLS}$	IOCLK Pad to Pad H/L, Low Slew		11.3		11.3		13.5		15.0		19.5	ns
d$_{TLHHS}$	Delta Low to High, High Slew		0.02		0.02		0.03		0.03		0.04	ns/pF
d$_{TLHLS}$	Delta Low to High, Low Slew		0.05		0.05		0.06		0.07		0.09	ns/pF
d$_{THLHS}$	Delta High to Low, High Slew		0.04		0.04		0.04		0.05		0.07	ns/pF
d$_{THLLS}$	Delta High to Low, Low Slew		0.05		0.05		0.06		0.07		0.09	ns/pF
I/O Module – CMOS Output Timing[1]												
t$_{DHS}$	Data to Pad, High Slew		6.2		7.0		7.9		9.3		12.1	ns
t$_{DLS}$	Data to Pad, Low Slew		11.7		13.1		14.9		17.5		22.8	ns
t$_{ENZHS}$	Enable to Pad, Z to H/L, High Slew		5.2		5.9		6.6		7.8		10.1	ns
t$_{ENZLS}$	Enable to Pad, Z to H/L, Low Slew		8.9		10.0		11.3		13.3		17.3	ns
t$_{ENHSZ}$	Enable to Pad, H/L to Z, High Slew		6.7		7.5		8.5		10.0		13.0	ns
t$_{ENLSZ}$	Enable to Pad, H/L to Z, Low Slew		6.7		7.5		9.0		10.0		13.0	ns
t$_{CKHS}$	IOCLK Pad to Pad H/L, High Slew		8.9		8.9		10.7		11.8		15.3	ns
t$_{CKLS}$	IOCLK Pad to Pad H/L, Low Slew		13.0		13.0		15.6		17.3		22.5	ns
d$_{TLHHS}$	Delta Low to High, High Slew		0.04		0.04		0.05		0.06		0.08	ns/pF
d$_{TLHLS}$	Delta Low to High, Low Slew		0.07		0.08		0.09		0.11		0.14	ns/pF
d$_{THLHS}$	Delta High to Low, High Slew		0.03		0.03		0.03		0.04		0.05	ns/pF
d$_{THLLS}$	Delta High to Low, Low Slew		0.04		0.04		0.04		0.05		0.07	ns/pF

Notes:

1. *Delays based on 35 pF loading.*

2. *The –2 and –3 speed grades have been discontinued. Please refer to the Product Discontinuation Notices (PDNs) listed below:*

   PDN March 2001
   PDN 0104
   PDN 0203
   PDN 0604
   PDN 1004

A1425A, A14V25A Timing Characteristics

Table 2-22 • A1425A, A14V25A Worst-Case Commercial Conditions, VCC = 4.75 V, T_J = 70°C[1]

Logic Module Propagation Delays[2]		−3 Speed[3]		−2 Speed[3]		−1 Speed		Std. Speed		3.3 V Speed[1]		Units
Parameter/Description		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t_{PD}	Internal Array Module		2.0		2.3		2.6		3.0		3.9	ns
t_{CO}	Sequential Clock to Q		2.0		2.3		2.6		3.0		3.9	ns
t_{CLR}	Asynchronous Clear to Q		2.0		2.3		2.6		3.0		3.9	ns
Predicted Routing Delays[4]												
t_{RD1}	FO = 1 Routing Delay		0.9		1.0		1.1		1.3		1.7	ns
t_{RD2}	FO = 2 Routing Delay		1.2		1.4		1.6		1.8		2.4	ns
t_{RD3}	FO = 3 Routing Delay		1.4		1.6		1.8		2.1		2.8	ns
t_{RD4}	FO = 4 Routing Delay		1.7		1.9		2.2		2.5		3.3	ns
t_{RD8}	FO = 8 Routing Delay		2.8		3.2		3.6		4.2		5.5	ns
Logic Module Sequential Timing												
t_{SUD}	Flip-Flop Data Input Setup	0.5		0.6		0.7		0.8		0.8		ns
t_{HD}	Flip-Flop Data Input Hold	0.0		0.0		0.0		0.0		0.0		ns
t_{SUD}	Latch Data Input Setup	0.5		0.6		0.7		0.8		0.8		ns
t_{HD}	Latch Data Input Hold	0.0		0.0		0.0		0.0		0.0		ns
t_{WASYN}	Asynchronous Pulse Width	1.9		2.4		3.2		3.8		4.8		ns
t_{WCLKA}	Flip-Flop Clock Pulse Width	1.9		2.4		3.2		3.8		4.8		ns
t_A	Flip-Flop Clock Input Period	4.0		5.0		6.8		8.0		10.0		ns
f_{MAX}	Flip-Flop Clock Frequency		250		200		150		125		100	MHz

Notes:

1. *VCC = 3.0 V for 3.3 V specifications.*

2. *For dual-module macros, use $t_{PD} + t_{RD1} + t_{PDn} + t_{CO} + t_{RD1} + t_{PDn}$ or $t_{PD1} + t_{RD1} + t_{SUD}$, whichever is appropriate.*

3. *The −2 and −3 speed grades have been discontinued. Refer to PDN 0104, PDN 0203, PDN 0604, and PDN 1004 at http://www.microsemi.com/soc/support/notifications/default.aspx#pdn.*

4. *Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual worst-case performance. Post-route timing is based on actual routing delay measurements performed on the device prior to shipment.*

A1425A, A14V25A Timing Characteristics (continued)

Table 2-23 • **A1425A, A14V25A Worst-Case Commercial Conditions, VCC = 4.75 V, T$_J$ = 70°C**

I/O Module Input Propagation Delays		–3 Speed[1]		–2 Speed[1]		–1 Speed		Std. Speed		3.3 V Speed[1]		Units
Parameter/Description		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t$_{INY}$	Input Data Pad to Y		2.8		3.2		3.6		4.2		5.5	ns
t$_{ICKY}$	Input Reg IOCLK Pad to Y		4.7		5.3		6.0		7.0		9.2	ns
t$_{OCKY}$	Output Reg IOCLK Pad to Y		4.7		5.3		6.0		7.0		9.2	ns
t$_{ICLRY}$	Input Asynchronous Clear to Y		4.7		5.3		6.0		7.0		9.2	ns
t$_{OCLRY}$	Output Asynchronous Clear to Y		4.7		5.3		6.0		7.0		9.2	ns
Predicted Input Routing Delays[2]												
t$_{RD1}$	FO = 1 Routing Delay		0.9		1.0		1.1		1.3		1.7	ns
t$_{RD2}$	FO = 2 Routing Delay		1.2		1.4		1.6		1.8		2.4	ns
t$_{RD3}$	FO = 3 Routing Delay		1.4		1.6		1.8		2.1		2.8	ns
t$_{RD4}$	FO = 4 Routing Delay		1.7		1.9		2.2		2.5		3.3	ns
t$_{RD8}$	FO = 8 Routing Delay		2.8		3.2		3.6		4.2		5.5	ns
I/O Module Sequential Timing (wrt IOCLK pad)												
t$_{INH}$	Input F-F Data Hold	0.0		0.0		0.0		0.0		0.0		ns
t$_{INSU}$	Input F-F Data Setup	1.8		2.0		2.3		2.7		3.0		ns
t$_{IDEH}$	Input Data Enable Hold	0.0		0.0		0.0		0.0		0.0		ns
t$_{IDESU}$	Input Data Enable Setup	5.8		6.5		7.5		8.6		8.6		ns
t$_{OUTH}$	Output F-F Data hold	0.7		0.8		0.9		1.0		1.0		ns
t$_{OUTSU}$	Output F-F Data Setup	0.7		0.8		0.9		1.0		1.0		ns
t$_{ODEH}$	Output Data Enable Hold	0.3		0.4		0.4		0.5		0.5		ns
f$_{ODESU}$	Output Data Enable Setup	1.3		1.5		1.7		2.0		2.0		ns

Notes: *

1. *The –2 and –3 speed grades have been discontinued. Refer to PDN 0104, PDN 0203, PDN 0604, and PDN 1004 at http://www.microsemi.com/soc/support/notifications/default.aspx#pdn.*

2. *Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual worst-case performance. Post-route timing is based on actual routing delay measurements performed on the device prior to shipment.*

A1440A, A14V40A Timing Characteristics (continued)

Table 2-28 • **A1440A, A14V40A Worst-Case Commercial Conditions, VCC = 4.75 V, T$_J$ = 70°C**

I/O Module – TTL Output Timing[1]		–3 Speed[2]		–2 Speed[2]		–1 Speed		Std. Speed		3.3 V Speed[1]		Units
Parameter/Description		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t$_{DHS}$	Data to Pad, High Slew		5.0		5.6		6.4		7.5		9.8	ns
t$_{DLS}$	Data to Pad, Low Slew		8.0		9.0		10.2		12.0		15.6	ns
t$_{ENZHS}$	Enable to Pad, Z to H/L, High Slew		4.0		4.5		5.1		6.0		7.8	ns
t$_{ENZLS}$	Enable to Pad, Z to H/L, Low Slew		7.4		8.3		9.4		11.0		14.3	ns
t$_{ENHSZ}$	Enable to Pad, H/L to Z, High Slew		7.4		8.3		9.4		11.0		14.3	ns
t$_{ENLSZ}$	Enable to Pad, H/L to Z, Low Slew		7.4		8.3		9.4		11.0		14.3	ns
t$_{CKHS}$	IOCLK Pad to Pad H/L, High Slew		8.5		8.5		9.5		11.0		14.3	ns
t$_{CKLS}$	IOCLK Pad to Pad H/L, Low Slew		11.3		11.3		13.5		15.0		19.5	ns
d$_{TLHHS}$	Delta Low to High, High Slew		0.02		0.02		0.03		0.03		0.04	ns/pF
d$_{TLHLS}$	Delta Low to High, Low Slew		0.05		0.05		0.06		0.07		0.09	ns/pF
d$_{THLHS}$	Delta High to Low, High Slew		0.04		0.04		0.04		0.05		0.07	ns/pF
d$_{THLLS}$	Delta High to Low, Low Slew		0.05		0.05		0.06		0.07		0.09	ns/pF
I/O Module – CMOS Output Timing[1]												
t$_{DHS}$	Data to Pad, High Slew		6.2		7.0		7.9		9.3		12.1	ns
t$_{DLS}$	Data to Pad, Low Slew		11.7		13.1		14.9		17.5		22.8	ns
t$_{ENZHS}$	Enable to Pad, Z to H/L, High Slew		5.2		5.9		6.6		7.8		10.1	ns
t$_{ENZLS}$	Enable to Pad, Z to H/L, Low Slew		8.9		10.0		11.3		13.3		17.3	ns
t$_{ENHSZ}$	Enable to Pad, H/L to Z, High Slew		7.4		8.3		9.4		11.0		14.3	ns
t$_{ENLSZ}$	Enable to Pad, H/L to Z, Low Slew		7.4		8.3		9.4		11.0		14.3	ns
t$_{CKHS}$	IOCLK Pad to Pad H/L, High Slew		9.0		9.0		10.1		11.8		14.3	ns
t$_{CKLS}$	IOCLK Pad to Pad H/L, Low Slew		13.0		13.0		15.6		17.3		22.5	ns
d$_{TLHHS}$	Delta Low to High, High Slew		0.04		0.04		0.05		0.06		0.08	ns/pF
d$_{TLHLS}$	Delta Low to High, Low Slew		0.07		0.08		0.09		0.11		0.14	ns/pF
d$_{THLHS}$	Delta High to Low, High Slew		0.03		0.03		0.03		0.04		0.05	ns/pF
d$_{THLLS}$	Delta High to Low, Low Slew		0.04		0.04		0.04		0.05		0.07	ns/pF

Notes:

1. Delays based on 35 pF loading.

2. The –2 and –3 speed grades have been discontinued. Refer to PDN 0104, PDN 0203, PDN 0604, and PDN 1004 at http://www.microsemi.com/soc/support/notifications/default.aspx#pdn.

A14100A, A14V100A Timing Characteristics (continued)

Table 2-36 • **A14100A, A14V100A Worst-Case Commercial Conditions, VCC = 4.75 V, T$_J$ = 70°C**

| I/O Module – TTL Output Timing[1]		–3 Speed[2]		–2 Speed[2]		–1 Speed		Std. Speed		3.3 V Speed[1]		Units
Parameter/Description		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t$_{DHS}$	Data to Pad, High Slew		5.0		5.6		6.4		7.5		9.8	ns
t$_{DLS}$	Data to Pad, Low Slew		8.0		9.0		10.2		12.0		15.6	ns
t$_{ENZHS}$	Enable to Pad, Z to H/L, High Slew		4.0		4.5		5.1		6.0		7.8	ns
t$_{ENZLS}$	Enable to Pad, Z to H/L, Low Slew		7.4		8.3		9.4		11.0		14.3	ns
t$_{ENHSZ}$	Enable to Pad, H/L to Z, High Slew		8.0		9.0		10.2		12.0		15.6	ns
t$_{ENLSZ}$	Enable to Pad, H/L to Z, Low Slew		7.4		8.3		9.4		11.0		14.3	ns
t$_{CKHS}$	IOCLK Pad to Pad H/L, High Slew		9.5		9.5		10.5		12.0		15.6	ns
t$_{CKLS}$	IOCLK Pad to Pad H/L, Low Slew		12.8		12.8		15.3		17.0		22.1	ns
d$_{TLHHS}$	Delta Low to High, High Slew		0.02		0.02		0.03		0.03		0.04	ns/pF
d$_{TLHLS}$	Delta Low to High, Low Slew		0.05		0.05		0.06		0.07		0.09	ns/pF
d$_{THLHS}$	Delta High to Low, High Slew		0.04		0.04		0.04		0.05		0.07	ns/pF
d$_{THLLS}$	Delta High to Low, Low Slew		0.05		0.05		0.06		0.07		0.09	ns/pF
I/O Module – CMOS Output Timing[1]												
t$_{DHS}$	Data to Pad, High Slew		6.2		7.0		7.9		9.3		12.1	ns
t$_{DLS}$	Data to Pad, Low Slew		11.7		13.1		14.9		17.5		22.8	ns
t$_{ENZHS}$	Enable to Pad, Z to H/L, High Slew		5.2		5.9		6.6		7.8		10.1	ns
t$_{ENZLS}$	Enable to Pad, Z to H/L, Low Slew		8.9		10.0		11.3		13.3		17.3	ns
t$_{ENHSZ}$	Enable to Pad, H/L to Z, High Slew		8.0		9.0		10.0		12.0		15.6	ns
t$_{ENLSZ}$	Enable to Pad, H/L to Z, Low Slew		7.4		8.3		9.4		11.0		14.3	ns
t$_{CKHS}$	IOCLK Pad to Pad H/L, High Slew		10.4		10.4		12.4		13.8		17.9	ns
t$_{CKLS}$	IOCLK Pad to Pad H/L, Low Slew		14.5		14.5		17.4		19.3		25.1	ns
d$_{TLHHS}$	Delta Low to High, High Slew		0.04		0.04		0.05		0.06		0.08	ns/pF
d$_{TLHLS}$	Delta Low to High, Low Slew		0.07		0.08		0.09		0.11		0.14	ns/pF
d$_{THLHS}$	Delta High to Low, High Slew		0.03		0.03		0.03		0.04		0.05	ns/pF
d$_{THLLS}$	Delta High to Low, Low Slew		0.04		0.04		0.04		0.05		0.07	ns/pF

*Notes: *

1. Delays based on 35 pF loading.

2. The –2 and –3 speed grades have been discontinued. Refer to PDN 0104, PDN 0203, PDN 0604, and PDN 1004 at http://www.microsemi.com/soc/support/notifications/default.aspx#pdn.

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PL84			
Pin Number	**A1415, A14V15 Function**	**A1425, A14V25 Function**	**A1440, A14V40 Function**
1	VCC	VCC	VCC
2	GND	GND	GND
3	VCC	VCC	VCC
4	PRA, I/O	PRA, I/O	PRA, I/O
11	DCLK, I/O	DCLK, I/O	DCLK, I/O
12	SDI, I/O	SDI, I/O	SDI, I/O
16	MODE	MODE	MODE
27	GND	GND	GND
28	VCC	VCC	VCC
40	PRB, I/O	PRB, I/O	PRB, I/O
41	VCC	VCC	VCC
42	GND	GND	GND
43	VCC	VCC	VCC
45	HCLK, I/O	HCLK, I/O	HCLK, I/O
52	SDO	SDO	SDO
53	IOPCL, I/O	IOPCL, I/O	IOPCL, I/O
59	VCC	VCC	VCC
60	VCC	VCC	VCC
61	GND	GND	GND
68	VCC	VCC	VCC
69	GND	GND	GND
74	IOCLK, I/O	IOCLK, I/O	IOCLK, I/O
83	CLKA, I/O	CLKA, I/O	CLKA, I/O
84	CLKB, I/O	CLKB, I/O	CLKB, I/O

Notes:

1. All unlisted pin numbers are user I/Os.

2. NC denotes no connection.

3. MODE should be terminated to GND through a 10K resistor to enable Actionprobe usage; otherwise it can be terminated directly to GND.
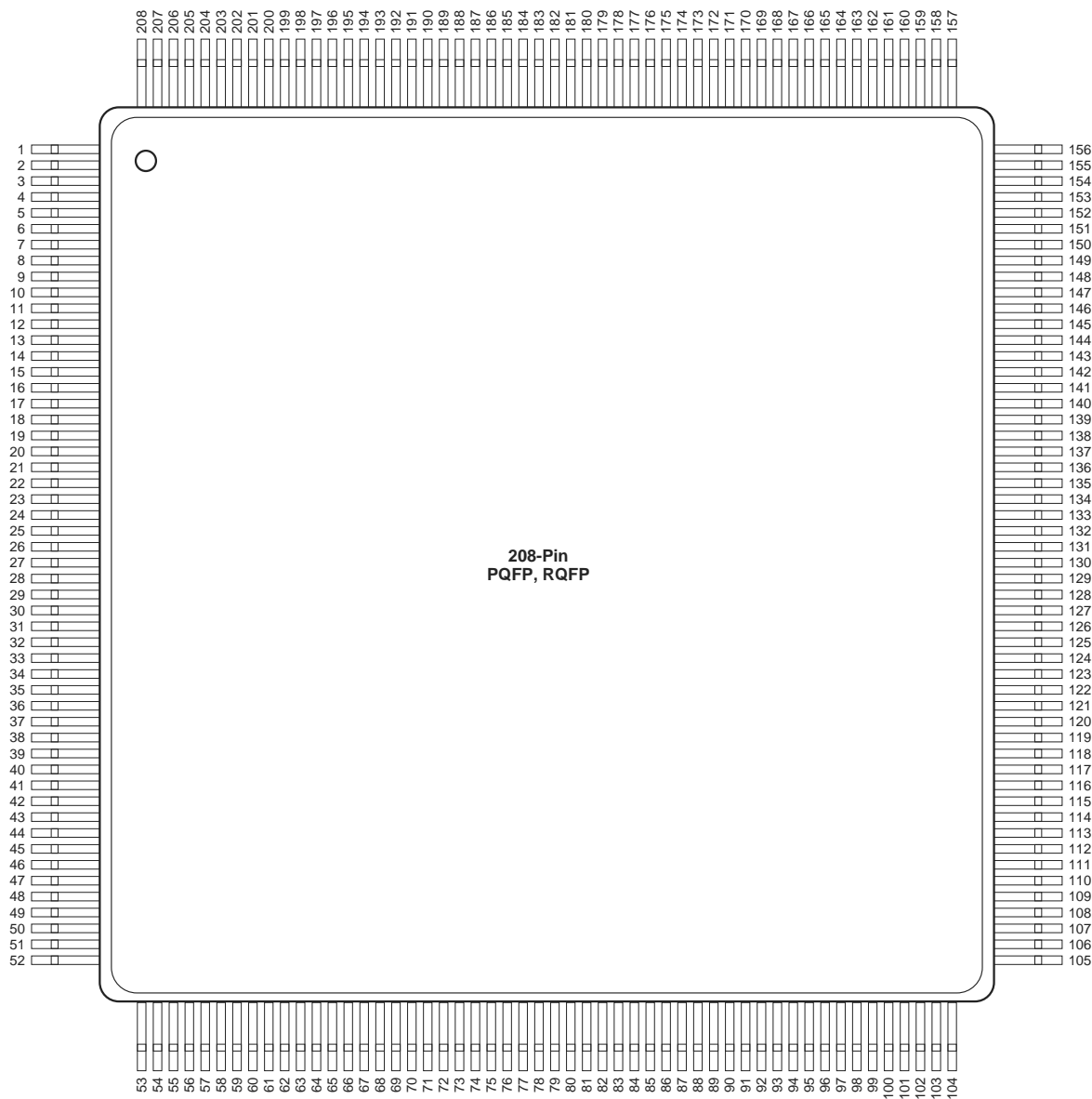
PQ100
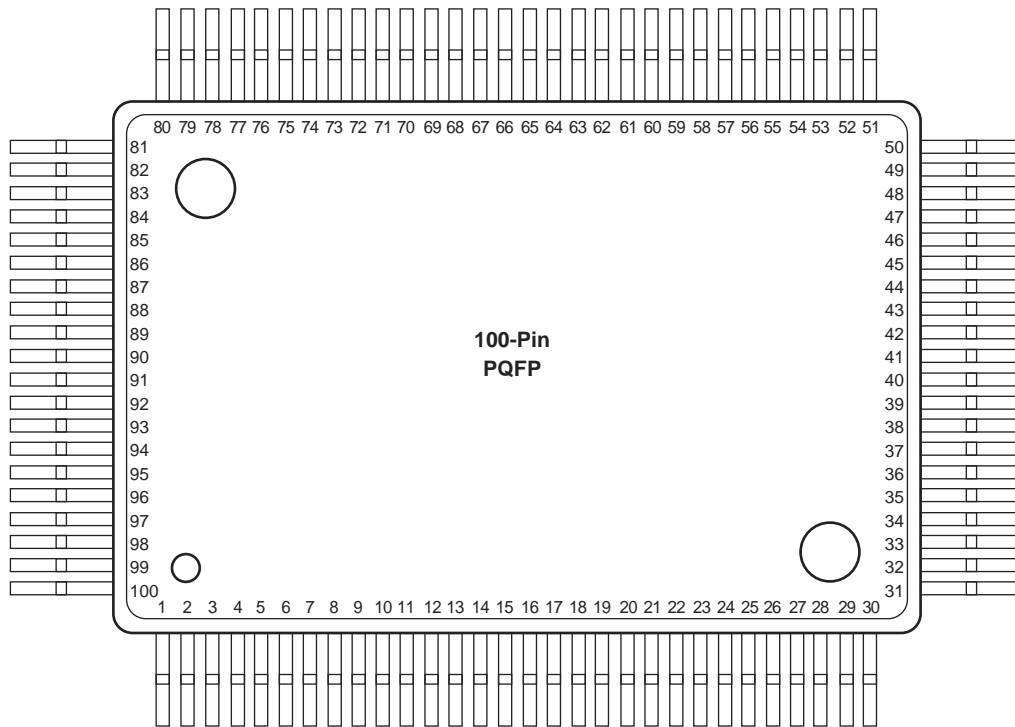
**100-Pin
PQFP**

Note: This is the top view of the package.

Note

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http://www.microsemi.com/soc/products/solutions/package/docs.aspx

PQ160			
Pin Number	**A1425, A14V25 Function**	**A1440, A14V40 Function**	**A1460, A14V60 Function**
1	GND	GND	GND
2	SDI, I/O	SDI, I/O	SDI, I/O
5	NC	I/O	I/O
9	MODE	MODE	MODE
10	VCC	VCC	VCC
14	NC	I/O	I/O
15	GND	GND	GND
18	VCC	VCC	VCC
19	GND	GND	GND
20	NC	I/O	I/O
24	NC	I/O	I/O
27	NC	I/O	I/O
28	VCC	VCC	VCC
29	VCC	VCC	VCC
40	GND	GND	GND
41	NC	I/O	I/O
43	NC	I/O	I/O
45	NC	I/O	I/O
46	VCC	VCC	VCC
47	NC	I/O	I/O
49	NC	I/O	I/O
51	NC	I/O	I/O
53	NC	I/O	I/O
58	PRB, I/O	PRB, I/O	PRB, I/O
59	GND	GND	GND
60	VCC	VCC	VCC
62	HCLK, I/O	HCLK, I/O	HCLK, I/O
63	GND	GND	GND
74	NC	I/O	I/O
75	VCC	VCC	VCC
76	NC	I/O	I/O
77	NC	I/O	I/O
78	NC	I/O	I/O
79	SDO	SDO	SDO
80	IOPCL, I/O	IOPCL, I/O	IOPCL, I/O
81	GND	GND	GND
90	VCC	VCC	VCC
91	VCC	VCC	VCC

PQ208, RQ208

Note: This is the top view of the package

Note

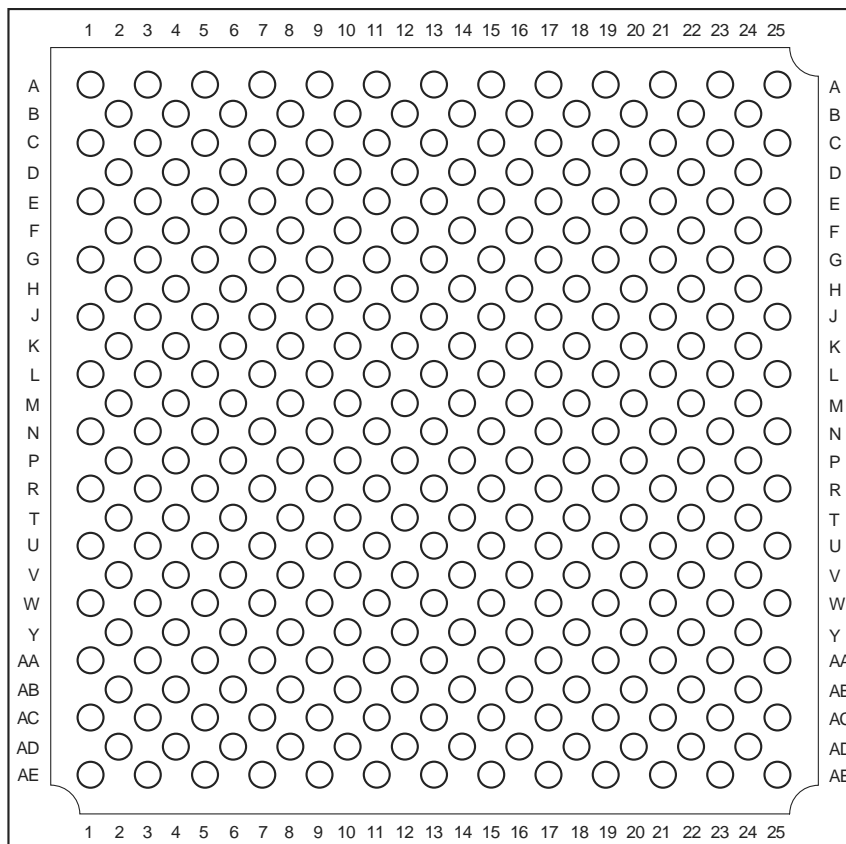For Package Manufacturing and Environmental information, visit the Resource Center at
http://www.microsemi.com/soc/products/solutions/package/docs.aspx

PQ208, RQ208			PQ208, RQ208		
Pin Number	A1460, A14V60 Function	A14100, A14V100 Function	Pin Number	A1460, A14V60 Function	A14100, A14V100 Function
1	GND	GND	115	VCC	VCC
2	SDI, I/O	SDI, I/O	116	NC	I/O
11	MODE	MODE	129	GND	GND
12	VCC	VCC	130	VCC	VCC
25	VCC	VCC	131	GND	GND
26	GND	GND	132	VCC	VCC
27	VCC	VCC	145	VCC	VCC
28	GND	GND	146	GND	GND
40	VCC	VCC	147	NC	I/O
41	VCC	VCC	148	VCC	VCC
52	GND	GND	156	IOCLK, I/O	IOCLK, I/O
53	NC	I/O	157	GND	GND
60	VCC	VCC	158	NC	I/O
65	NC	I/O	164	VCC	VCC
76	PRB, I/O	PRB, I/O	180	CLKA, I/O	CLKA, I/O
77	GND	GND	181	CLKB, I/O	CLKB, I/O
78	VCC	VCC	182	VCC	VCC
79	GND	GND	183	GND	GND
80	VCC	VCC	184	VCC	VCC
82	HCLK, I/O	HCLK, I/O	185	GND	GND
98	VCC	VCC	186	PRA, I/O	PRA, I/O
102	NC	I/O	195	NC	I/O
103	SDO	SDO	201	VCC	VCC
104	IOPCL, I/O	IOPCL, I/O	205	NC	I/O
105	GND	GND	208	DCLK, I/O	DCLK, I/O
114	VCC	VCC			

Notes:

1. All unlisted pin numbers are user I/Os.
2. NC denotes no connection.
3. MODE should be terminated to GND through a 10K resistor to enable Actionprobe usage; otherwise it can be terminated directly to GND.
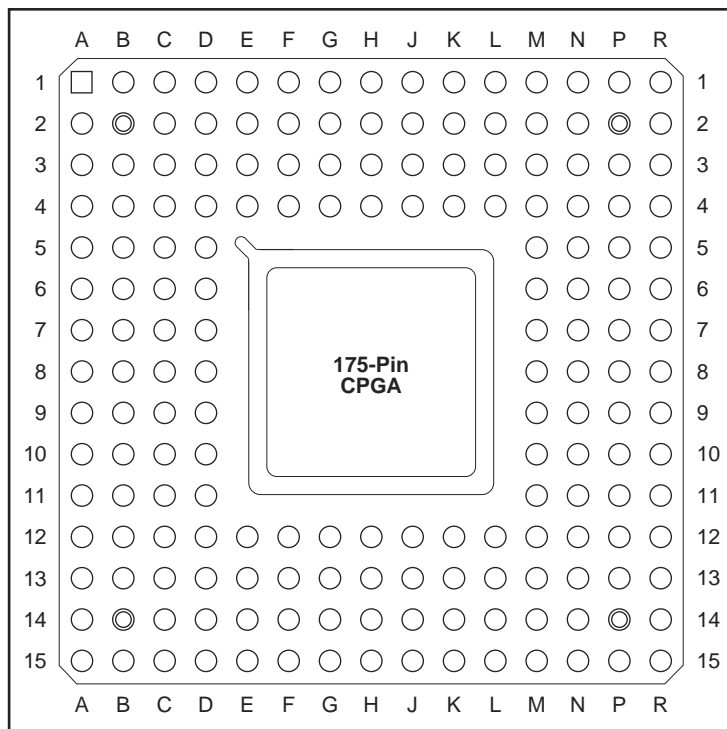
BG313

Note: This is the top view.

Note

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BG313	
A14100, A14V100 Function	**Location**
CLKA or I/O	J13
CLKB or I/O	G13
DCLK or I/O	B2
GND	A1, A25, AD2, AE25, J21, L13, M12, M14, N11, N13, N15, P12, P14, R13
HCLK or I/O	T14
IOCLK or I/O	B24
IOPCL or I/O	AD24
MODE	G3
NC	A3, A13, A23, AA5, AA9, AA23, AB2, AB4, AB20, AC13, AC25, AD22, AE1, AE21, B14, C5, C25, D4, D24, E3, E21, F6, F10, F16, G1, G25, H18, H24, J1, J7, J25, K12, L15, L17, M6, N1, N5, N7, N21, N23, P20, R11, T6, T8, U9, U13, U21, V16, W7, Y20, Y24
PRA or I/O	H12
PRB or I/O	AD12
SDI or I/O	C1
SDO	AE23
VCC	AB18, AD6, AE13, C13, C19, E13, G9, H22, K8, K20, M16, N3, N9, N25, U5, W13, V2, V22, V24

Notes:

1. All unlisted pin numbers are user I/Os.

2. NC denotes no connection.

3. MODE should be terminated to GND through a 10K resistor to enable Actionprobe usage; otherwise it can be terminated directly to GND.

PG175

Note: This is the top view.

Note

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