Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications,

Details

Product Status	Obsolete
Number of LABs/CLBs	564
Number of Logic Elements/Cells	-
Total RAM Bits	-
Number of I/O	83
Number of Gates	4000
Voltage - Supply	4.5V ~ 5.5V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 85°C (TA)
Package / Case	100-TQFP
Supplier Device Package	100-VQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/microsemi/a1440a-1vqg100i

Product Plan

Device/Package	Speed Grade[1]				Application[1]			
	Std.	–1	–2	–3	C	I	M	B
A1415A Device								
84-Pin Plastic Leaded Chip Carrier (PLCC)	✓	✓	D	D	✓	✓	✓	–
100-Pin Plastic Quad Flatpack (PQFP)	✓	✓	D	D	✓	✓	✓	–
100-Pin Very Thin Quad Flatpack (VQFP)	✓	✓	D	D	✓	✓	✓	–
100-Pin Ceramic Pin Grid Array (CPGA)	D	D	D	D	D	–	–	–
A14V15A Device								
84-Pin Plastic Leaded Chip Carrier (PLCC)	✓	–	–	–	✓	–	–	–
100-Pin Very Thin Quad Flatpack (VQFP)	✓	–	–	–	✓	–	–	–
A1425A Device								
84-Pin Plastic Leaded Chip Carrier (PLCC)	✓	✓	D	D	✓	✓		
100-Pin Plastic Quad Flatpack (PQFP)	✓	✓	D	D	✓	✓	–	–
100-Pin Very Thin Quad Flatpack (VQFP)	✓	✓	D	D	✓	✓	–	–
132-Pin Ceramic Quad Flatpack (CQFP)	✓	✓	–	–	✓	–	✓	✓
133-Pin Ceramic Pin Grid Array (CPGA)	D	D	D	D	D	–	D	D
160-Pin Plastic Quad Flatpack (PQFP)	✓	✓	D	D	✓	✓	–	–
A14V25A Device								
84-Pin Plastic Leaded Chip Carrier (PLCC)	✓	–	–	–	✓	–	–	–
100-Pin Very Thin Quad Flatpack (VQFP)	✓	–	–	–	✓	–	–	–
160-Pin Plastic Quad Flatpack (PQFP)	✓	–	–	–	✓	–	–	–
A1440A Device								
84-Pin Plastic Leaded Chip Carrier (PLCC)	✓	✓	D	D	✓	✓	–	–
100-Pin Very Thin Quad Flatpack (VQFP)	✓	✓	D	D	✓	✓	–	–
160-Pin Plastic Quad Flatpack (PQFP)	✓	✓	D	D	✓	✓	–	–
175-Pin Ceramic Pin Grid Array (CPGA)	D	D	D	D	D	–	–	–
176-Pin Thin Quad Flatpack (TQFP)	✓	✓	D	D	✓	✓	–	–

Notes:

1. Applications:
   C = Commercial
   I = Industrial
   M = Military
2. Commercial only

Availability:
✓ = Available
P = Planned
– = Not planned
D = Discontinued

Speed Grade:
–1 = Approx. 15% faster than Std.
–2 = Approx. 25% faster than Std.
–3 = Approx. 35% faster than Std.
(–2 and –3 speed grades have been discontinued.)

The S-module contains a full implementation of the C-module plus a clearable sequential element that can either implement a latch or flip-flop function. The S-module can therefore implement any function implemented by the C-module. This allows complex combinatorial-sequential functions to be implemented with no delay penalty. The Designer Series Development System will automatically combine any C-module macro driving an S-module macro into the S-module, thereby freeing up a logic module and eliminating a module delay.

The clear input CLR is accessible from the routing channel. In addition, the clock input may be connected to one of three clock networks: CLKA, CLKB, or HCLK. The C-module and S-module functional descriptions are shown in Figure 2-2 and Figure 2-3 on page 2-2. The clock selection is determined by a multiplexer select at the clock input to the S-module.

I/Os

I/O Modules

I/O modules provide an interface between the array and the I/O Pad Drivers. I/O modules are located in the array and access the routing channels in a similar fashion to logic modules. The I/O module schematic is shown in Figure 4. The signals DataIn and DataOut connect to the I/O pad driver.
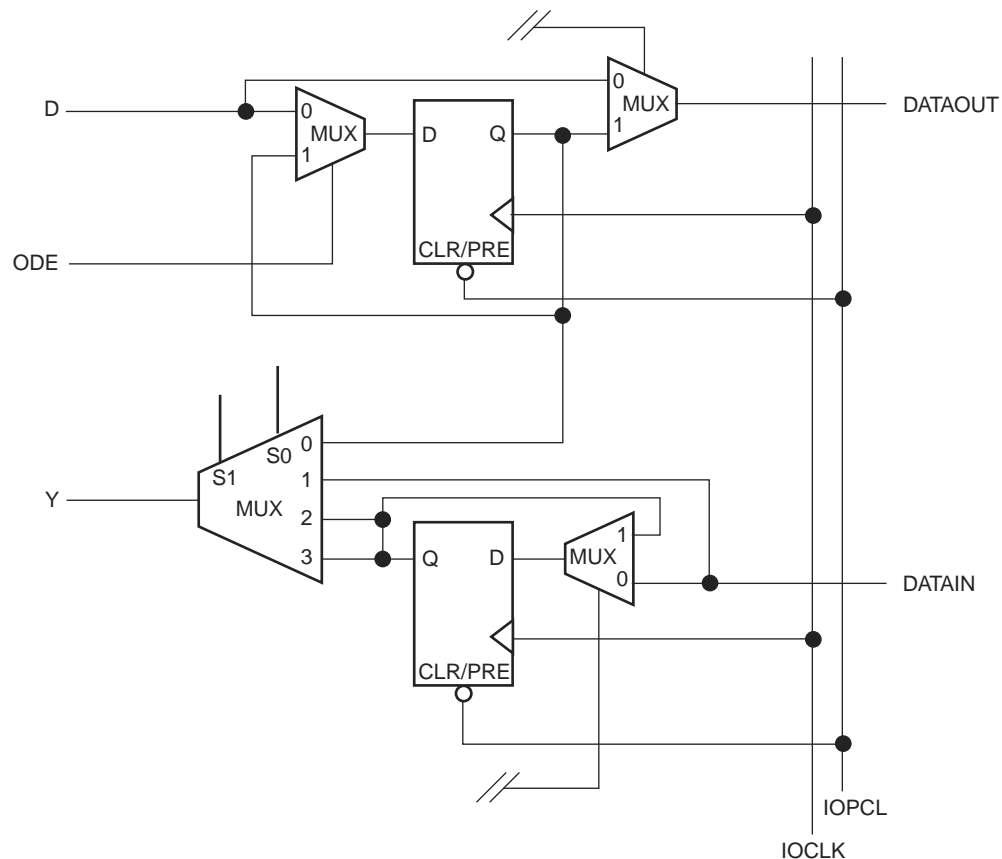

Figure 2-4 • **Functional Diagram for I/O Module**

Each I/O module contains two D-type flip-flops. Each flip-flop is connected to the dedicated I/O clock (IOCLK). Each flip-flop can be bypassed by nonsequential I/Os. In addition, each flip-flop contains a data enable input that can be accessed from the routing channels (ODE and IDE). The asynchronous preset/clear input is driven by the dedicated preset/clear network (IOPCL). Either preset or clear can be selected individually on an I/O module by I/O module basis.

The I/O module output Y is used to bring Pad signals into the array or to feed the output register back into the array. This allows the output register to be used in high-speed state machine applications. Side I/O modules have a dedicated output segment for Y extending into the routing channels above and below (similar to logic modules). Top/Bottom I/O modules have no dedicated output segment. Signals coming into the chip from the top or bottom are routed using F-fuses and LVTs (F-fuses and LVTs are explained in detail in the routing section).

I/O Pad Drivers

All pad drivers are capable of being tristate. Each buffer connects to an associated I/O module with four signals: OE (Output Enable), IE (Input Enable), DataOut, and DataIn. Certain special signals used only during programming and test also connect to the pad drivers: OUTEN (global output enable), INEN (global input enable), and SLEW (individual slew selection). See Figure 2-5.
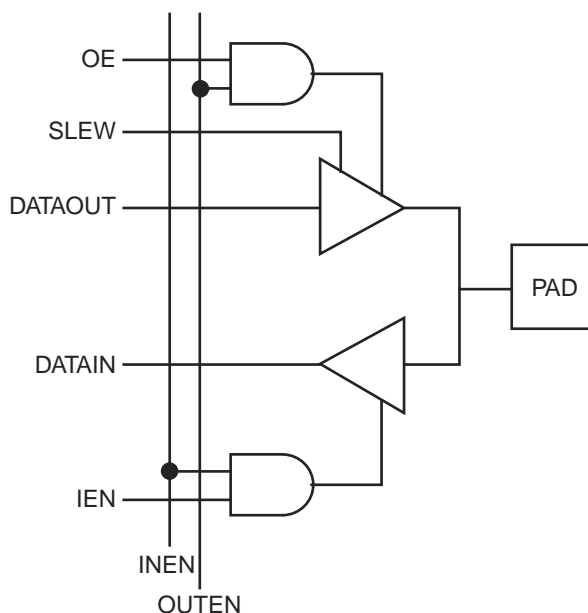

Figure 2-5 • Function Diagram for I/O Pad Driver

Special I/Os

The special I/Os are of two types: temporary and permanent. Temporary special I/Os are used during programming and testing. They function as normal I/Os when the MODE pin is inactive. Permanent special I/Os are user programmed as either normal I/Os or special I/Os. Their function does not change once the device has been programmed. The permanent special I/Os consist of the array clock input buffers (CLKA and CLKB), the hard-wired array clock input buffer (HCLK), the hard-wired I/O clock input buffer (IOCLK), and the hard-wired I/O register preset/clear input buffer (IOPCL). Their function is determined by the I/O macros selected.

Clock Networks

The ACT 3 architecture contains four clock networks: two high-performance dedicated clock networks and two general purpose routed networks. The high-performance networks function up to 200 MHz, while the general purpose routed networks function up to 150 MHz.

Dedicated Clocks

Dedicated clock networks support high performance by providing sub-nanosecond skew and guaranteed performance. Dedicated clock networks contain no programming elements in the path from the I/O Pad Driver to the input of S-modules or I/O modules. There are two dedicated clock networks: one for the array registers (HCLK), and one for the I/O registers (IOCLK). The clock networks are accessed by special I/Os.
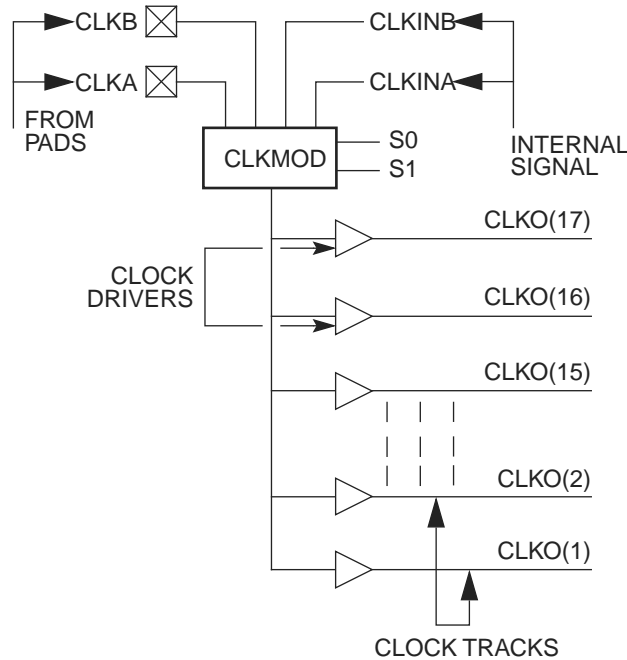

Figure 2-6 • **Clock Networks**

The routed clock networks are referred to as CLK0 and CLK1. Each network is connected to a clock module (CLKMOD) that selects the source of the clock signal and may be driven as follows (Figure 2-6):

*   Externally from the CLKA pad
*   Externally from the CLKB pad
*   Internally from the CLKINA input
*   Internally from the CLKINB input

The clock modules are located in the top row of I/O modules. Clock drivers and a dedicated horizontal clock track are located in each horizontal routing channel. The function of the clock module is determined by the selection of clock macros from the macro library. The macro CLKBUF is used to connect one of the two external clock pins to a clock network, and the macro CLKINT is used to connect an internally generated clock signal to a clock network. Since both clock networks are identical, the user does not care whether CLK0 or CLK1 is being used. Routed clocks can also be used to drive high fanout nets like resets, output enables, or data enables. This saves logic modules and results in performance increases in some cases.

Routing Structure

The ACT 3 architecture uses vertical and horizontal routing tracks to connect the various logic and I/O modules. These routing tracks are metal interconnects that may either be of continuous length or broken into segments. Segments can be joined together at the ends using antifuses to increase their lengths up to the full length of the track.

Antifuse Connections

An antifuse is a "normally open" structure as opposed to the normally closed fuse structure used in PROMs or PALs. The use of antifuses to implement a programmable logic device results in highly testable structures as well as an efficient programming architecture. The structure is highly testable because there are no preexisting connections; temporary connections can be made using pass transistors. These temporary connections can isolate individual antifuses to be programmed as well as isolate individual circuit structures to be tested. This can be done both before and after programming. For example, all metal tracks can be tested for continuity and shorts between adjacent tracks, and the functionality of all logic modules can be verified.

Four types of antifuse connections are used in the routing structure of the ACT 3 array. (The physical structure of the antifuse is identical in each case; only the usage differs.)

Table 2-1 shows four types of antifuses.

Table 2-1 • **Antifuse Types**

Type	Description
XF	Horizontal-to-vertical connection
HF	Horizontal-to-horizontal connection
VF	Vertical-to-vertical connection
FF	"Fast" vertical connection

Examples of all four types of connections are shown in Figure 2-7 on page 2-6 and Figure 2-8 on page 2-6.

Module Interface

Connections to Logic and I/O modules are made through vertical segments that connect to the module inputs and outputs. These vertical segments lie on vertical tracks that span the entire height of the array.

Module Input Connections

The tracks dedicated to module inputs are segmented by pass transistors in each module row. During normal user operation, the pass transistors are inactive, which isolates the inputs of a module from the inputs of the module directly above or below it. During certain test modes, the pass transistors are active to verify the continuity of the metal tracks. Vertical input segments span only the channel above or the channel below. The logic modules are arranged such that half of the inputs are connected to the channel above and half of the inputs to segments in the channel below, as shown in Figure 2-9.
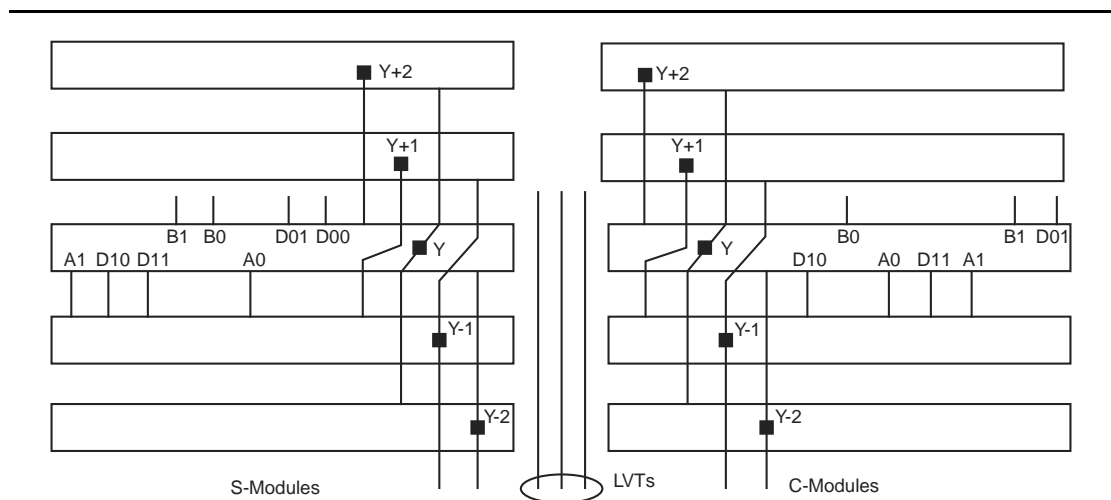

Figure 2-9 • **Logic Module Routing Interface**

5 V Operating Conditions

Table 2-2 • **Absolute Maximum Ratings[1], Free Air Temperature Range**

Symbol	Parameter	Limits	Units
VCC	DC supply voltage	−0.5 to +7.0	V
VI	Input voltage	−0.5 to VCC + 0.5	V
VO	Output voltage	−0.5 to VCC + 0.5	V
IIO	I/O source sink current[2]	±20	mA
T_{STG}	Storage temperature	−65 to +150	°C

Notes:

1. *Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum rated conditions for extended periods may affect device reliability. Device should not be operated outside the recommended operating conditions.*

2. *Device inputs are normally high impedance and draw extremely low current. However, when input voltage is greater than VCC + 0.5 V for less than GND −0.5 V, the internal protection diodes will forward bias and can draw excessive current.*

Table 2-3 • **Recommended Operating Conditions**

Parameter	Commercial	Industrial	Military	Units
Temperature range*	0 to +70	−40 to +85	−55 to +125	°C
5 V power supply tolerance	±5	±10	±10	%VCC

*Note: *Ambient temperature (T_A) is used for commercial and industrial; case temperature (T_C) is used for military.*

Table 2-4 • **Electrical Specifications**

Symbol	Parameter	Test Condition	Commercial Min.	Commercial Max.	Industrial Min.	Industrial Max.	Military Min.	Military Max.	Units
VOH[1,2]	High level output	IOH = −4 mA (CMOS)	–	–	3.7	–	3.7	–	V
		IOH = −6 mA (CMOS)	3.84						V
		IOH = −10 mA (TTL)[3]	2.40						V
VOL[1,2]	Low level output	IOL = +6 mA (CMOS)		0.33		0.4		0.4	V
		IOL = +12 mA (TTL)[3]		0.50					V
VIH	High level input	TTL inputs	2.0	VCC + 0.3	2.0	VCC + 0.3	2.0	VCC + 0.3	V
VIL	Low level input	TTL inputs	−0.3	0.8	−0.3	0.8	−0.3	0.8	V
IIN	Input leakage	VI = VCC or GND	−10	+10	−10	+10	−10	+10	µA
IOZ	3-state output leakage	VO = VCC or GND	−10	+10	−10	+10	−10	+10	µA
C_{IO}	I/O capacitance[3,4]			10		10		10	pF
ICC(S)	Standby VCC supply current (typical = 0.7 mA)			2		10		20	mA
ICC(D)	Dynamic VCC supply current. See the Power Dissipation section.								

Notes:

1. *Microsemi devices can drive and receive either CMOS or TTL signal levels. No assignment of I/Os as TTL or CMOS is required.*

2. *Tested one output at a time, VCC = minimum.*

3. *Not tested; for information only.*

4. *VOUT = 0 V, f = 1 MHz*

5. *Typical standby current = 0.7 mA. All outputs unloaded. All inputs = VCC or GND.*

3.3 V Operating Conditions

Table 2-5 • **Absolute Maximum Ratings[1], Free Air Temperature Range**

Symbol	Parameter	Limits	Units
VCC	DC supply voltage	−0.5 to +7.0	V
VI	Input voltage	−0.5 to VCC + 0.5	V
VO	Output voltage	−0.5 to VCC + 0.5	V
IIO	I/O source sink current[2]	±20	mA
T_{STG}	Storage temperature	−65 to +150	°C

Notes:

1. *Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum rated conditions for extended periods may affect device reliability. Device should not be operated outside the recommended operating conditions.*

2. *Device inputs are normally high impedance and draw extremely low current. However, when input voltage is greater than VCC + 0.5 V for less than GND −0.5 V, the internal protection diodes will forward bias and can draw excessive current.*

Table 2-6 • **Recommended Operating Conditions**

Parameter	Commercial	Units
Temperature range*	0 to +70	°C
Power supply tolerance	3.0 to 3.6	V

Note: *Ambient temperature (T_A) is used for commercial.*

Table 2-7 • **Electrical Specifications**

Parameter		Commercial		Units
		Min.	Max.	
VOH[1]	IOH = −4 mA	2.15	–	V
	IOH = −3.2 mA	2.4		V
VOL[1]	IOL = 6 mA		0.4	V
VIL		−0.3	0.8	V
VIH		2.0	VCC + 0.3	V
Input transition time t_R, t_F[2]	VI = VCC or GND	−10	+10	µA
C_{IO} I/O Capacitance[2,3]			10	pF
Standby current, ICC[4] (typical = 0.3 mA)			0.75	mA
Leakage current[5]		−10	10	µA

1. *Only one output tested at a time. VCC = minimum.*

2. *Not tested; for information only.*

3. *Includes worst-case 84-pin PLCC package capacitance. VOUT = 0 V, f - 1 MHz.*

4. *Typical standby current = 0.3 mA. All outputs unloaded. All inputs = VCC or GND.*

5. *VO, VIN = VCC or GND*

ACT 3 Timing Model
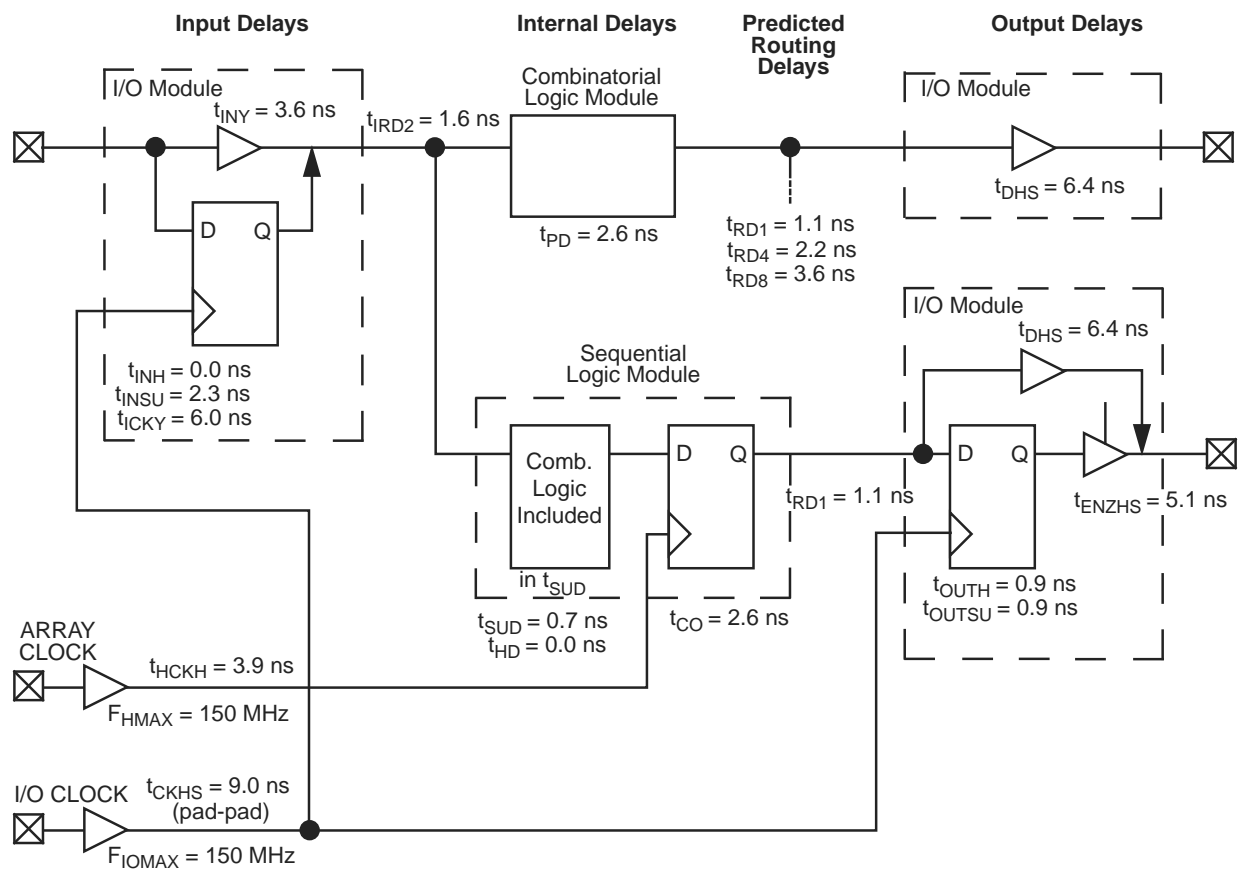
Note: Values shown for A1425A –1 speed grade device.

***Figure 2-10 •** **Timing Model**

Tightest Delay Distributions

Propagation delay between logic modules depends on the resistive and capacitive loading of the routing tracks, the interconnect elements, and the module inputs being driven. Propagation delay increases as the length of routing tracks, the number of interconnect elements, or the number of inputs increases.

From a design perspective, the propagation delay can be statistically correlated or modeled by the fanout (number of loads) driven by a module. Higher fanout usually requires some paths to have longer lengths of routing track. The ACT 3 family delivers the tightest fanout delay distribution of any FPGA. This tight distribution is achieved in two ways: by decreasing the delay of the interconnect elements and by decreasing the number of interconnect elements per path.

Microsemi's patented PLICE antifuse offers a very low resistive/capacitive interconnect. The ACT 3 family's antifuses, fabricated in 0.8 micron m lithography, offer nominal levels of 200Ω resistance and 6 femtofarad (fF) capacitance per antifuse. The ACT 3 fanout distribution is also tighter than alternative devices due to the low number of antifuses required per interconnect path. The ACT 3 family's proprietary architecture limits the number of antifuses per path to only four, with 90% of interconnects using only two antifuses.

The ACT 3 family's tight fanout delay distribution offers an FPGA design environment in which fanout can be traded for the increased performance of reduced logic level designs. This also simplifies performance estimates when designing with ACT 3 devices.

Table 2-14 • Logic Module and Routing Delay by Fanout (ns); Worst-Case Commercial Conditions

Speed Grade	FO = 1	FO = 2	FO = 3	FO = 4	FO = 8
ACT 3 –3	2.9	3.2	3.4	3.7	4.8
ACT 3 –2	3.3	3.7	3.9	4.2	5.5
ACT 3 –1	3.7	4.2	4.4	4.8	6.2
ACT 3 STD	4.3	4.8	5.1	5.5	7.2

Notes:

1. *Obtained by added $t_{RD(x=FO)}$ to t_{PD} from the Logic Module Timing Characteristics Tables found in this datasheet.*
2. *The –2 and –3 speed grades have been discontinued. Refer to PDN 0104, PDN 0203, PDN 0604, and PDN 1004 at http://www.microsemi.com/soc/support/notifications/default.aspx#pdn.*

Timing Characteristics

Timing characteristics for ACT 3 devices fall into three categories: family dependent, device dependent, and design dependent. The input and output buffer characteristics are common to all ACT 3 family members. Internal routing delays are device dependent. Design dependency means actual delays are not determined until after placement and routing of the user's design is complete. Delay values may then be determined by using the ALS Timer utility or performing simulation with post-layout delays.

Critical Nets and Typical Nets

Propagation delays are expressed only for typical nets, which are used for initial design performance evaluation. Critical net delays can then be applied to the most time-critical paths. Critical nets are determined by net property assignment prior to placement and routing. Up to 6% of the nets in a design may be designated as critical, while 90% of the nets in a design are typical.

Long Tracks

Some nets in the design use long tracks. Long tracks are special routing resources that span multiple rows, columns, or modules. Long tracks employ three and sometimes four antifuse connections. This increases capacitance and resistance, result ng in longer net delays for macros connected to long tracks. Typically up to 6% of nets in a fully utilized device require long tracks. Long tracks contribute approximately 4 ns to 14 ns delay. This additional delay is represented statistically in higher fanout (FO = 8) routing delays in the datasheet specifications section.

A1415A, A14V15A Timing Characteristics (continued)

Table 2-20 • **A1415A, A14V15A Worst-Case Commercial Conditions, VCC = 4.75 V, T$_J$ = 70°C**

I/O Module – TTL Output Timing[1]		–3 Speed[2]		–2 Speed[2]		–1 Speed		Std. Speed		3.3 V Speed[1]		Units
Parameter/Description		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t$_{DHS}$	Data to Pad, High Slew		5.0		5.6		6.4		7.5		9.8	ns
t$_{DLS}$	Data to Pad, Low Slew		8.0		9.0		10.2		12.0		15.6	ns
t$_{ENZHS}$	Enable to Pad, Z to H/L, High Slew		4.0		4.5		5.1		6.0		7.8	ns
t$_{ENZLS}$	Enable to Pad, Z to H/L, Low Slew		7.4		8.3		9.4		11.0		14.3	ns
t$_{ENHSZ}$	Enable to Pad, H/L to Z, High Slew		6.5		7.5		8.5		10.0		13.0	ns
t$_{ENLSZ}$	Enable to Pad, H/L to Z, Low Slew		6.5		7.5		8.5		10.0		13.0	ns
t$_{CKHS}$	IOCLK Pad to Pad H/L, High Slew		7.5		7.5		9.0		10.0		13.0	ns
t$_{CKLS}$	IOCLK Pad to Pad H/L, Low Slew		11.3		11.3		13.5		15.0		19.5	ns
d$_{TLHHS}$	Delta Low to High, High Slew		0.02		0.02		0.03		0.03		0.04	ns/pF
d$_{TLHLS}$	Delta Low to High, Low Slew		0.05		0.05		0.06		0.07		0.09	ns/pF
d$_{THLHS}$	Delta High to Low, High Slew		0.04		0.04		0.04		0.05		0.07	ns/pF
d$_{THLLS}$	Delta High to Low, Low Slew		0.05		0.05		0.06		0.07		0.09	ns/pF
I/O Module – CMOS Output Timing[1]												
t$_{DHS}$	Data to Pad, High Slew		6.2		7.0		7.9		9.3		12.1	ns
t$_{DLS}$	Data to Pad, Low Slew		11.7		13.1		14.9		17.5		22.8	ns
t$_{ENZHS}$	Enable to Pad, Z to H/L, High Slew		5.2		5.9		6.6		7.8		10.1	ns
t$_{ENZLS}$	Enable to Pad, Z to H/L, Low Slew		8.9		10.0		11.3		13.3		17.3	ns
t$_{ENHSZ}$	Enable to Pad, H/L to Z, High Slew		6.7		7.5		8.5		10.0		13.0	ns
t$_{ENLSZ}$	Enable to Pad, H/L to Z, Low Slew		6.7		7.5		9.0		10.0		13.0	ns
t$_{CKHS}$	IOCLK Pad to Pad H/L, High Slew		8.9		8.9		10.7		11.8		15.3	ns
t$_{CKLS}$	IOCLK Pad to Pad H/L, Low Slew		13.0		13.0		15.6		17.3		22.5	ns
d$_{TLHHS}$	Delta Low to High, High Slew		0.04		0.04		0.05		0.06		0.08	ns/pF
d$_{TLHLS}$	Delta Low to High, Low Slew		0.07		0.08		0.09		0.11		0.14	ns/pF
d$_{THLHS}$	Delta High to Low, High Slew		0.03		0.03		0.03		0.04		0.05	ns/pF
d$_{THLLS}$	Delta High to Low, Low Slew		0.04		0.04		0.04		0.05		0.07	ns/pF

Notes:

1. *Delays based on 35 pF loading.*

2. *The –2 and –3 speed grades have been discontinued. Please refer to the Product Discontinuation Notices (PDNs) listed below:*

   PDN March 2001
   PDN 0104
   PDN 0203
   PDN 0604
   PDN 1004

A1460A, A14V60A Timing Characteristics (continued)

Table 2-31 • A1460A, A14V60A Worst-Case Commercial Conditions, VCC = 4.75 V, T$_J$ = 70°C

I/O Module Input Propagation Delays		–3 Speed[1]		–2 Speed[1]		–1 Speed		Std. Speed		3.3 V Speed[1]		Units
Parameter/Description		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t$_{INY}$	Input Data Pad to Y		2.8		3.2		3.6		4.2		5.5	ns
t$_{ICKY}$	Input Reg IOCLK Pad to Y		4.7		5.3		6.0		7.0		9.2	ns
t$_{OCKY}$	Output Reg IOCLK Pad to Y		4.7		5.3		6.0		7.0		9.2	ns
t$_{ICLRY}$	Input Asynchronous Clear to Y		4.7		5.3		6.0		7.0		9.2	ns
t$_{OCLRY}$	Output Asynchronous Clear to Y		4.7		5.3		6.0		7.0		9.2	ns
Predicted Input Routing Delays[2]												
t$_{RD1}$	FO = 1 Routing Delay		0.9		1.0		1.1		1.3		1.7	ns
t$_{RD2}$	FO = 2 Routing Delay		1.2		1.4		1.6		1.8		2.4	ns
t$_{RD3}$	FO = 3 Routing Delay		1.4		1.6		1.8		2.1		2.8	ns
t$_{RD4}$	FO = 4 Routing Delay		1.7		1.9		2.2		2.5		3.3	ns
t$_{RD8}$	FO = 8 Routing Delay		2.8		3.2		3.6		4.2		5.5	ns
I/O Module Sequential Timing (wrt IOCLK pad)												
t$_{INH}$	Input F-F Data Hold	0.0		0.0		0.0		0.0		0.0		ns
t$_{INSU}$	Input F-F Data Setup	1.3		1.5		1.8		2.0		2.0		ns
t$_{IDEH}$	Input Data Enable Hold	0.0		0.0		0.0		0.0		0.0		ns
t$_{IDESU}$	Input Data Enable Setup	5.8		6.5		7.5		8.6		8.6		ns
t$_{OUTH}$	Output F-F Data hold	0.7		0.8		0.9		1.0		1.0		ns
t$_{OUTSU}$	Output F-F Data Setup	0.7		0.8		0.9		1.0		1.0		ns
t$_{ODEH}$	Output Data Enable Hold	0.3		0.4		0.4		0.5		0.5		ns
f$_{ODESU}$	Output Data Enable Setup	1.3		1.5		1.7		2.0		2.0		ns

Notes:

5. The –2 and –3 speed grades have been discontinued. Refer to PDN 0104, PDN 0203, PDN 0604, and PDN 1004 at http://www.microsemi.com/soc/support/notifications/default.aspx#pdn.

6. Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual worst-case performance. Post-route timing is based on actual routing delay measurements performed on the device prior to shipment.

A1460A, A14V60A Timing Characteristics (continued)

Table 2-32 • **A1460A, A14V60A Worst-Case Commercial Conditions, VCC = 4.75 V, T$_J$ = 70°C**

I/O Module – TTL Output Timing[1]		–3 Speed[2]		–2 Speed[2]		–1 Speed		Std. Speed		3.3 V Speed[1]		Units
Parameter/Description		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t$_{DHS}$	Data to Pad, High Slew		5.0		5.6		6.4		7.5		9.8	ns
t$_{DLS}$	Data to Pad, Low Slew		8.0		9.0		10.2		12.0		15.6	ns
t$_{ENZHS}$	Enable to Pad, Z to H/L, High Slew		4.0		4.5		5.1		6.0		7.8	ns
t$_{ENZLS}$	Enable to Pad, Z to H/L, Low Slew		7.4		8.3		9.4		11.0		14.3	ns
t$_{ENHSZ}$	Enable to Pad, H/L to Z, High Slew		7.8		8.7		9.9		11.6		15.1	ns
t$_{ENLSZ}$	Enable to Pad, H/L to Z, Low Slew		7.4		8.3		9.4		11.0		14.3	ns
t$_{CKHS}$	IOCLK Pad to Pad H/L, High Slew		9.0		9.0		10.0		11.5		15.0	ns
t$_{CKLS}$	IOCLK Pad to Pad H/L, Low Slew		12.8		12.8		15.3		17.0		22.1	ns
d$_{TLHHS}$	Delta Low to High, High Slew		0.02		0.02		0.03		0.03		0.04	ns/pF
d$_{TLHLS}$	Delta Low to High, Low Slew		0.05		0.05		0.06		0.07		0.09	ns/pF
d$_{THLHS}$	Delta High to Low, High Slew		0.04		0.04		0.04		0.05		0.07	ns/pF
d$_{THLLS}$	Delta High to Low, Low Slew		0.05		0.05		0.06		0.07		0.09	ns/pF
I/O Module – CMOS Output Timing[1]												
t$_{DHS}$	Data to Pad, High Slew		6.2		7.0		7.9		9.3		12.1	ns
t$_{DLS}$	Data to Pad, Low Slew		11.7		13.1		14.9		17.5		22.8	ns
t$_{ENZHS}$	Enable to Pad, Z to H/L, High Slew		5.2		5.9		6.6		7.8		10.1	ns
t$_{ENZLS}$	Enable to Pad, Z to H/L, Low Slew		8.9		10.0		11.3		13.3		17.3	ns
t$_{ENHSZ}$	Enable to Pad, H/L to Z, High Slew		7.4		8.3		9.4		11.0		14.3	ns
t$_{ENLSZ}$	Enable to Pad, H/L to Z, Low Slew		7.4		8.3		9.4		11.0		14.3	ns
t$_{CKHS}$	IOCLK Pad to Pad H/L, High Slew		10.4		10.4		12.1		13.8		17.9	ns
t$_{CKLS}$	IOCLK Pad to Pad H/L, Low Slew		14.5		14.5		17.4		19.3		25.1	ns
d$_{TLHHS}$	Delta Low to High, High Slew		0.04		0.04		0.05		0.06		0.08	ns/pF
d$_{TLHLS}$	Delta Low to High, Low Slew		0.07		0.08		0.09		0.11		0.14	ns/pF
d$_{THLHS}$	Delta High to Low, High Slew		0.03		0.03		0.03		0.04		0.05	ns/pF
d$_{THLLS}$	Delta High to Low, Low Slew		0.04		0.04		0.04		0.05		0.07	ns/pF

Notes:

1. *Delays based on 35 pF loading.*
2. *The –2 and –3 speed grades have been discontinued. Refer to PDN 0104, PDN 0203, PDN 0604, and PDN 1004 at http://www.microsemi.com/soc/support/notifications/default.aspx#pdn.*

A14100A, A14V100A Timing Characteristics

Table 2-34 • A14100A, A14V100A Worst-Case Commercial Conditions, VCC = 4.75 V, T_J = 70°C[1]

Logic Module Propagation Delays[2]		−3 Speed[3]		−2 Speed[3]		−1 Speed		Std. Speed		3.3 V Speed[1]		Units
Parameter/Description		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t_{PD}	Internal Array Module		2.0		2.3		2.6		3.0		3.9	ns
t_{CO}	Sequential Clock to Q		2.0		2.3		2.6		3.0		3.9	ns
t_{CLR}	Asynchronous Clear to Q		2.0		2.3		2.6		3.0		3.9	ns
Predicted Routing Delays[4]												
t_{RD1}	FO = 1 Routing Delay		0.9		1.0		1.1		1.3		1.7	ns
t_{RD2}	FO = 2 Routing Delay		1.2		1.4		1.6		1.8		2.4	ns
t_{RD3}	FO = 3 Routing Delay		1.4		1.6		1.8		2.1		2.8	ns
t_{RD4}	FO = 4 Routing Delay		1.7		1.9		2.2		2.5		3.3	ns
t_{RD8}	FO = 8 Routing Delay		2.8		3.2		3.6		4.2		5.5	ns
Logic Module Sequential Timing												
t_{SUD}	Flip-Flop Data Input Setup	0.5		0.6		0.8		0.8		0.8		ns
t_{HD}	Flip-Flop Data Input Hold	0.0		0.0		0.5		0.5		0.5		ns
t_{SUD}	Latch Data Input Setup	0.5		0.6		0.8		0.8		0.8		ns
t_{HD}	Latch Data Input Hold	0.0		0.0		0.5		0.5		0.5		ns
t_{WASYN}	Asynchronous Pulse Width	2.4		3.2		3.8		4.8		6.5		ns
t_{WCLKA}	Flip-Flop Clock Pulse Width	2.4		3.2		3.8		4.8		6.5		ns
t_A	Flip-Flop Clock Input Period	5.0		6.8		8.0		10.0		13.4		ns
f_{MAX}	Flip-Flop Clock Frequency		200		150		125		100		75	MHz

Notes:

1. *VCC = 3.0 V for 3.3 V specifications.*

2. *For dual-module macros, use $t_{PD} + t_{RD1} + t_{PDn} + t_{CO} + t_{RD1} + t_{PDn}$ or $t_{PD1} + t_{RD1} + t_{SUD}$, whichever is appropriate.*

3. *The −2 and −3 speed grades have been discontinued. Refer to PDN 0104, PDN 0203, PDN 0604, and PDN 1004 at http://www.microsemi.com/soc/support/notifications/default.aspx#pdn.*

4. *Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual worst-case performance. Post-route timing is based on actual routing delay measurements performed on the device prior to shipment.*

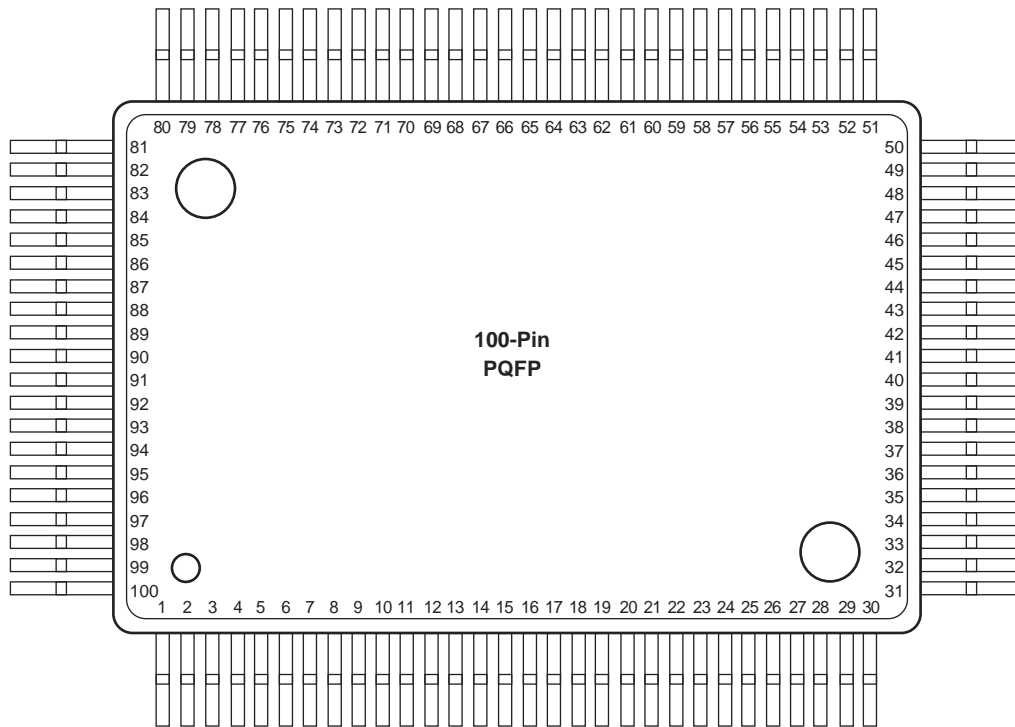## *A14100A, A14V100A Timing Characteristics (continued)*

Table 2-36 • **A14100A, A14V100A Worst-Case Commercial Conditions, VCC = 4.75 V, T_J = 70°C**

I/O Module – TTL Output Timing[1]		–3 Speed[2]		–2 Speed[2]		–1 Speed		Std. Speed		3.3 V Speed[1]		Units
Parameter/Description		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t_{DHS}	Data to Pad, High Slew		5.0		5.6		6.4		7.5		9.8	ns
t_{DLS}	Data to Pad, Low Slew		8.0		9.0		10.2		12.0		15.6	ns
t_{ENZHS}	Enable to Pad, Z to H/L, High Slew		4.0		4.5		5.1		6.0		7.8	ns
t_{ENZLS}	Enable to Pad, Z to H/L, Low Slew		7.4		8.3		9.4		11.0		14.3	ns
t_{ENHSZ}	Enable to Pad, H/L to Z, High Slew		8.0		9.0		10.2		12.0		15.6	ns
t_{ENLSZ}	Enable to Pad, H/L to Z, Low Slew		7.4		8.3		9.4		11.0		14.3	ns
t_{CKHS}	IOCLK Pad to Pad H/L, High Slew		9.5		9.5		10.5		12.0		15.6	ns
t_{CKLS}	IOCLK Pad to Pad H/L, Low Slew		12.8		12.8		15.3		17.0		22.1	ns
d_{TLHHS}	Delta Low to High, High Slew		0.02		0.02		0.03		0.03		0.04	ns/pF
d_{TLHLS}	Delta Low to High, Low Slew		0.05		0.05		0.06		0.07		0.09	ns/pF
d_{THLHS}	Delta High to Low, High Slew		0.04		0.04		0.04		0.05		0.07	ns/pF
d_{THLLS}	Delta High to Low, Low Slew		0.05		0.05		0.06		0.07		0.09	ns/pF
I/O Module – CMOS Output Timing[1]												
t_{DHS}	Data to Pad, High Slew		6.2		7.0		7.9		9.3		12.1	ns
t_{DLS}	Data to Pad, Low Slew		11.7		13.1		14.9		17.5		22.8	ns
t_{ENZHS}	Enable to Pad, Z to H/L, High Slew		5.2		5.9		6.6		7.8		10.1	ns
t_{ENZLS}	Enable to Pad, Z to H/L, Low Slew		8.9		10.0		11.3		13.3		17.3	ns
t_{ENHSZ}	Enable to Pad, H/L to Z, High Slew		8.0		9.0		10.0		12.0		15.6	ns
t_{ENLSZ}	Enable to Pad, H/L to Z, Low Slew		7.4		8.3		9.4		11.0		14.3	ns
t_{CKHS}	IOCLK Pad to Pad H/L, High Slew		10.4		10.4		12.4		13.8		17.9	ns
t_{CKLS}	IOCLK Pad to Pad H/L, Low Slew		14.5		14.5		17.4		19.3		25.1	ns
d_{TLHHS}	Delta Low to High, High Slew		0.04		0.04		0.05		0.06		0.08	ns/pF
d_{TLHLS}	Delta Low to High, Low Slew		0.07		0.08		0.09		0.11		0.14	ns/pF
d_{THLHS}	Delta High to Low, High Slew		0.03		0.03		0.03		0.04		0.05	ns/pF
d_{THLLS}	Delta High to Low, Low Slew		0.04		0.04		0.04		0.05		0.07	ns/pF

Notes: *

1. Delays based on 35 pF loading.

2. The –2 and –3 speed grades have been discontinued. Refer to PDN 0104, PDN 0203, PDN 0604, and PDN 1004 at http://www.microsemi.com/soc/support/notifications/default.aspx#pdn.

PQ100

**100-Pin
PQFP**

Note: This is the top view of the package.

Note

For Package Manufacturing and Environmental information, visit the Resource Center at
http://www.microsemi.com/soc/products/solutions/package/docs.aspx

BG225	
A1460 Function	**Location**
CLKA or I/O	C8
CLKB or I/O	B8
DCLK or I/O	B2
GND	A1, A15, D15, F8, G7, G8, G9, H6, H7, H8, H9, H10, J7, J8, J9, K8, P2, R15
HCLK or I/O	P9
IOCLK or I/O	B14
IOPCL or I/O	P14
MODE	D1
NC	A11, B5, B7, D8, D12, F6, F11, H1, H12, H14, K11, L1, L13, N8, P5, R1, R8, R11, R14
PRA or I/O	A7
PRB or I/O	L7
SDI or I/O	D4
SDO	N13
VCC	A8, B12, D5, D14, E3, E8, E13, H2, H3, H11, H15, K4, L2, L12, M8, M15, P4, P8, R13

Notes:

1. All unlisted pin numbers are user I/Os.
2. NC denotes no connection.
3. MODE should be terminated to GND through a 10K resistor to enable Actionprobe usage; otherwise it can be terminated directly to GND.
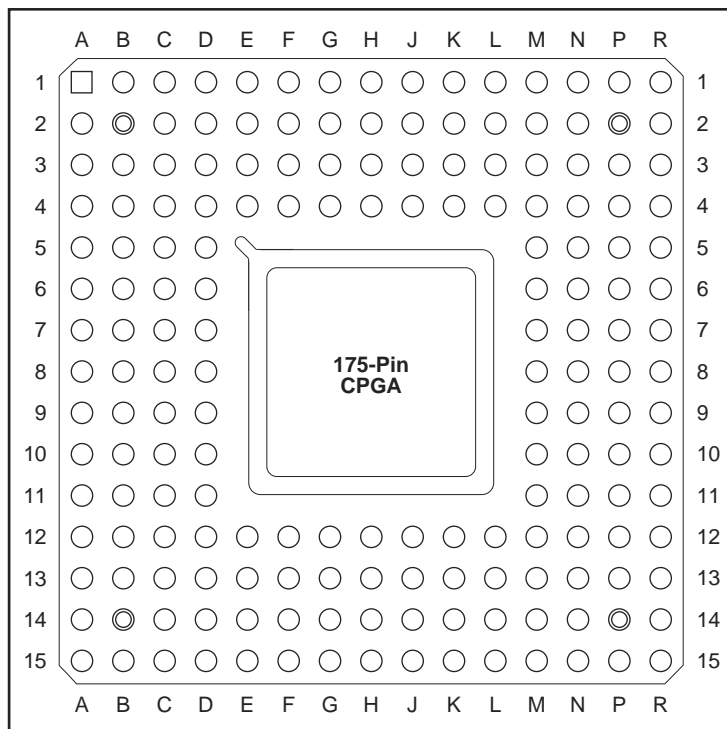4. The BG225 package has been discontinued.

PG133

Note: This is the top view.

Note

For Package Manufacturing and Environmental information, visit the Resource Center at
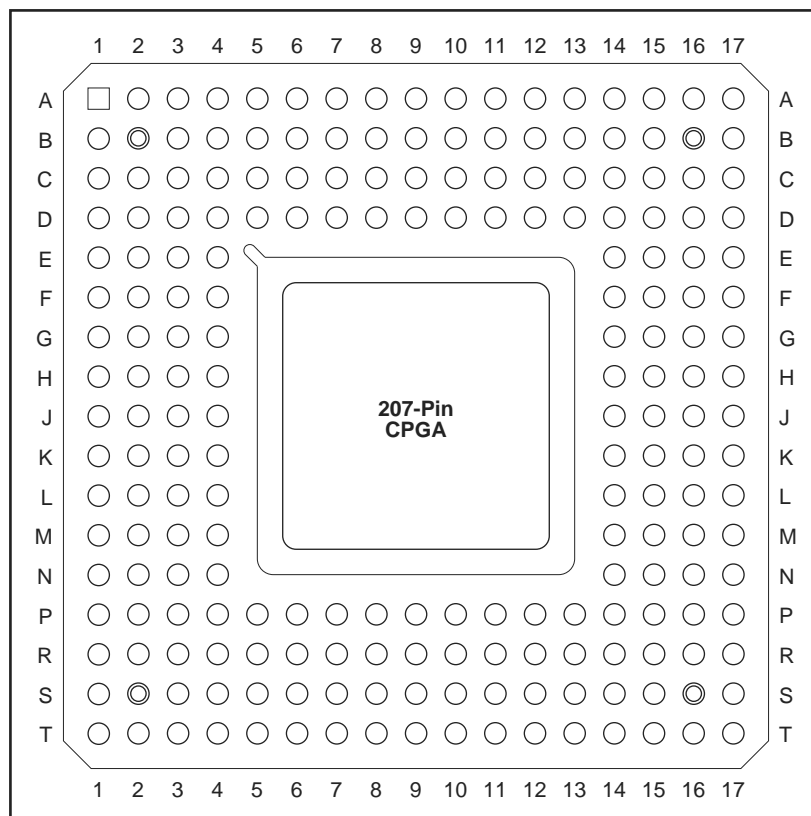http://www.microsemi.com/soc/products/solutions/package/docs.aspx

PG175

Note: This is the top view.

Note

For Package Manufacturing and Environmental information, visit the Resource Center at
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PG207

Note: This is the top view.

Note

For Package Manufacturing and Environmental information, visit the Resource Center at
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