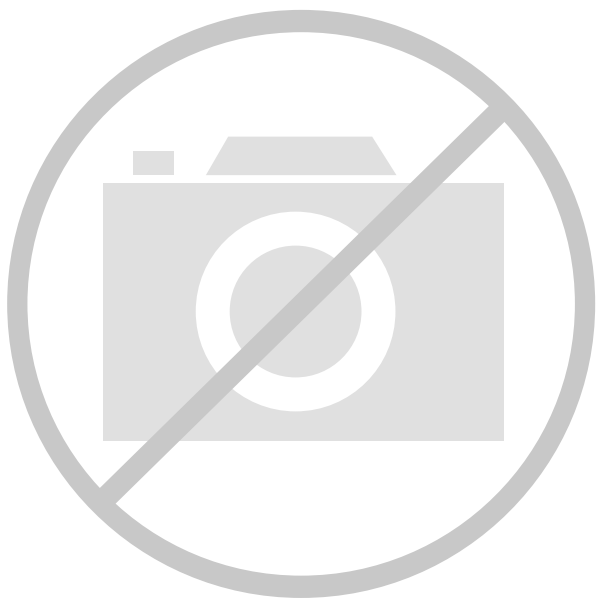




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Understanding [Embedded - FPGAs \(Field Programmable Gate Array\)](#)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Obsolete
Number of LABs/CLBs	564
Number of Logic Elements/Cells	-
Total RAM Bits	-
Number of I/O	131
Number of Gates	4000
Voltage - Supply	4.5V ~ 5.5V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 85°C (TA)
Package / Case	160-BQFP
Supplier Device Package	160-PQFP (28x28)
Purchase URL	https://www.e-xfl.com/product-detail/microsemi/a1440a-pq160i

ACT 3 Family Overview

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The S-module contains a full implementation of the C-module plus a clearable sequential element that can either implement a latch or flip-flop function. The S-module can therefore implement any function implemented by the C-module. This allows complex combinatorial-sequential functions to be implemented with no delay penalty. The Designer Series Development System will automatically combine any C-module macro driving an S-module macro into the S-module, thereby freeing up a logic module and eliminating a module delay.

The clear input CLR is accessible from the routing channel. In addition, the clock input may be connected to one of three clock networks: CLKA, CLKB, or HCLK. The C-module and S-module functional descriptions are shown in [Figure 2-2](#) and [Figure 2-3 on page 2-2](#). The clock selection is determined by a multiplexer select at the clock input to the S-module.

I/Os

I/O Modules

I/O modules provide an interface between the array and the I/O Pad Drivers. I/O modules are located in the array and access the routing channels in a similar fashion to logic modules. The I/O module schematic is shown in [Figure 4](#). The signals DataIn and DataOut connect to the I/O pad driver.

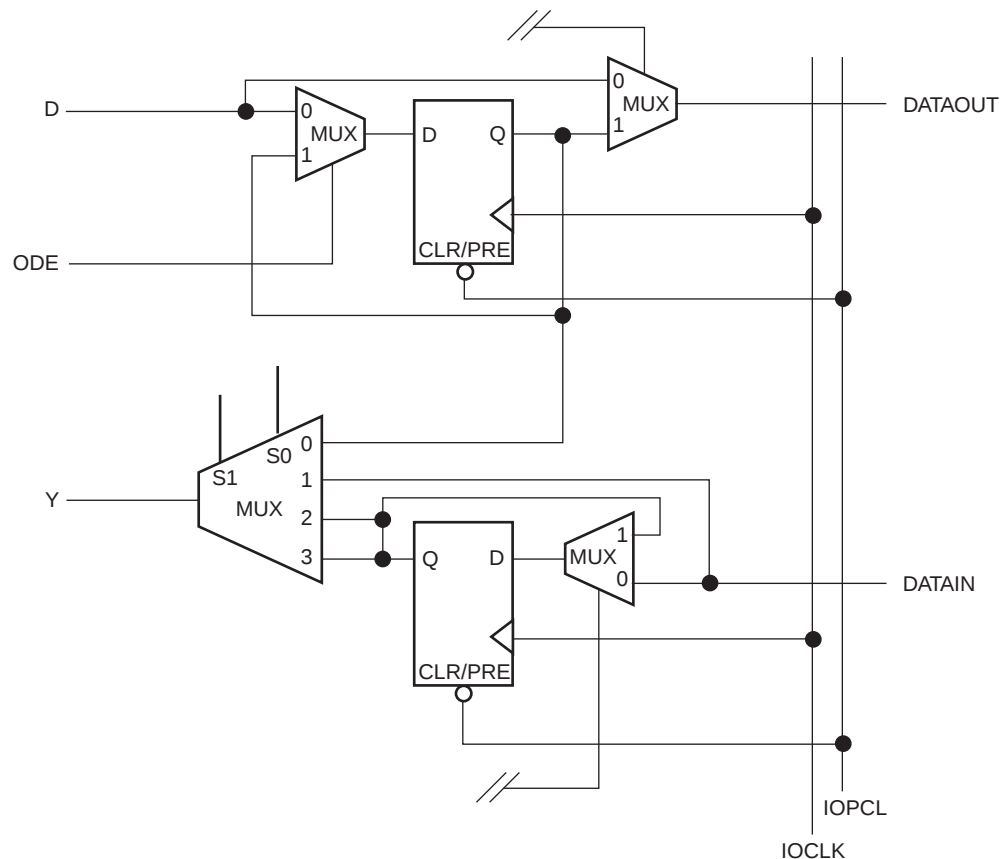


Figure 2-4 • Functional Diagram for I/O Module

Each I/O module contains two D-type flip-flops. Each flip-flop is connected to the dedicated I/O clock (IOCLK). Each flip-flop can be bypassed by nonsequential I/Os. In addition, each flip-flop contains a data enable input that can be accessed from the routing channels (ODE and IDE). The asynchronous preset/clear input is driven by the dedicated preset/clear network (IOPCL). Either preset or clear can be selected individually on an I/O module by I/O module basis.

Horizontal Routing

Horizontal channels are located between the rows of modules and are composed of several routing tracks. The horizontal routing tracks within the channel are divided into one or more segments. The minimum horizontal segment length is the width of a module-pair, and the maximum horizontal segment length is the full length of the channel. Any segment that spans more than one-third the row length is considered a long horizontal segment. A typical channel is shown in [Figure 2-7](#). Undedicated horizontal routing tracks are used to route signal nets. Dedicated routing tracks are used for the global clock networks and for power and ground tie-off tracks.

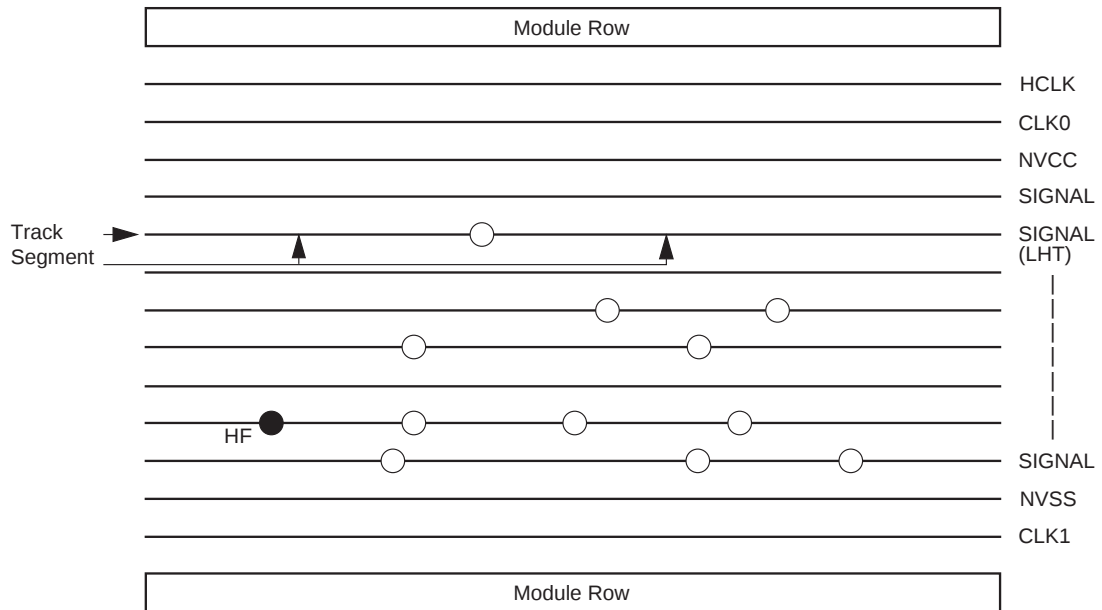


Figure 2-7 • Horizontal Routing Tracks and Segments

Vertical Routing

Other tracks run vertically through the modules. Vertical tracks are of three types: input, output, and long. Vertical tracks are also divided into one or more segments. Each segment in an input track is dedicated to the input of a particular module. Each segment in an output track is dedicated to the output of a particular module. Long segments are uncommitted and can be assigned during routing. Each output segment spans four channels (two above and two below), except near the top and bottom of the array where edge effects occur. LVTs contain either one or two segments. An example of vertical routing tracks and segments is shown in [Figure 2-8](#).

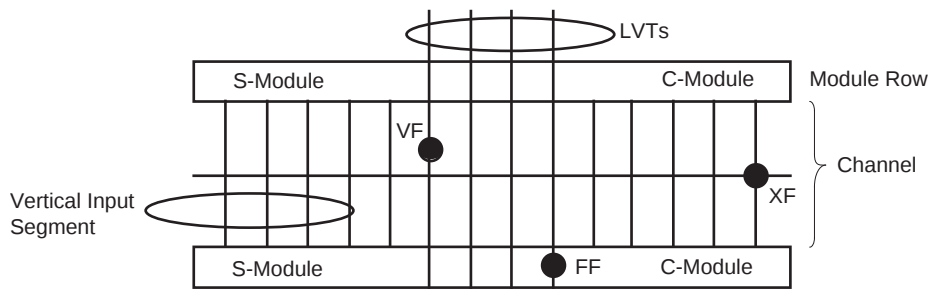


Figure 2-8 • Vertical Routing Tracks and Segments

A1415A, A14V15A Timing Characteristics

Table 2-18 • A1415A, A14V15A Worst-Case Commercial Conditions, VCC = 4.75 V, T_J = 70°C¹

Logic Module Propagation Delays ²		–3 Speed ³		–2 Speed ³		–1 Speed		Std. Speed		3.3 V Speed ¹		Units
Parameter/Description		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t _{PD}	Internal Array Module		2.0		2.3		2.6		3.0		3.9	ns
t _{CO}	Sequential Clock to Q		2.0		2.3		2.6		3.0		3.9	ns
t _{CLR}	Asynchronous Clear to Q		2.0		2.3		2.6		3.0		3.9	ns
Predicted Routing Delays⁴												
t _{RD1}	FO = 1 Routing Delay		0.9		1.0		1.1		1.3		1.7	ns
t _{RD2}	FO = 2 Routing Delay		1.2		1.4		1.6		1.8		2.4	ns
t _{RD3}	FO = 3 Routing Delay		1.4		1.6		1.8		2.1		2.8	ns
t _{RD4}	FO = 4 Routing Delay		1.7		1.9		2.2		2.5		3.3	ns
t _{RD8}	FO = 8 Routing Delay		2.8		3.2		3.6		4.2		5.5	ns
Logic Module Sequential Timing												
t _{SUD}	Flip-Flop Data Input Setup	0.5		0.6		0.7		0.8		0.8		ns
t _{HD}	Flip-Flop Data Input Hold	0.0		0.0		0.0		0.0		0.0		ns
t _{SUD}	Latch Data Input Setup	0.5		0.6		0.7		0.8		0.8		ns
t _{HD}	Latch Data Input Hold	0.0		0.0		0.0		0.0		0.0		ns
t _{WASYN}	Asynchronous Pulse Width	1.9		2.4		3.2		3.8		4.8		ns
t _{WCLKA}	Flip-Flop Clock Pulse Width	1.9		2.4		3.2		3.8		4.8		ns
t _A	Flip-Flop Clock Input Period	4.0		5.0		6.8		8.0		10.0		ns
f _{MAX}	Flip-Flop Clock Frequency		250		200		150		125		100	MHz

Notes:

- VCC = 3.0 V for 3.3 V specifications.
- For dual-module macros, use t_{PD} + t_{RD1} + t_{PDn} + t_{CO} + t_{RD1} + t_{PDn} or t_{PD1} + t_{RD1} + t_{SUD}, whichever is appropriate.
- The –2 and –3 speed grades have been discontinued. Please refer to the Product Discontinuation Notices (PDNs) listed below:
[PDN March 2001](#)
[PDN 0104](#)
[PDN 0203](#)
[PDN 0604](#)
[PDN 1004](#)
- Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual worst-case performance. Post-route timing is based on actual routing delay measurements performed on the device prior to shipment.

A1415A, A14V15A Timing Characteristics (continued)

Table 2-20 • A1415A, A14V15A Worst-Case Commercial Conditions, VCC = 4.75 V, T_J = 70°C

I/O Module – TTL Output Timing ¹		–3 Speed ²		–2 Speed ²		–1 Speed		Std. Speed		3.3 V Speed ¹		Units
Parameter/Description		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t _{DHS}	Data to Pad, High Slew		5.0		5.6		6.4		7.5		9.8	ns
t _{DLS}	Data to Pad, Low Slew		8.0		9.0		10.2		12.0		15.6	ns
t _{ENZHS}	Enable to Pad, Z to H/L, High Slew		4.0		4.5		5.1		6.0		7.8	ns
t _{ENZLS}	Enable to Pad, Z to H/L, Low Slew		7.4		8.3		9.4		11.0		14.3	ns
t _{ENHSZ}	Enable to Pad, H/L to Z, High Slew		6.5		7.5		8.5		10.0		13.0	ns
t _{ENLSZ}	Enable to Pad, H/L to Z, Low Slew		6.5		7.5		8.5		10.0		13.0	ns
t _{CKHS}	IOCLK Pad to Pad H/L, High Slew		7.5		7.5		9.0		10.0		13.0	ns
t _{CKLS}	IOCLK Pad to Pad H/L, Low Slew		11.3		11.3		13.5		15.0		19.5	ns
d _{TLHHS}	Delta Low to High, High Slew		0.02		0.02		0.03		0.03		0.04	ns/pF
d _{TLHLS}	Delta Low to High, Low Slew		0.05		0.05		0.06		0.07		0.09	ns/pF
d _{THLHS}	Delta High to Low, High Slew		0.04		0.04		0.04		0.05		0.07	ns/pF
d _{THLLS}	Delta High to Low, Low Slew		0.05		0.05		0.06		0.07		0.09	ns/pF
I/O Module – CMOS Output Timing ¹												
t _{DHS}	Data to Pad, High Slew		6.2		7.0		7.9		9.3		12.1	ns
t _{DLS}	Data to Pad, Low Slew		11.7		13.1		14.9		17.5		22.8	ns
t _{ENZHS}	Enable to Pad, Z to H/L, High Slew		5.2		5.9		6.6		7.8		10.1	ns
t _{ENZLS}	Enable to Pad, Z to H/L, Low Slew		8.9		10.0		11.3		13.3		17.3	ns
t _{ENHSZ}	Enable to Pad, H/L to Z, High Slew		6.7		7.5		8.5		10.0		13.0	ns
t _{ENLSZ}	Enable to Pad, H/L to Z, Low Slew		6.7		7.5		9.0		10.0		13.0	ns
t _{CKHS}	IOCLK Pad to Pad H/L, High Slew		8.9		8.9		10.7		11.8		15.3	ns
t _{CKLS}	IOCLK Pad to Pad H/L, Low Slew		13.0		13.0		15.6		17.3		22.5	ns
d _{TLHHS}	Delta Low to High, High Slew		0.04		0.04		0.05		0.06		0.08	ns/pF
d _{TLHLS}	Delta Low to High, Low Slew		0.07		0.08		0.09		0.11		0.14	ns/pF
d _{THLHS}	Delta High to Low, High Slew		0.03		0.03		0.03		0.04		0.05	ns/pF
d _{THLLS}	Delta High to Low, Low Slew		0.04		0.04		0.04		0.05		0.07	ns/pF

Notes:

- Delays based on 35 pF loading.
- The –2 and –3 speed grades have been discontinued. Please refer to the Product Discontinuation Notices (PDNs) listed below:

[PDN March 2001](#)
[PDN 0104](#)
[PDN 0203](#)
[PDN 0604](#)
[PDN 1004](#)

A1425A, A14V25A Timing Characteristics (continued)

Table 2-23 • A1425A, A14V25A Worst-Case Commercial Conditions, VCC = 4.75 V, T_J = 70°C

I/O Module Input Propagation Delays		–3 Speed ¹		–2 Speed ¹		–1 Speed		Std. Speed		3.3 V Speed ¹		Units
Parameter/Description		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t _{INY}	Input Data Pad to Y		2.8		3.2		3.6		4.2		5.5	ns
t _{ICKY}	Input Reg IOCLK Pad to Y		4.7		5.3		6.0		7.0		9.2	ns
t _{OCKY}	Output Reg IOCLK Pad to Y		4.7		5.3		6.0		7.0		9.2	ns
t _{ICLRY}	Input Asynchronous Clear to Y		4.7		5.3		6.0		7.0		9.2	ns
t _{OCLRY}	Output Asynchronous Clear to Y		4.7		5.3		6.0		7.0		9.2	ns
Predicted Input Routing Delays²												
t _{RD1}	FO = 1 Routing Delay		0.9		1.0		1.1		1.3		1.7	ns
t _{RD2}	FO = 2 Routing Delay		1.2		1.4		1.6		1.8		2.4	ns
t _{RD3}	FO = 3 Routing Delay		1.4		1.6		1.8		2.1		2.8	ns
t _{RD4}	FO = 4 Routing Delay		1.7		1.9		2.2		2.5		3.3	ns
t _{RD8}	FO = 8 Routing Delay		2.8		3.2		3.6		4.2		5.5	ns
I/O Module Sequential Timing (wrt IOCLK pad)												
t _{INH}	Input F-F Data Hold	0.0		0.0		0.0		0.0		0.0		ns
t _{INSU}	Input F-F Data Setup	1.8		2.0		2.3		2.7		3.0		ns
t _{IDEH}	Input Data Enable Hold	0.0		0.0		0.0		0.0		0.0		ns
t _{IDESU}	Input Data Enable Setup	5.8		6.5		7.5		8.6		8.6		ns
t _{OUTH}	Output F-F Data hold	0.7		0.8		0.9		1.0		1.0		ns
t _{OUTSU}	Output F-F Data Setup	0.7		0.8		0.9		1.0		1.0		ns
t _{ODEH}	Output Data Enable Hold	0.3		0.4		0.4		0.5		0.5		ns
f _{ODESU}	Output Data Enable Setup	1.3		1.5		1.7		2.0		2.0		ns

Notes: *

1. The –2 and –3 speed grades have been discontinued. Refer to [PDN 0104](http://www.microsemi.com/soc/support/notifications/default.aspx#pdn), [PDN 0203](http://www.microsemi.com/soc/support/notifications/default.aspx#pdn), [PDN 0604](http://www.microsemi.com/soc/support/notifications/default.aspx#pdn), and [PDN 1004](http://www.microsemi.com/soc/support/notifications/default.aspx#pdn) at <http://www.microsemi.com/soc/support/notifications/default.aspx#pdn>.
2. Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual worst-case performance. Post-route timing is based on actual routing delay measurements performed on the device prior to shipment.

A14100A, A14V100A Timing Characteristics (continued)

Table 2-36 • A14100A, A14V100A Worst-Case Commercial Conditions, VCC = 4.75 V, T_J = 70°C

I/O Module – TTL Output Timing ¹		–3 Speed ²		–2 Speed ²		–1 Speed		Std. Speed		3.3 V Speed ¹		Units
Parameter/Description		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t _{DHS}	Data to Pad, High Slew		5.0		5.6		6.4		7.5		9.8	ns
t _{DLS}	Data to Pad, Low Slew		8.0		9.0		10.2		12.0		15.6	ns
t _{ENZHS}	Enable to Pad, Z to H/L, High Slew		4.0		4.5		5.1		6.0		7.8	ns
t _{ENZLS}	Enable to Pad, Z to H/L, Low Slew		7.4		8.3		9.4		11.0		14.3	ns
t _{ENHSZ}	Enable to Pad, H/L to Z, High Slew		8.0		9.0		10.2		12.0		15.6	ns
t _{ENLSZ}	Enable to Pad, H/L to Z, Low Slew		7.4		8.3		9.4		11.0		14.3	ns
t _{CKHS}	IOCLK Pad to Pad H/L, High Slew		9.5		9.5		10.5		12.0		15.6	ns
t _{CKLS}	IOCLK Pad to Pad H/L, Low Slew		12.8		12.8		15.3		17.0		22.1	ns
d _{TLHHS}	Delta Low to High, High Slew		0.02		0.02		0.03		0.03		0.04	ns/pF
d _{TLHLS}	Delta Low to High, Low Slew		0.05		0.05		0.06		0.07		0.09	ns/pF
d _{THLHS}	Delta High to Low, High Slew		0.04		0.04		0.04		0.05		0.07	ns/pF
d _{THLLS}	Delta High to Low, Low Slew		0.05		0.05		0.06		0.07		0.09	ns/pF
I/O Module – CMOS Output Timing ¹												
t _{DHS}	Data to Pad, High Slew		6.2		7.0		7.9		9.3		12.1	ns
t _{DLS}	Data to Pad, Low Slew		11.7		13.1		14.9		17.5		22.8	ns
t _{ENZHS}	Enable to Pad, Z to H/L, High Slew		5.2		5.9		6.6		7.8		10.1	ns
t _{ENZLS}	Enable to Pad, Z to H/L, Low Slew		8.9		10.0		11.3		13.3		17.3	ns
t _{ENHSZ}	Enable to Pad, H/L to Z, High Slew		8.0		9.0		10.0		12.0		15.6	ns
t _{ENLSZ}	Enable to Pad, H/L to Z, Low Slew		7.4		8.3		9.4		11.0		14.3	ns
t _{CKHS}	IOCLK Pad to Pad H/L, High Slew		10.4		10.4		12.4		13.8		17.9	ns
t _{CKLS}	IOCLK Pad to Pad H/L, Low Slew		14.5		14.5		17.4		19.3		25.1	ns
d _{TLHHS}	Delta Low to High, High Slew		0.04		0.04		0.05		0.06		0.08	ns/pF
d _{TLHLS}	Delta Low to High, Low Slew		0.07		0.08		0.09		0.11		0.14	ns/pF
d _{THLHS}	Delta High to Low, High Slew		0.03		0.03		0.03		0.04		0.05	ns/pF
d _{THLLS}	Delta High to Low, Low Slew		0.04		0.04		0.04		0.05		0.07	ns/pF

Notes: *

- Delays based on 35 pF loading.
- The –2 and –3 speed grades have been discontinued. Refer to [PDN 0104](http://www.microsemi.com/soc/support/notifications/default.aspx#pdn), [PDN 0203](http://www.microsemi.com/soc/support/notifications/default.aspx#pdn), [PDN 0604](http://www.microsemi.com/soc/support/notifications/default.aspx#pdn), and [PDN 1004](http://www.microsemi.com/soc/support/notifications/default.aspx#pdn) at <http://www.microsemi.com/soc/support/notifications/default.aspx#pdn>.

A14100A, A14V100A Timing Characteristics (continued)

Table 2-37 • A14100A, A14V100A Worst-Case Commercial Conditions, VCC = 4.75 V, T_J = 70°C

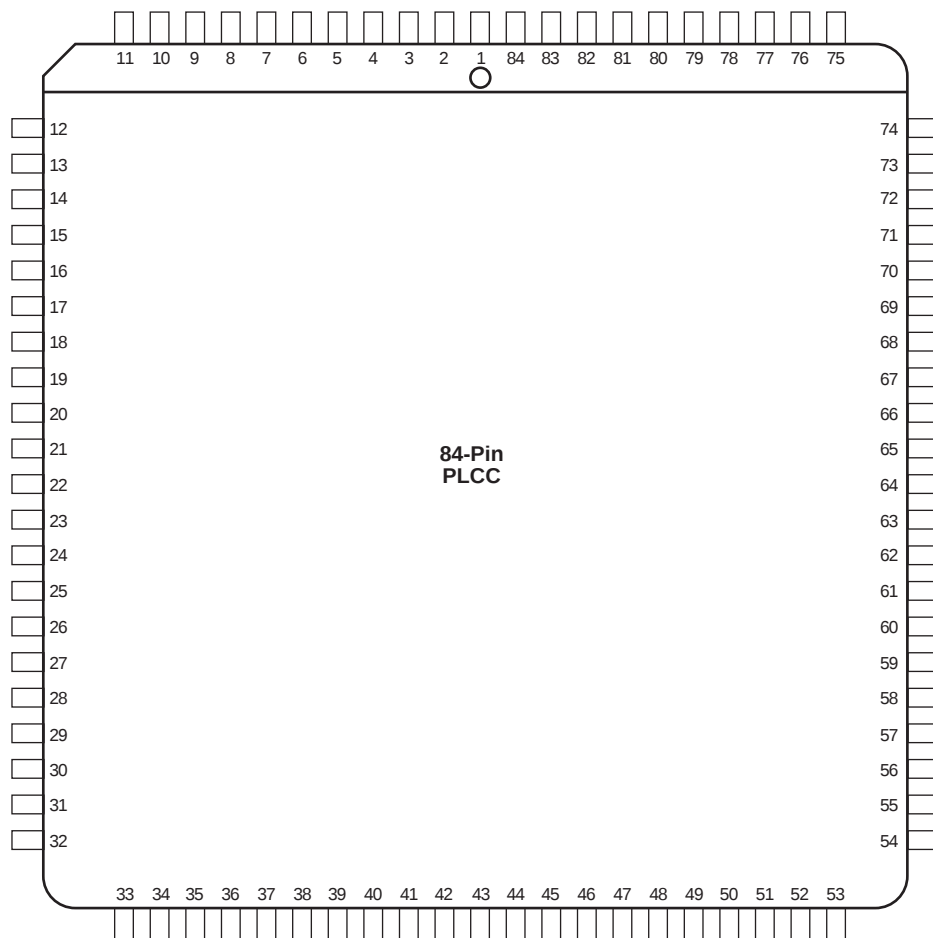
Dedicated (hardwired) I/O Clock Network		–3 Speed ¹		–2 Speed ¹		–1 Speed		Std. Speed		3.3 V Speed ¹		Units
Parameter/Description		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t _{ILOCKH}	Input Low to High (pad to I/O module input)		2.3		2.6		3.0		3.5		4.5	ns
t _{IOPWH}	Minimum Pulse Width High	2.4		3.3		3.8		4.8		6.5		ns
t _{IPOWL}	Minimum Pulse Width Low	2.4		3.3		3.8		4.8		6.5		ns
t _{IOSAPW}	Minimum Asynchronous Pulse Width	2.4		3.3		3.8		4.8		6.5		ns
t _{ILOCKSW}	Maximum Skew		0.6		0.6		0.7		0.8		0.6	ns
t _{IOP}	Minimum Period	5.0		6.8		8.0		10.0		13.4		ns
f _{IOMAX}	Maximum Frequency		200		150		125		100		75	MHz
Dedicated (hardwired) Array Clock												
t _{HCKH}	Input Low to High (pad to S-module input)		3.7		4.1		4.7		5.5		7.0	ns
t _{HCKL}	Input High to Low (pad to S-module input)		3.7		4.1		4.7		5.5		7.0	ns
t _{HPWH}	Minimum Pulse Width High	2.4		3.3		3.8		4.8		6.5		ns
t _{HPWL}	Minimum Pulse Width Low	2.4		3.3		3.8		4.8		6.5		ns
t _{HCKSW}	Delta High to Low, Low Slew		0.6		0.6		0.7		0.8		0.6	ns
t _{HP}	Minimum Period	5.0		6.8		8.0		10.0		13.4		ns
f _{HMAX}	Maximum Frequency		200		150		125		100		75	MHz
Routed Array Clock Networks												
t _{RCKH}	Input Low to High (FO = 64)		6.0		6.8		7.7		9.0		11.8	ns
t _{RCKL}	Input High to Low (FO = 64)		6.0		6.8		7.7		9.0		11.8	ns
t _{RPWH}	Min. Pulse Width High (FO = 64)	4.1		4.5		5.4		6.1		8.2		ns
t _{RPWL}	Min. Pulse Width Low (FO = 64)	4.1		4.5		5.4		6.1		8.2		ns
t _{RCKSW}	Maximum Skew (FO = 128)		1.2		1.4		1.6		1.8		1.8	ns
t _{RP}	Minimum Period (FO = 64)	8.3		9.3		11.1		12.5		16.7		ns
f _{RMAX}	Maximum Frequency (FO = 64)		120		105		90		80		60	MHz
Clock-to-Clock Skews												
t _{ILOCKSW}	I/O Clock to H-Clock Skew	0.0	2.6	0.0	2.7	0.0	2.9	0.0	3.0	0.0	3.0	ns
t _{IORCKSW}	I/O Clock to R-Clock Skew (FO = 64) (FO = 350)	0.0 0.0	1.7 5.0	0.0 0.0	1.7 5.0	0.0 0.0	1.7 5.0	0.0 0.0	1.7 5.0	0.0 0.0	5.0 5.0	ns
t _{HRCKSW}	H-Clock to R-Clock Skew (FO = 64) (FO = 350)	0.0 0.0	1.3 3.0	0.0 0.0	1.0 3.0	0.0 0.0	1.0 3.0	0.0 0.0	1.0 3.0	0.0 0.0	1.0 3.0	ns

Notes: *

1. The –2 and –3 speed grades have been discontinued. Refer to PDN 0104, PDN 0203, PDN 0604, and PDN 1004 at <http://www.microsemi.com/soc/support/notifications/default.aspx#pdn>.
2. Delays based on 35 pF loading.

3 – Package Pin Assignments

PL84

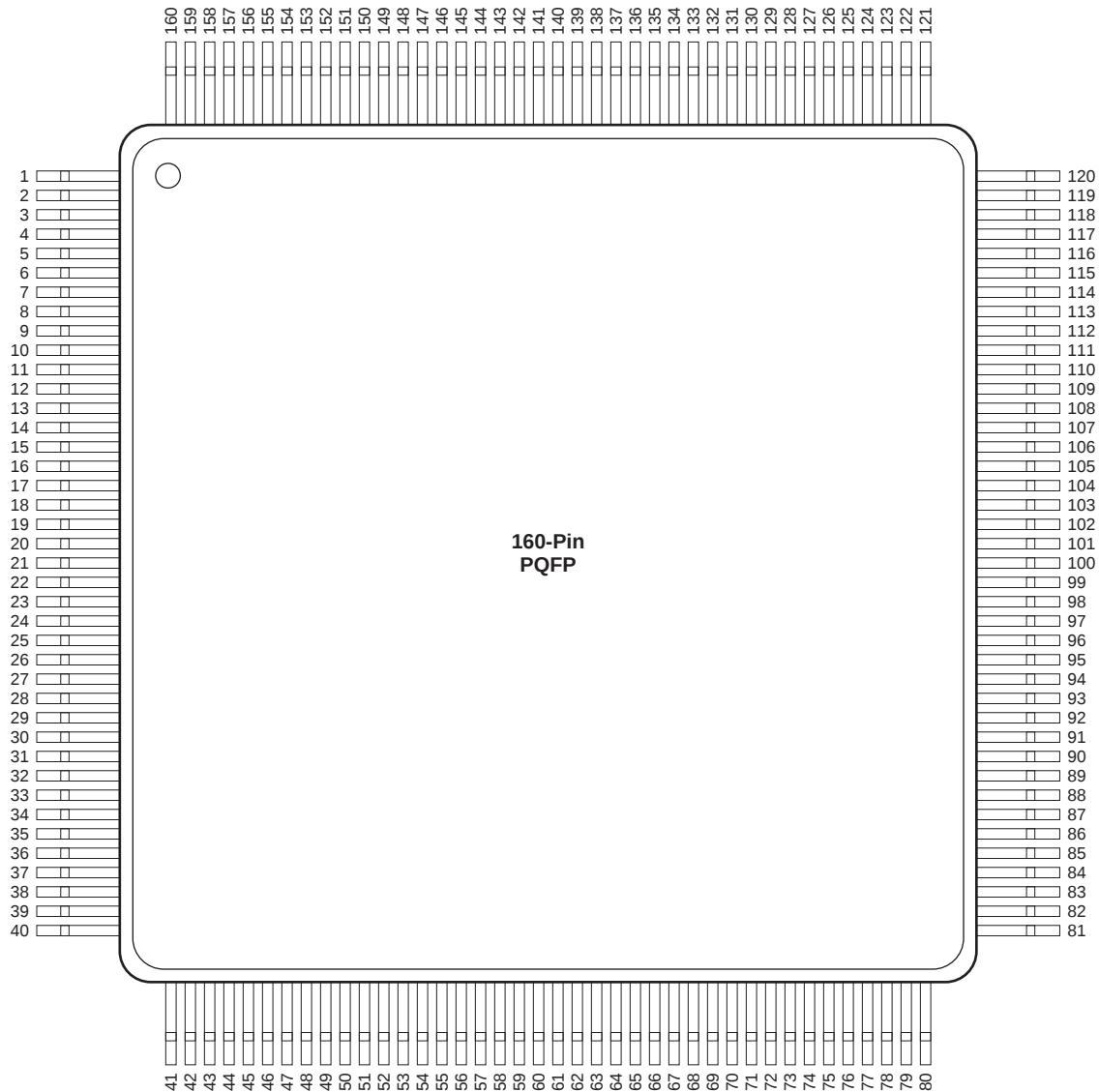


Note: This is the top view of the package.

Note

For Package Manufacturing and Environmental information, visit the Resource Center at <http://www.microsemi.com/soc/products/solutions/package/docs.aspx>.

PQ160



Note: This is the top view of the package

Note

For Package Manufacturing and Environmental information, visit the Resource Center at <http://www.microsemi.com/soc/products/solutions/package/docs.aspx>

PQ160			
Pin Number	A1425, A14V25 Function	A1440, A14V40 Function	A1460, A14V60 Function
1	GND	GND	GND
2	SDI, I/O	SDI, I/O	SDI, I/O
5	NC	I/O	I/O
9	MODE	MODE	MODE
10	VCC	VCC	VCC
14	NC	I/O	I/O
15	GND	GND	GND
18	VCC	VCC	VCC
19	GND	GND	GND
20	NC	I/O	I/O
24	NC	I/O	I/O
27	NC	I/O	I/O
28	VCC	VCC	VCC
29	VCC	VCC	VCC
40	GND	GND	GND
41	NC	I/O	I/O
43	NC	I/O	I/O
45	NC	I/O	I/O
46	VCC	VCC	VCC
47	NC	I/O	I/O
49	NC	I/O	I/O
51	NC	I/O	I/O
53	NC	I/O	I/O
58	PRB, I/O	PRB, I/O	PRB, I/O
59	GND	GND	GND
60	VCC	VCC	VCC
62	HCLK, I/O	HCLK, I/O	HCLK, I/O
63	GND	GND	GND
74	NC	I/O	I/O
75	VCC	VCC	VCC
76	NC	I/O	I/O
77	NC	I/O	I/O
78	NC	I/O	I/O
79	SDO	SDO	SDO
80	IOPCL, I/O	IOPCL, I/O	IOPCL, I/O
81	GND	GND	GND
90	VCC	VCC	VCC
91	VCC	VCC	VCC

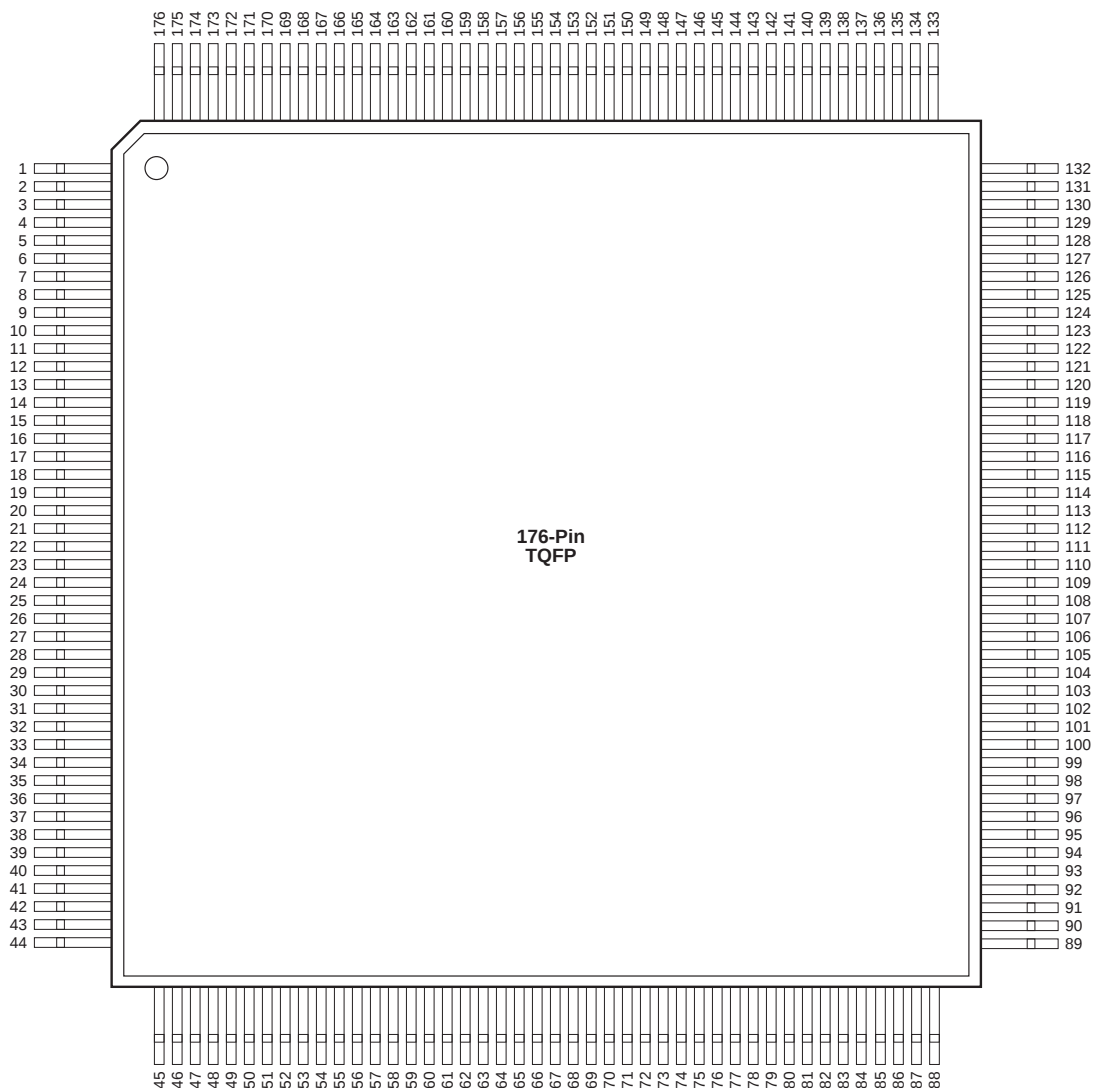
PQ208, RQ208		
Pin Number	A1460, A14V60 Function	A14100, A14V100 Function
1	GND	GND
2	SDI, I/O	SDI, I/O
11	MODE	MODE
12	VCC	VCC
25	VCC	VCC
26	GND	GND
27	VCC	VCC
28	GND	GND
40	VCC	VCC
41	VCC	VCC
52	GND	GND
53	NC	I/O
60	VCC	VCC
65	NC	I/O
76	PRB, I/O	PRB, I/O
77	GND	GND
78	VCC	VCC
79	GND	GND
80	VCC	VCC
82	HCLK, I/O	HCLK, I/O
98	VCC	VCC
102	NC	I/O
103	SDO	SDO
104	IOPCL, I/O	IOPCL, I/O
105	GND	GND
114	VCC	VCC

PQ208, RQ208		
Pin Number	A1460, A14V60 Function	A14100, A14V100 Function
115	VCC	VCC
116	NC	I/O
129	GND	GND
130	VCC	VCC
131	GND	GND
132	VCC	VCC
145	VCC	VCC
146	GND	GND
147	NC	I/O
148	VCC	VCC
156	IOCLK, I/O	IOCLK, I/O
157	GND	GND
158	NC	I/O
164	VCC	VCC
180	CLKA, I/O	CLKA, I/O
181	CLKB, I/O	CLKB, I/O
182	VCC	VCC
183	GND	GND
184	VCC	VCC
185	GND	GND
186	PRA, I/O	PRA, I/O
195	NC	I/O
201	VCC	VCC
205	NC	I/O
208	DCLK, I/O	DCLK, I/O

Notes:

1. All unlisted pin numbers are user I/Os.
2. NC denotes no connection.
3. MODE should be terminated to GND through a 10K resistor to enable Actionprobe usage; otherwise it can be terminated directly to GND.

TQ176

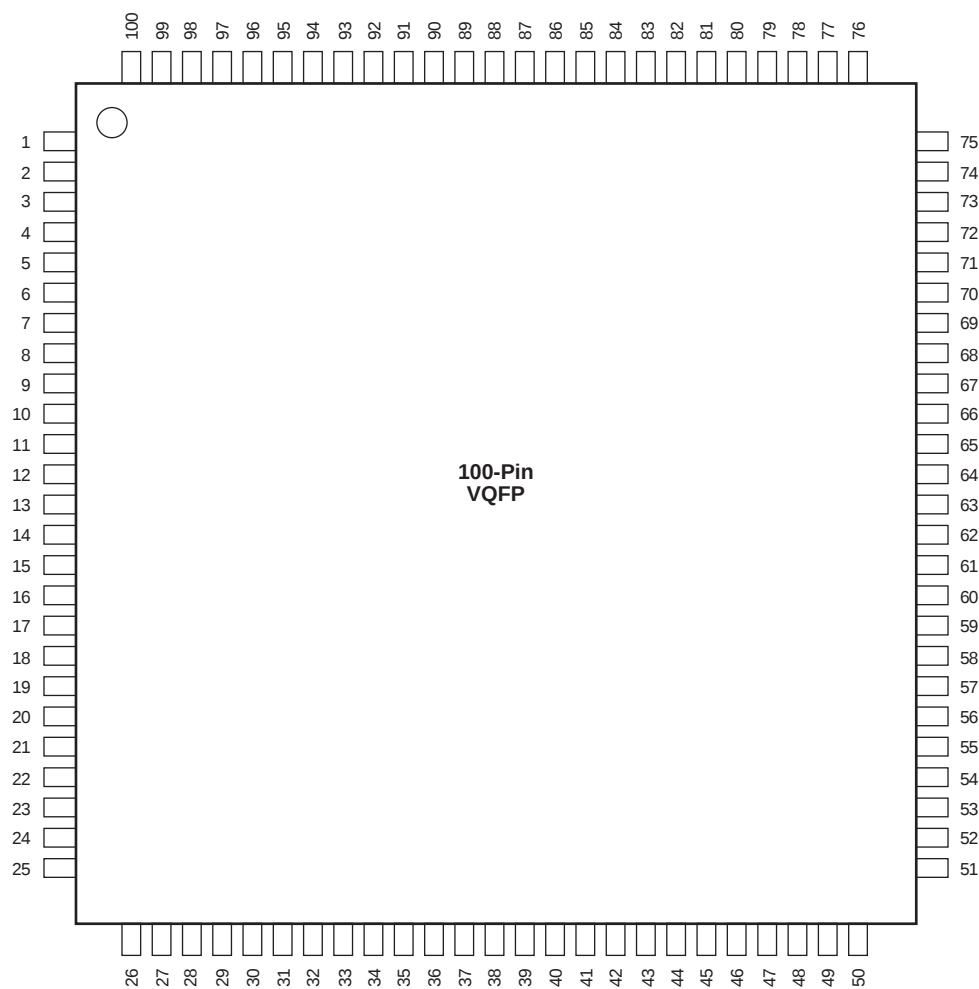


Note: This is the top view.

Note

For Package Manufacturing and Environmental information, visit the Resource Center at <http://www.microsemi.com/soc/products/solutions/package/docs.aspx>

VQ100



Note: This is the top view.

Note

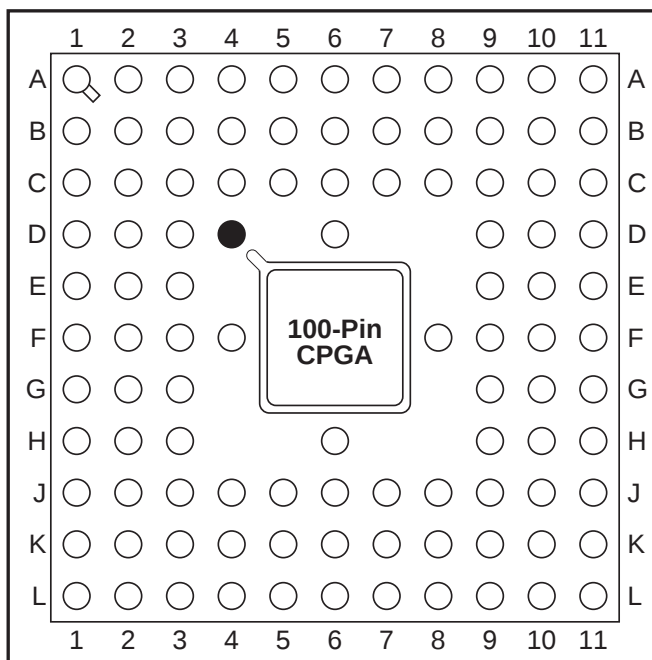
For Package Manufacturing and Environmental information, visit the Resource Center at <http://www.microsemi.com/soc/products/solutions/package/docs.aspx>

BG225	
A1460 Function	Location
CLKA or I/O	C8
CLKB or I/O	B8
DCLK or I/O	B2
GND	A1, A15, D15, F8, G7, G8, G9, H6, H7, H8, H9, H10, J7, J8, J9, K8, P2, R15
HCLK or I/O	P9
IOCLK or I/O	B14
IOPCL or I/O	P14
MODE	D1
NC	A11, B5, B7, D8, D12, F6, F11, H1, H12, H14, K11, L1, L13, N8, P5, R1, R8, R11, R14
PRA or I/O	A7
PRB or I/O	L7
SDI or I/O	D4
SDO	N13
VCC	A8, B12, D5, D14, E3, E8, E13, H2, H3, H11, H15, K4, L2, L12, M8, M15, P4, P8, R13

Notes:

1. All unlisted pin numbers are user I/Os.
2. NC denotes no connection.
3. MODE should be terminated to GND through a 10K resistor to enable Actionprobe usage; otherwise it can be terminated directly to GND.
4. The BG225 package has been discontinued.

PG100



● Orientation Pin

Note: This is the top view.

Note

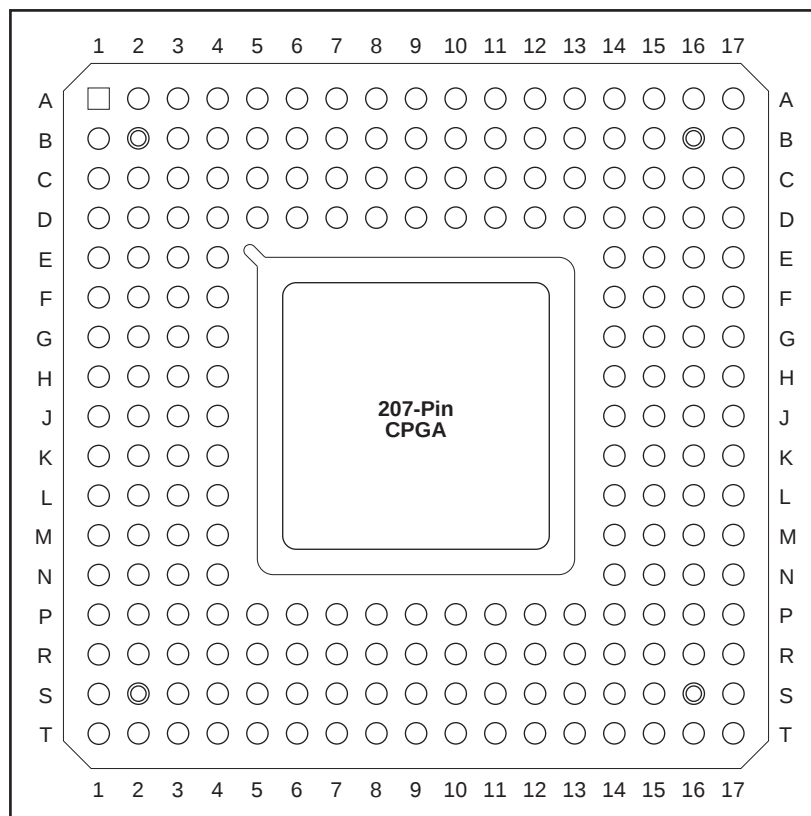
For Package Manufacturing and Environmental information, visit the Resource Center at <http://www.microsemi.com/soc/products/solutions/package/docs.aspx>

PG175	
A1440 Function	Location
CLKA or I/O	C9
CLKB or I/O	A9
DCLK or I/O	D5
GND	D4, D8, D11, D12, E4, E14, H4, H12, L4, L12, M4, M8, M12
HCLK or I/O	R8
IOCLK or I/O	E12
IOPCL or I/O	P13
MODE	F3
NC	A1, A2, A15, B2, B3, P2, P14, R1, R2, R14, R15
PRA or I/O	B8
PRB or I/O	R7
SDI or I/O	D3
SDO	N12
VCC	C3, C8, C13, E15, H3, H13, L1, L14, N3, N8, N13

Notes:

1. All unlisted pin numbers are user I/Os.
2. NC denotes no connection.
3. MODE should be terminated to GND through a 10K resistor to enable Actionprobe usage; otherwise it can be terminated directly to GND.
4. The PG175 package has been discontinued.

PG207



Note: This is the top view.

Note

For Package Manufacturing and Environmental information, visit the Resource Center at <http://www.microsemi.com/soc/products/solutions/package/docs.aspx>



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