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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Obsolete
Number of LABs/CLBs	564
Number of Logic Elements/Cells	-
Total RAM Bits	-
Number of I/O	83
Number of Gates	4000
Voltage - Supply	4.5V ~ 5.5V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 70°C (TA)
Package / Case	100-TQFP
Supplier Device Package	100-VQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/microsemi/a1440a-vqg100c

Device/Package	Speed Grade ¹				Application ¹			
	Std.	–1	–2	–3	C	I	M	B
A14V40A Device								
84-Pin Plastic Leaded Chip Carrier (PLCC)	✓	–	–	–	✓	–	–	–
100-Pin Very Thin Quad Flatpack (VQFP)	✓	–	–	–	✓	–	–	–
160-Pin Plastic Quad Flatpack (PQFP)	✓	–	–	–	✓	–	–	–
176-Pin Thin Quad Flatpack (TQFP)	✓	–	–	–	✓	–	–	–
A1460A Device								
160-Pin Plastic Quad Flatpack (PQFP)	✓	✓	D	D	✓	✓	–	–
176-Pin Thin Quad Flatpack (TQFP)	✓	✓	D	D	✓	✓	–	–
196-Pin Ceramic Quad Flatpack (CQFP)	✓	✓	–	–	✓	–	✓	✓
207-Pin Ceramic Pin Grid Array (CPGA)	✓	✓	D	D	✓	–	✓	✓
208-Pin Plastic Quad Flatpack (PQFP)	✓	✓	D	D	✓	✓	–	–
225-Pin Plastic Ball Grid Array (BGA)	D	D	D	D	D	–	–	–
A14V60A Device								
160-Pin Plastic Quad Flatpack (PQFP)	✓	–	–	–	✓	–	–	–
176-Pin Thin Quad Flatpack (TQFP)	✓	–	–	–	✓	–	–	–
208-Pin Plastic Quad Flatpack (PQFP)	✓	–	–	–	✓	–	–	–
A14100A Device								
208-Pin Power Quad Flatpack (RQFP)	✓	✓	D	D	✓	✓	–	–
257-Pin Ceramic Pin Grid Array (CPGA)	✓	✓	D	D	✓	–	✓	✓
313-Pin Plastic Ball Grid Array (BGA)	✓	✓	D	D	✓	–	–	–
256-Pin Ceramic Quad Flatpack (CQFP)	✓	✓	–	–	✓	–	✓	✓
A14V100A Device								
208-Pin Power Quad Flatpack (RQFP)	✓	–	–	–	✓	–	–	–
313-Pin Plastic Ball Grid Array (BGA)	✓	–	–	–	✓	–	–	–

Notes:

- Applications:**
C = Commercial
I = Industrial
M = Military
- Commercial only

Availability:
✓ = Available
P = Planned
– = Not planned
D = Discontinued

Speed Grade:
–1 = Approx. 15% faster than Std.
–2 = Approx. 25% faster than Std.
–3 = Approx. 35% faster than Std.
(–2 and –3 speed grades have been discontinued.)

Logic Modules

ACT 3 logic modules are enhanced versions of the 1200XL family logic modules. As in the 1200XL family, there are two types of modules: C-modules and S-modules (Figure 2-2 and Figure 2-3). The C-module is functionally equivalent to the 1200XL C-module and implements high fanin combinatorial macros, such as 5-input AND, 5-input OR, and so on. It is available for use as the CM8 hard macro. The S-module is designed to implement high-speed sequential functions within a single module.

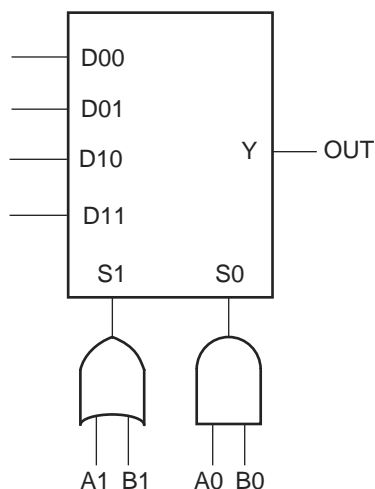


Figure 2-2 • C-Module Diagram

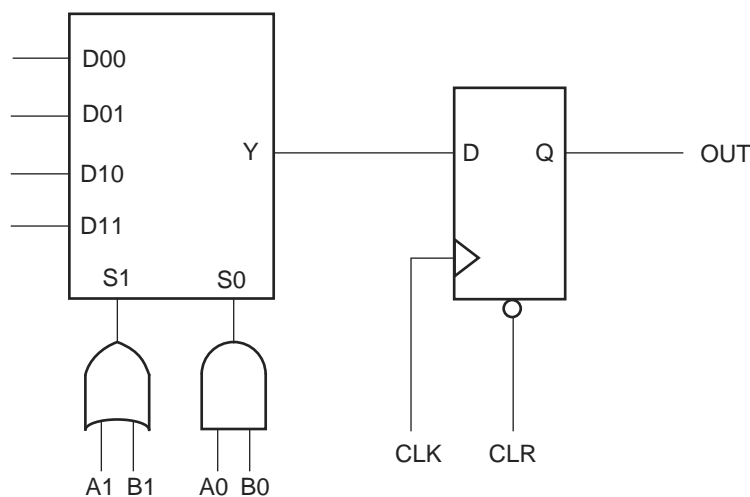


Figure 2-3 • S-Module Diagram

S-modules consist of a full C-module driving a flip-flop, which allows an additional level of logic to be implemented without additional propagation delay. It is available for use as the DFM8A/B and DLM8A/B hard macros. C-modules and S-modules are arranged in pairs called module-pairs. Module-pairs are arranged in alternating patterns and make up the bulk of the array. This arrangement allows the placement software to support two-module macros of four types (CC, CS, SC, and SS). The C-module implements the following function:

$$Y = !S1 * !S0 * D00 + !S1 * S0 * D01 + S1 * !S0 * D10 + S1 * S0 * D11$$

EQ 1

where: $S0 = A0 * B0$ and $S1 = A1 + B1$

Horizontal Routing

Horizontal channels are located between the rows of modules and are composed of several routing tracks. The horizontal routing tracks within the channel are divided into one or more segments. The minimum horizontal segment length is the width of a module-pair, and the maximum horizontal segment length is the full length of the channel. Any segment that spans more than one-third the row length is considered a long horizontal segment. A typical channel is shown in Figure 2-7. Undedicated horizontal routing tracks are used to route signal nets. Dedicated routing tracks are used for the global clock networks and for power and ground tie-off tracks.

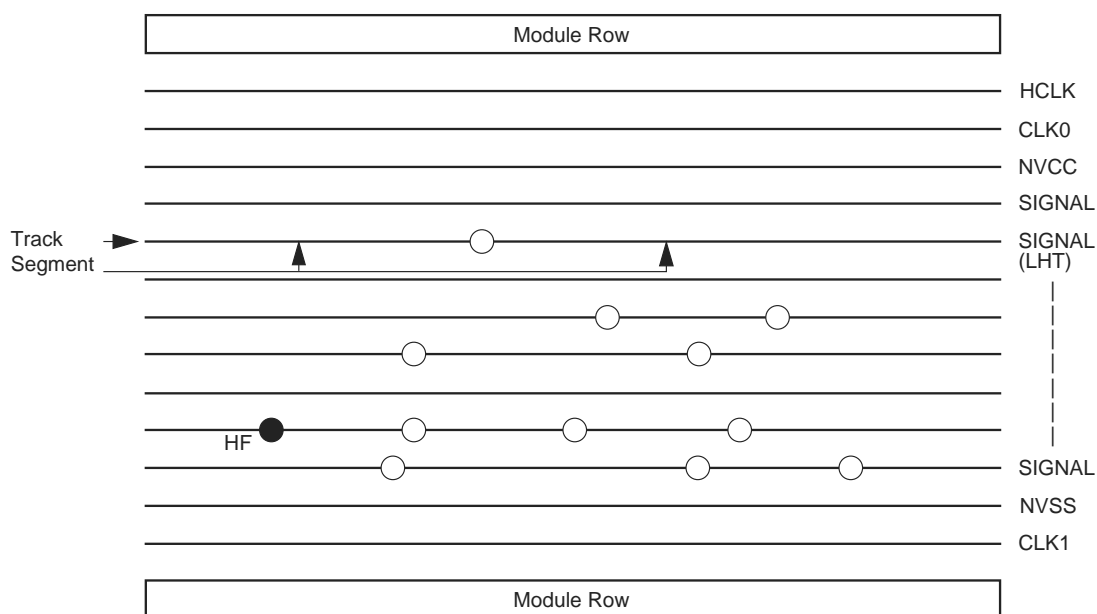


Figure 2-7 • Horizontal Routing Tracks and Segments

Vertical Routing

Other tracks run vertically through the modules. Vertical tracks are of three types: input, output, and long. Vertical tracks are also divided into one or more segments. Each segment in an input track is dedicated to the input of a particular module. Each segment in an output track is dedicated to the output of a particular module. Long segments are uncommitted and can be assigned during routing. Each output segment spans four channels (two above and two below), except near the top and bottom of the array where edge effects occur. LVTs contain either one or two segments. An example of vertical routing tracks and segments is shown in Figure 2-8.

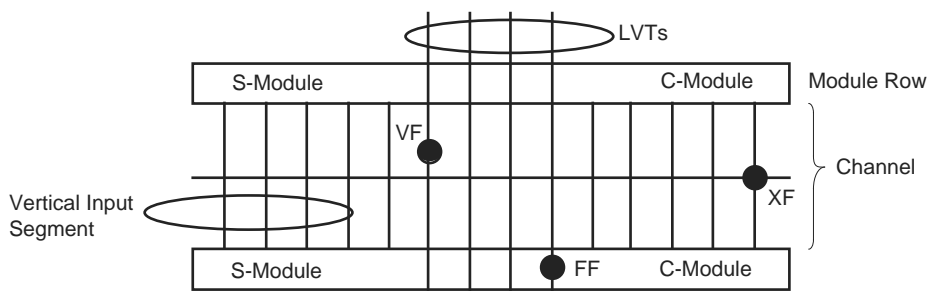


Figure 2-8 • Vertical Routing Tracks and Segments

Determining Average Switching Frequency

To determine the switching frequency for a design, you must have a detailed understanding of the data input values to the circuit. The following guidelines are meant to represent worst-case scenarios so that they can be generally used to predict the upper limits of power dissipation. These guidelines are as follows:

Table 2-13 • Guidelines for Predicting Power Dissipation

Data	Value
Logic Modules (m)	80% of modules
Inputs switching (n)	# inputs/4
Outputs switching (p)	# output/4
First routed array clock loads (q1)	40% of sequential modules
Second routed array clock loads (q2)	40% of sequential modules
Load capacitance (CL)	35 pF
Average logic module switching rate (fm)	F/10
Average input switching rate (fn)	F/5
Average output switching rate (fp)	F/10
Average first routed array clock rate (fq1)	F/2
Average second routed array clock rate (fq2)	F/2
Average dedicated array clock rate (fs1)	F
Average dedicated I/O clock rate (fs2)	F

A1415A, A14V15A Timing Characteristics

Table 2-18 • A1415A, A14V15A Worst-Case Commercial Conditions, VCC = 4.75 V, T_J = 70°C¹

Logic Module Propagation Delays ²		–3 Speed ³		–2 Speed ³		–1 Speed		Std. Speed		3.3 V Speed ¹		Units
Parameter/Description		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t _{PD}	Internal Array Module		2.0		2.3		2.6		3.0		3.9	ns
t _{CO}	Sequential Clock to Q		2.0		2.3		2.6		3.0		3.9	ns
t _{CLR}	Asynchronous Clear to Q		2.0		2.3		2.6		3.0		3.9	ns
Predicted Routing Delays⁴												
t _{RD1}	FO = 1 Routing Delay		0.9		1.0		1.1		1.3		1.7	ns
t _{RD2}	FO = 2 Routing Delay		1.2		1.4		1.6		1.8		2.4	ns
t _{RD3}	FO = 3 Routing Delay		1.4		1.6		1.8		2.1		2.8	ns
t _{RD4}	FO = 4 Routing Delay		1.7		1.9		2.2		2.5		3.3	ns
t _{RD8}	FO = 8 Routing Delay		2.8		3.2		3.6		4.2		5.5	ns
Logic Module Sequential Timing												
t _{SUD}	Flip-Flop Data Input Setup	0.5		0.6		0.7		0.8		0.8		ns
t _{HD}	Flip-Flop Data Input Hold	0.0		0.0		0.0		0.0		0.0		ns
t _{SUD}	Latch Data Input Setup	0.5		0.6		0.7		0.8		0.8		ns
t _{HD}	Latch Data Input Hold	0.0		0.0		0.0		0.0		0.0		ns
t _{WASYN}	Asynchronous Pulse Width	1.9		2.4		3.2		3.8		4.8		ns
t _{WCLKA}	Flip-Flop Clock Pulse Width	1.9		2.4		3.2		3.8		4.8		ns
t _A	Flip-Flop Clock Input Period	4.0		5.0		6.8		8.0		10.0		ns
f _{MAX}	Flip-Flop Clock Frequency		250		200		150		125		100	MHz

Notes:

- VCC = 3.0 V for 3.3 V specifications.
- For dual-module macros, use t_{PD} + t_{RD1} + t_{PDn} + t_{CO} + t_{RD1} + t_{PDn} or t_{PD1} + t_{RD1} + t_{SUD}, whichever is appropriate.
- The –2 and –3 speed grades have been discontinued. Please refer to the Product Discontinuation Notices (PDNs) listed below:
PDN March 2001
PDN 0104
PDN 0203
PDN 0604
PDN 1004
- Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual worst-case performance. Post-route timing is based on actual routing delay measurements performed on the device prior to shipment.

A1425A, A14V25A Timing Characteristics (continued)

Table 2-23 • A1425A, A14V25A Worst-Case Commercial Conditions, VCC = 4.75 V, T_J = 70°C

I/O Module Input Propagation Delays		–3 Speed ¹		–2 Speed ¹		–1 Speed		Std. Speed		3.3 V Speed ¹		Units
Parameter/Description		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t _{INY}	Input Data Pad to Y		2.8		3.2		3.6		4.2		5.5	ns
t _{ICKY}	Input Reg IOCLK Pad to Y		4.7		5.3		6.0		7.0		9.2	ns
t _{OCKY}	Output Reg IOCLK Pad to Y		4.7		5.3		6.0		7.0		9.2	ns
t _{ICLRY}	Input Asynchronous Clear to Y		4.7		5.3		6.0		7.0		9.2	ns
t _{OCLRY}	Output Asynchronous Clear to Y		4.7		5.3		6.0		7.0		9.2	ns
Predicted Input Routing Delays²												
t _{RD1}	FO = 1 Routing Delay		0.9		1.0		1.1		1.3		1.7	ns
t _{RD2}	FO = 2 Routing Delay		1.2		1.4		1.6		1.8		2.4	ns
t _{RD3}	FO = 3 Routing Delay		1.4		1.6		1.8		2.1		2.8	ns
t _{RD4}	FO = 4 Routing Delay		1.7		1.9		2.2		2.5		3.3	ns
t _{RD8}	FO = 8 Routing Delay		2.8		3.2		3.6		4.2		5.5	ns
I/O Module Sequential Timing (wrt IOCLK pad)												
t _{INH}	Input F-F Data Hold	0.0		0.0		0.0		0.0		0.0		ns
t _{INSU}	Input F-F Data Setup	1.8		2.0		2.3		2.7		3.0		ns
t _{IDEH}	Input Data Enable Hold	0.0		0.0		0.0		0.0		0.0		ns
t _{IDESU}	Input Data Enable Setup	5.8		6.5		7.5		8.6		8.6		ns
t _{OUTH}	Output F-F Data hold	0.7		0.8		0.9		1.0		1.0		ns
t _{OUTSU}	Output F-F Data Setup	0.7		0.8		0.9		1.0		1.0		ns
t _{ODEH}	Output Data Enable Hold	0.3		0.4		0.4		0.5		0.5		ns
f _{ODESU}	Output Data Enable Setup	1.3		1.5		1.7		2.0		2.0		ns

Notes: *

1. The –2 and –3 speed grades have been discontinued. Refer to PDN 0104, PDN 0203, PDN 0604, and PDN 1004 at <http://www.microsemi.com/soc/support/notifications/default.aspx#pdn>.
2. Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual worst-case performance. Post-route timing is based on actual routing delay measurements performed on the device prior to shipment.

A1440A, A14V40A Timing Characteristics

Table 2-26 • A1440A, A14V40A Worst-Case Commercial Conditions, VCC = 4.75 V, T_J = 70°C¹

Logic Module Propagation Delays ²		–3 Speed ³		–2 Speed ³		–1 Speed		Std. Speed		3.3 V Speed ¹		Units
Parameter/Description		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t _{PD}	Internal Array Module		2.0		2.3		2.6		3.0		3.9	ns
t _{CO}	Sequential Clock to Q		2.0		2.3		2.6		3.0		3.9	ns
t _{CLR}	Asynchronous Clear to Q		2.0		2.3		2.6		3.0		3.9	ns
Predicted Routing Delays⁴												
t _{RD1}	FO = 1 Routing Delay		0.9		1.0		1.1		1.3		1.7	ns
t _{RD2}	FO = 2 Routing Delay		1.2		1.4		1.6		1.8		2.4	ns
t _{RD3}	FO = 3 Routing Delay		1.4		1.6		1.8		2.1		2.8	ns
t _{RD4}	FO = 4 Routing Delay		1.7		1.9		2.2		2.5		3.3	ns
t _{RD8}	FO = 8 Routing Delay		2.8		3.2		3.6		4.2		5.5	ns
Logic Module Sequential Timing												
t _{SUD}	Flip-Flop Data Input Setup	0.5		0.6		0.7		0.8		0.8		ns
t _{HD}	Flip-Flop Data Input Hold	0.0		0.0		0.0		0.0		0.0		ns
t _{SUD}	Latch Data Input Setup	0.5		0.6		0.7		0.8		0.8		ns
t _{HD}	Latch Data Input Hold	0.0		0.0		0.0		0.0		0.0		ns
t _{WASYN}	Asynchronous Pulse Width	1.9		2.4		3.2		3.8		4.8		ns
t _{WCLKA}	Flip-Flop Clock Pulse Width	1.9		2.4		3.2		3.8		4.8		ns
t _A	Flip-Flop Clock Input Period	4.0		5.0		6.8		8.0		10.0		ns
f _{MAX}	Flip-Flop Clock Frequency		250		200		150		125		100	MHz

Notes:

1. VCC = 3.0 V for 3.3 V specifications.
2. For dual-module macros, use t_{PD} + t_{RD1} + t_{PDn} + t_{CO} + t_{RD1} + t_{PDn} or t_{PD1} + t_{RD1} + t_{SUD}, whichever is appropriate.
3. The –2 and –3 speed grades have been discontinued. Refer to PDN 0104, PDN 0203, PDN 0604, and PDN 1004 at <http://www.microsemi.com/soc/support/notifications/default.aspx#pdn>.
4. Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual worst-case performance. Post-route timing is based on actual routing delay measurements performed on the device prior to shipment.

A1440A, A14V40A Timing Characteristics (continued)

Table 2-28 • A1440A, A14V40A Worst-Case Commercial Conditions, VCC = 4.75 V, T_J = 70°C

I/O Module – TTL Output Timing ¹		–3 Speed ²		–2 Speed ²		–1 Speed		Std. Speed		3.3 V Speed ¹		Units
Parameter/Description		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t _{DHS}	Data to Pad, High Slew		5.0		5.6		6.4		7.5		9.8	ns
t _{DLS}	Data to Pad, Low Slew		8.0		9.0		10.2		12.0		15.6	ns
t _{ENZHS}	Enable to Pad, Z to H/L, High Slew		4.0		4.5		5.1		6.0		7.8	ns
t _{ENZLS}	Enable to Pad, Z to H/L, Low Slew		7.4		8.3		9.4		11.0		14.3	ns
t _{ENHSZ}	Enable to Pad, H/L to Z, High Slew		7.4		8.3		9.4		11.0		14.3	ns
t _{ENLSZ}	Enable to Pad, H/L to Z, Low Slew		7.4		8.3		9.4		11.0		14.3	ns
t _{CKHS}	IOCLK Pad to Pad H/L, High Slew		8.5		8.5		9.5		11.0		14.3	ns
t _{CKLS}	IOCLK Pad to Pad H/L, Low Slew		11.3		11.3		13.5		15.0		19.5	ns
d _{TLHHS}	Delta Low to High, High Slew		0.02		0.02		0.03		0.03		0.04	ns/pF
d _{TLHLS}	Delta Low to High, Low Slew		0.05		0.05		0.06		0.07		0.09	ns/pF
d _{THLHS}	Delta High to Low, High Slew		0.04		0.04		0.04		0.05		0.07	ns/pF
d _{THLLS}	Delta High to Low, Low Slew		0.05		0.05		0.06		0.07		0.09	ns/pF
I/O Module – CMOS Output Timing ¹												
t _{DHS}	Data to Pad, High Slew		6.2		7.0		7.9		9.3		12.1	ns
t _{DLS}	Data to Pad, Low Slew		11.7		13.1		14.9		17.5		22.8	ns
t _{ENZHS}	Enable to Pad, Z to H/L, High Slew		5.2		5.9		6.6		7.8		10.1	ns
t _{ENZLS}	Enable to Pad, Z to H/L, Low Slew		8.9		10.0		11.3		13.3		17.3	ns
t _{ENHSZ}	Enable to Pad, H/L to Z, High Slew		7.4		8.3		9.4		11.0		14.3	ns
t _{ENLSZ}	Enable to Pad, H/L to Z, Low Slew		7.4		8.3		9.4		11.0		14.3	ns
t _{CKHS}	IOCLK Pad to Pad H/L, High Slew		9.0		9.0		10.1		11.8		14.3	ns
t _{CKLS}	IOCLK Pad to Pad H/L, Low Slew		13.0		13.0		15.6		17.3		22.5	ns
d _{TLHHS}	Delta Low to High, High Slew		0.04		0.04		0.05		0.06		0.08	ns/pF
d _{TLHLS}	Delta Low to High, Low Slew		0.07		0.08		0.09		0.11		0.14	ns/pF
d _{THLHS}	Delta High to Low, High Slew		0.03		0.03		0.03		0.04		0.05	ns/pF
d _{THLLS}	Delta High to Low, Low Slew		0.04		0.04		0.04		0.05		0.07	ns/pF

Notes:

1. Delays based on 35 pF loading.
2. The –2 and –3 speed grades have been discontinued. Refer to PDN 0104, PDN 0203, PDN 0604, and PDN 1004 at <http://www.microsemi.com/soc/support/notifications/default.aspx#pdn>.

A1440A, A14V40A Timing Characteristics (continued)

Table 2-29 • A1440A, A14V40A Worst-Case Commercial Conditions, VCC = 4.75 V, T_J = 70°C

Dedicated (hardwired) I/O Clock Network		–3 Speed ¹		–2 Speed ¹		–1 Speed		Std. Speed		3.3 V Speed ¹		Units
Parameter/Description		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t _{ILOCKH}	Input Low to High (pad to I/O module input)		2.0		2.3		2.6		3.0		3.5	ns
t _{IOPWH}	Minimum Pulse Width High	1.9		2.4		3.3		3.8		4.8		ns
t _{IPOWL}	Minimum Pulse Width Low	1.9		2.4		3.3		3.8		4.8		ns
t _{IOSAPW}	Minimum Asynchronous Pulse Width	1.9		2.4		3.3		3.8		4.8		ns
t _{ILOCKSW}	Maximum Skew		0.4		0.4		0.4		0.4		0.4	ns
t _{IOP}	Minimum Period	4.0		5.0		6.8		8.0		10.0		ns
f _{IOMAX}	Maximum Frequency		250		200		150		125		100	MHz
Dedicated (hardwired) Array Clock												
t _{HCKH}	Input Low to High (pad to S-module input)		3.0		3.4		3.9		4.5		5.5	ns
t _{HCKL}	Input High to Low (pad to S-module input)		3.0		3.4		3.9		4.5		5.5	ns
t _{HPWH}	Minimum Pulse Width High	1.9		2.4		3.3		3.8		4.8		ns
t _{HPWL}	Minimum Pulse Width Low	1.9		2.4		3.3		3.8		4.8		ns
t _{HCKSW}	Delta High to Low, Low Slew		0.3		0.3		0.3		0.3		0.3	ns
t _{HP}	Minimum Period	4.0		5.0		6.8		8.0		10.0		ns
f _{HMAX}	Maximum Frequency		250		200		150		125		100	MHz
Routed Array Clock Networks												
t _{RCKH}	Input Low to High (FO = 64)		3.7		4.1		4.7		5.5		9.0	ns
t _{RCKL}	Input High to Low (FO = 64)		4.0		4.5		5.1		6.0		9.0	ns
t _{RPWH}	Min. Pulse Width High (FO = 64)	3.3		3.8		4.2		4.9		6.5		ns
t _{RPWL}	Min. Pulse Width Low (FO = 64)	3.3		3.8		4.2		4.9		6.5		ns
t _{RCKSW}	Maximum Skew (FO = 128)		0.7		0.8		0.9		1.0		1.0	ns
t _{RP}	Minimum Period (FO = 64)	6.8		8.0		8.7		10.0		13.4		ns
f _{RMAX}	Maximum Frequency (FO = 64)		150		125		115		100		75	MHz
Clock-to-Clock Skews												
t _{IOHCKSW}	I/O Clock to H-Clock Skew	0.0	1.7	0.0	1.8	0.0	2.0	0.0	2.2	0.0	3.0	ns
t _{IORCKSW}	I/O Clock to R-Clock Skew (FO = 64) (FO = 144)	0.0	1.0	0.0	1.0	0.0	1.0	0.0	1.0	0.0	3.0	ns
		0.0	3.0	0.0	3.0	0.0	3.0	0.0	3.0	0.0	3.0	
t _{HRCKSW}	H-Clock to R-Clock Skew (FO = 64) (FO = 144)	0.0	1.0	0.0	1.0	0.0	1.0	0.0	1.0	0.0	1.0	ns
		0.0	3.0	0.0	3.0	0.0	3.0	0.0	3.0	0.0	3.0	

Notes:

1. The –2 and –3 speed grades have been discontinued. Refer to PDN 0104, PDN 0203, PDN 0604, and PDN 1004 at <http://www.microsemi.com/soc/support/notifications/default.aspx#pdn>.
2. Delays based on 35 pF loading.

A1460A, A14V60A Timing Characteristics (continued)

Table 2-32 • A1460A, A14V60A Worst-Case Commercial Conditions, VCC = 4.75 V, T_J = 70°C

I/O Module – TTL Output Timing ¹		–3 Speed ²		–2 Speed ²		–1 Speed		Std. Speed		3.3 V Speed ¹		Units
Parameter/Description		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t _{DHS}	Data to Pad, High Slew		5.0		5.6		6.4		7.5		9.8	ns
t _{DLS}	Data to Pad, Low Slew		8.0		9.0		10.2		12.0		15.6	ns
t _{ENZHS}	Enable to Pad, Z to H/L, High Slew		4.0		4.5		5.1		6.0		7.8	ns
t _{ENZLS}	Enable to Pad, Z to H/L, Low Slew		7.4		8.3		9.4		11.0		14.3	ns
t _{ENHSZ}	Enable to Pad, H/L to Z, High Slew		7.8		8.7		9.9		11.6		15.1	ns
t _{ENLSZ}	Enable to Pad, H/L to Z, Low Slew		7.4		8.3		9.4		11.0		14.3	ns
t _{CKHS}	IOCLK Pad to Pad H/L, High Slew		9.0		9.0		10.0		11.5		15.0	ns
t _{CKLS}	IOCLK Pad to Pad H/L, Low Slew		12.8		12.8		15.3		17.0		22.1	ns
d _{TLHHS}	Delta Low to High, High Slew		0.02		0.02		0.03		0.03		0.04	ns/pF
d _{TLHLS}	Delta Low to High, Low Slew		0.05		0.05		0.06		0.07		0.09	ns/pF
d _{THLHS}	Delta High to Low, High Slew		0.04		0.04		0.04		0.05		0.07	ns/pF
d _{THLLS}	Delta High to Low, Low Slew		0.05		0.05		0.06		0.07		0.09	ns/pF
I/O Module – CMOS Output Timing ¹												
t _{DHS}	Data to Pad, High Slew		6.2		7.0		7.9		9.3		12.1	ns
t _{DLS}	Data to Pad, Low Slew		11.7		13.1		14.9		17.5		22.8	ns
t _{ENZHS}	Enable to Pad, Z to H/L, High Slew		5.2		5.9		6.6		7.8		10.1	ns
t _{ENZLS}	Enable to Pad, Z to H/L, Low Slew		8.9		10.0		11.3		13.3		17.3	ns
t _{ENHSZ}	Enable to Pad, H/L to Z, High Slew		7.4		8.3		9.4		11.0		14.3	ns
t _{ENLSZ}	Enable to Pad, H/L to Z, Low Slew		7.4		8.3		9.4		11.0		14.3	ns
t _{CKHS}	IOCLK Pad to Pad H/L, High Slew		10.4		10.4		12.1		13.8		17.9	ns
t _{CKLS}	IOCLK Pad to Pad H/L, Low Slew		14.5		14.5		17.4		19.3		25.1	ns
d _{TLHHS}	Delta Low to High, High Slew		0.04		0.04		0.05		0.06		0.08	ns/pF
d _{TLHLS}	Delta Low to High, Low Slew		0.07		0.08		0.09		0.11		0.14	ns/pF
d _{THLHS}	Delta High to Low, High Slew		0.03		0.03		0.03		0.04		0.05	ns/pF
d _{THLLS}	Delta High to Low, Low Slew		0.04		0.04		0.04		0.05		0.07	ns/pF

Notes:

1. Delays based on 35 pF loading.
2. The –2 and –3 speed grades have been discontinued. Refer to PDN 0104, PDN 0203, PDN 0604, and PDN 1004 at <http://www.microsemi.com/soc/support/notifications/default.aspx#pdn>.

A14100A, A14V100A Timing Characteristics (continued)

Table 2-36 • A14100A, A14V100A Worst-Case Commercial Conditions, VCC = 4.75 V, T_J = 70°C

I/O Module – TTL Output Timing ¹		–3 Speed ²		–2 Speed ²		–1 Speed		Std. Speed		3.3 V Speed ¹		Units
Parameter/Description		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t _{DHS}	Data to Pad, High Slew		5.0		5.6		6.4		7.5		9.8	ns
t _{DLS}	Data to Pad, Low Slew		8.0		9.0		10.2		12.0		15.6	ns
t _{ENZHS}	Enable to Pad, Z to H/L, High Slew		4.0		4.5		5.1		6.0		7.8	ns
t _{ENZLS}	Enable to Pad, Z to H/L, Low Slew		7.4		8.3		9.4		11.0		14.3	ns
t _{ENHSZ}	Enable to Pad, H/L to Z, High Slew		8.0		9.0		10.2		12.0		15.6	ns
t _{ENLSZ}	Enable to Pad, H/L to Z, Low Slew		7.4		8.3		9.4		11.0		14.3	ns
t _{CKHS}	IOCLK Pad to Pad H/L, High Slew		9.5		9.5		10.5		12.0		15.6	ns
t _{CKLS}	IOCLK Pad to Pad H/L, Low Slew		12.8		12.8		15.3		17.0		22.1	ns
d _{TLHHS}	Delta Low to High, High Slew		0.02		0.02		0.03		0.03		0.04	ns/pF
d _{TLHLS}	Delta Low to High, Low Slew		0.05		0.05		0.06		0.07		0.09	ns/pF
d _{THLHS}	Delta High to Low, High Slew		0.04		0.04		0.04		0.05		0.07	ns/pF
d _{THLLS}	Delta High to Low, Low Slew		0.05		0.05		0.06		0.07		0.09	ns/pF
I/O Module – CMOS Output Timing ¹												
t _{DHS}	Data to Pad, High Slew		6.2		7.0		7.9		9.3		12.1	ns
t _{DLS}	Data to Pad, Low Slew		11.7		13.1		14.9		17.5		22.8	ns
t _{ENZHS}	Enable to Pad, Z to H/L, High Slew		5.2		5.9		6.6		7.8		10.1	ns
t _{ENZLS}	Enable to Pad, Z to H/L, Low Slew		8.9		10.0		11.3		13.3		17.3	ns
t _{ENHSZ}	Enable to Pad, H/L to Z, High Slew		8.0		9.0		10.0		12.0		15.6	ns
t _{ENLSZ}	Enable to Pad, H/L to Z, Low Slew		7.4		8.3		9.4		11.0		14.3	ns
t _{CKHS}	IOCLK Pad to Pad H/L, High Slew		10.4		10.4		12.4		13.8		17.9	ns
t _{CKLS}	IOCLK Pad to Pad H/L, Low Slew		14.5		14.5		17.4		19.3		25.1	ns
d _{TLHHS}	Delta Low to High, High Slew		0.04		0.04		0.05		0.06		0.08	ns/pF
d _{TLHLS}	Delta Low to High, Low Slew		0.07		0.08		0.09		0.11		0.14	ns/pF
d _{THLHS}	Delta High to Low, High Slew		0.03		0.03		0.03		0.04		0.05	ns/pF
d _{THLLS}	Delta High to Low, Low Slew		0.04		0.04		0.04		0.05		0.07	ns/pF

Notes: *

1. Delays based on 35 pF loading.
2. The –2 and –3 speed grades have been discontinued. Refer to PDN 0104, PDN 0203, PDN 0604, and PDN 1004 at <http://www.microsemi.com/soc/support/notifications/default.aspx#pdn>.

SDO Serial Data Output (Output)

Serial data output for diagnostic probe. SDO is active when the MODE pin is High. This pin functions as an I/O when the MODE pin is Low.

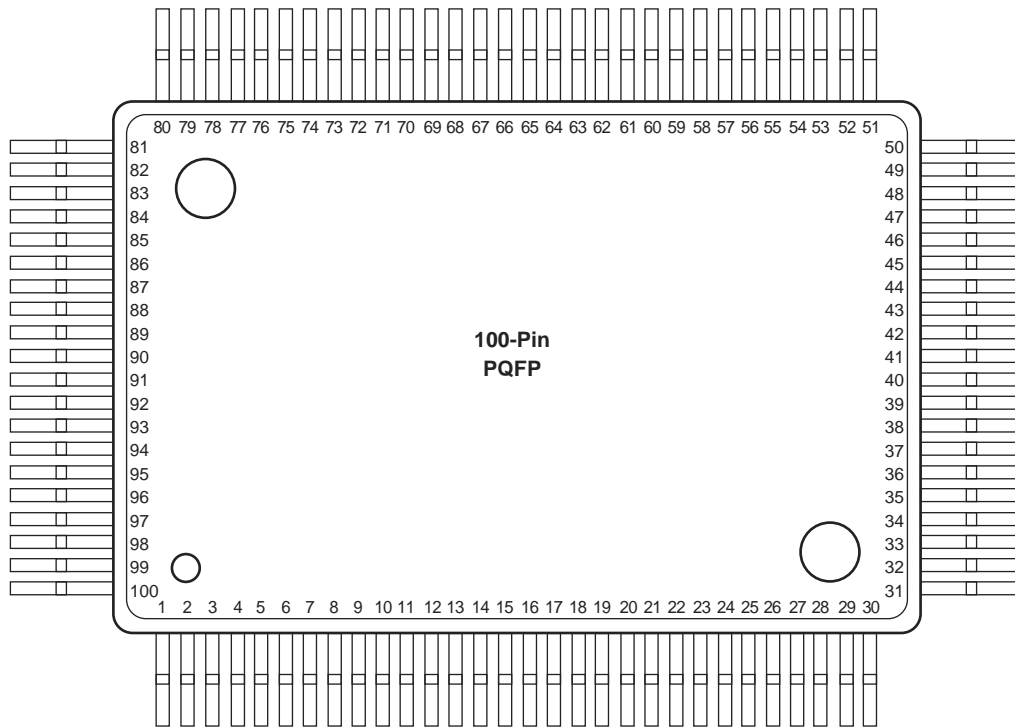
DCLK Diagnostic Clock (Input)

Clock input for diagnostic probe and device programming. DCLK is active when the MODE pin is HIGH. This pin functions as an I/O when the MODE pin is LOW.

VCC 5 V Supply Voltage

HIGH supply voltage.

PQ100



Note: This is the top view of the package.

Note

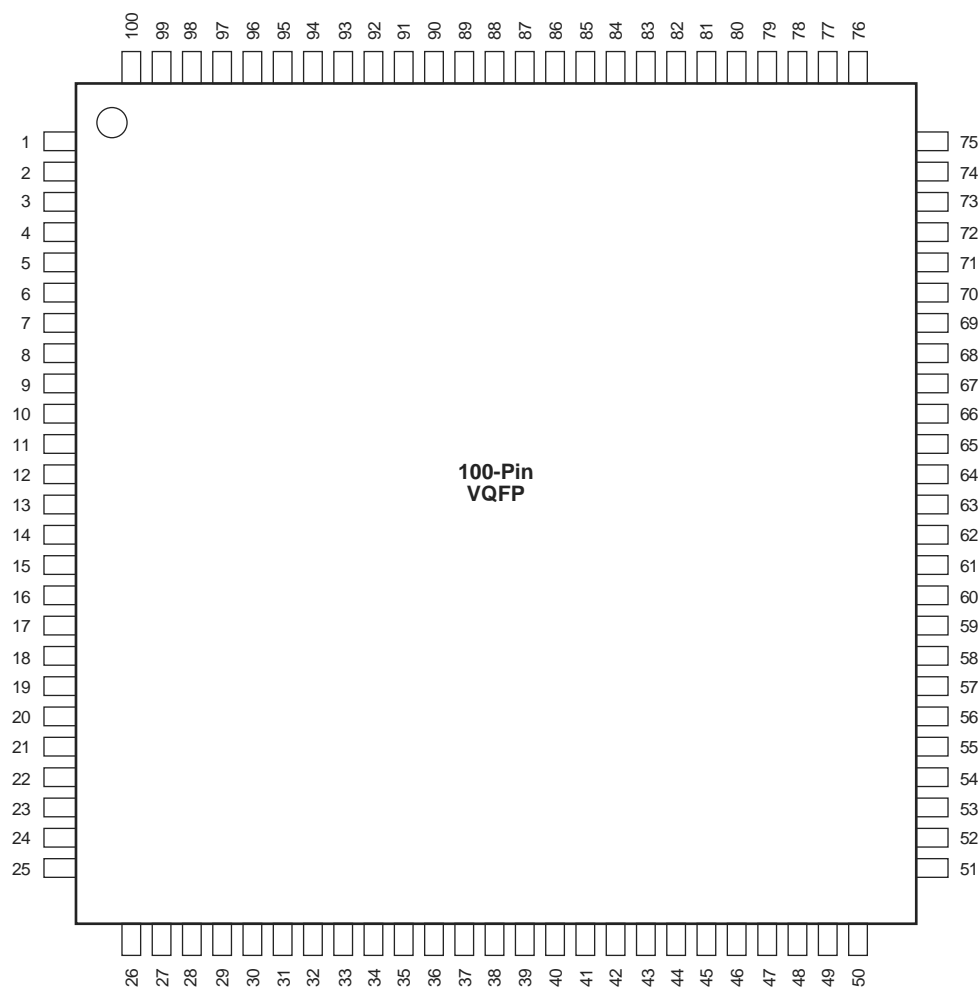
For Package Manufacturing and Environmental information, visit the Resource Center at <http://www.microsemi.com/soc/products/solutions/package/docs.aspx>

TQ176			TQ176		
Pin Number	A1440, A14V40 Function	A1460, A14V60 Function	Pin Number	A1440, A14V40 Function	A1460, A14V60 Function
1	GND	GND	89	GND	GND
2	SDI, I/O	SDI, I/O	98	VCC	VCC
10	MODE	MODE	99	VCC	VCC
11	VCC	VCC	108	GND	GND
20	NC	I/O	109	VCC	VCC
21	GND	GND	110	GND	GND
22	VCC	VCC	119	NC	I/O
23	GND	GND	121	NC	I/O
32	VCC	VCC	122	VCC	VCC
33	VCC	VCC	123	GND	GND
44	GND	GND	124	VCC	VCC
49	NC	I/O	132	IOCLK, I/O	IOCLK, I/O
51	NC	I/O	133	GND	GND
63	NC	I/O	138	NC	I/O
64	PRB, I/O	PRB, I/O	152	CLKA, I/O	CLKA, I/O
65	GND	GND	153	CLKB, I/O	CLKB, I/O
66	VCC	VCC	154	VCC	VCC
67	VCC	VCC	155	GND	GND
69	HCLK, I/O	HCLK, I/O	156	VCC	VCC
82	NC	I/O	157	PRA, I/O	PRA, I/O
83	NC	I/O	158	NC	I/O
87	SDO	SDO	170	NC	I/O
88	IOPCL, I/O	IOPCL, I/O	176	DCLK, I/O	DCLK, I/O

Notes:

1. All unlisted pin numbers are user I/Os.
2. NC denotes no connection.
3. MODE should be terminated to GND through a 10K resistor to enable Actionprobe usage; otherwise it can be terminated directly to GND.

VQ100

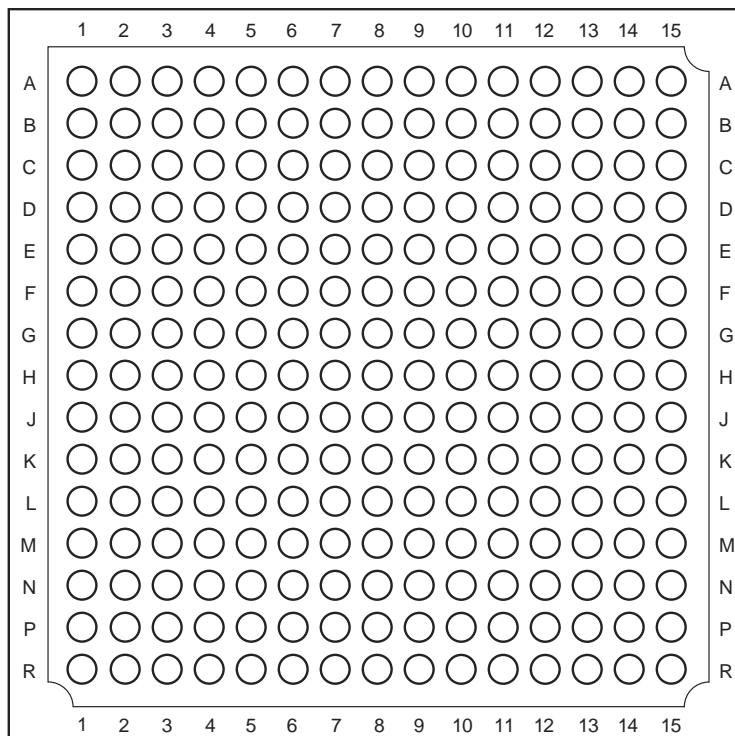


Note: This is the top view.

Note

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BG225

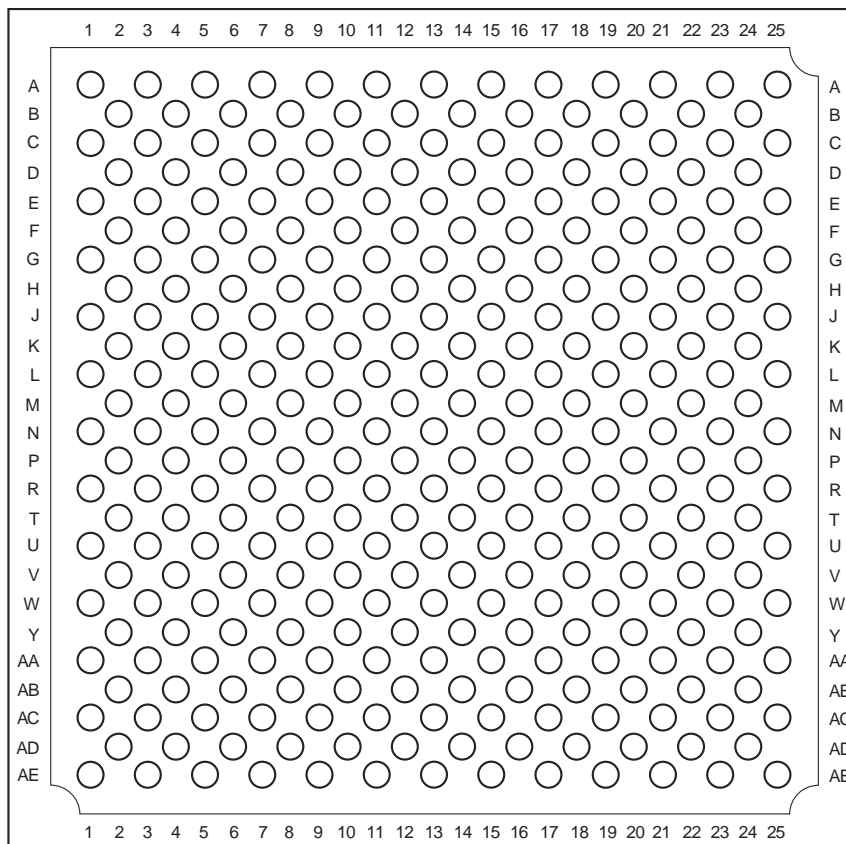


Note: This is the top view.

Note

For Package Manufacturing and Environmental information, visit the Resource Center at <http://www.microsemi.com/soc/products/solutions/package/docs.aspx>

BG313

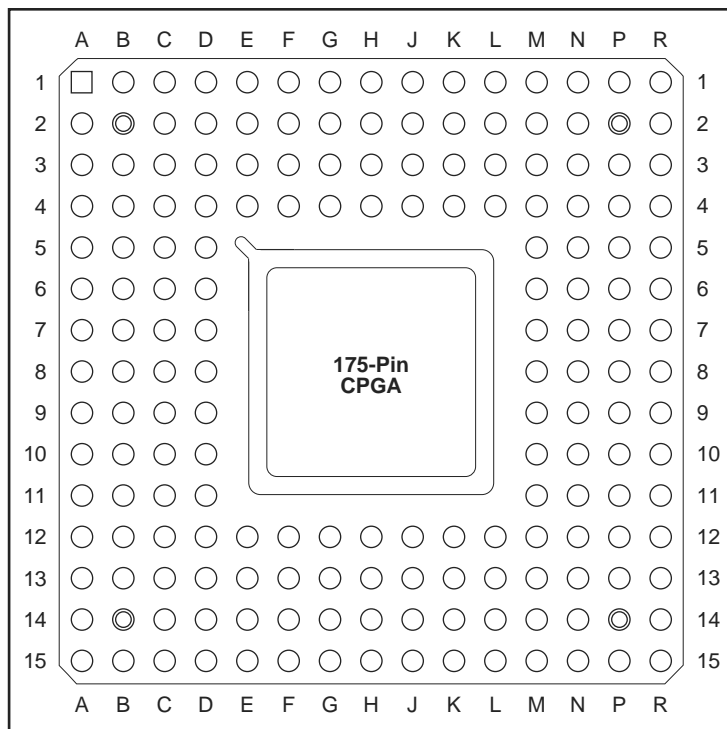


Note: This is the top view.

Note

For Package Manufacturing and Environmental information, visit the Resource Center at <http://www.microsemi.com/soc/products/solutions/package/docs.aspx>

PG175

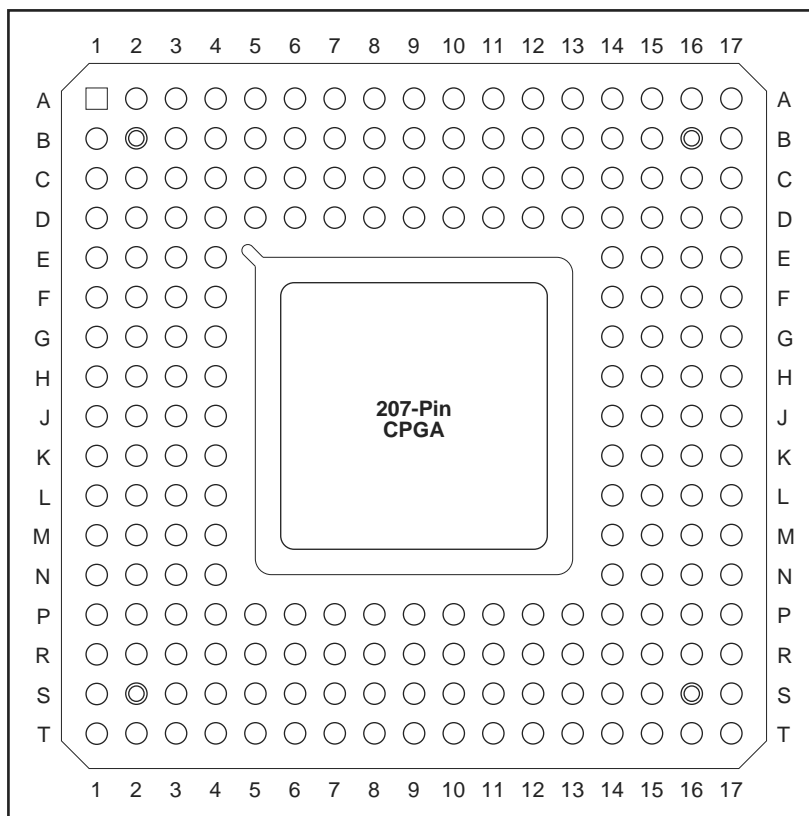


Note: This is the top view.

Note

For Package Manufacturing and Environmental information, visit the Resource Center at <http://www.microsemi.com/soc/products/solutions/package/docs.aspx>

PG207



Note: This is the top view.

Note

For Package Manufacturing and Environmental information, visit the Resource Center at <http://www.microsemi.com/soc/products/solutions/package/docs.aspx>

