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## Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

## Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications,

| Details | |
|---|---|
| Product Status | Obsolete |
| Number of LABs/CLBs | 848 |
| Number of Logic Elements/Cells | - |
| Total RAM Bits | - |
| Number of I/O | 151 |
| Number of Gates | 6000 |
| Voltage - Supply | 4.5V ~ 5.5V |
| Mounting Type | Surface Mount |
| Operating Temperature | -40°C ~ 85°C (TA) |
| Package / Case | 176-LQFP |
| Supplier Device Package | 176-TQFP (24x24) |
| Purchase URL | https://www.e-xfl.com/product-detail/microsemi/a1460a-1tq176i |

# Ordering Information

A14100 A – 1 RQ G 208 C

- **C** — Application (Temperature Range)
  - C = Commercial (0 to +70°C)
  - I = Industrial (–40 to +85°C)
  - M = Military (–55 to +125°C)
  - B = MIL-STD-883
- **208** — Package Lead Count
- **G** — Lead-Free Packaging
  - Blank = Standard Packaging
  - G = RoHS Compliant Packaging
- **RQ** — Package Type
  - PG = Ceramic Pin Grid Array
  - PL = Plastic Leaded Chip Carrier
  - PQ = Plastic Quad Flatpack
  - RQ = Plastic Power Quad Flatpack
  - VQ = Very Thin (1.0 mm) Quad Flatpack
  - TQ = Thin (1.4 mm) Quad Flatpack
  - CQ = Ceramic Quad Flatpack
  - BG = Plastic Ball Grid Array
- **1** — Speed Grade
  - Std = Standard Speed
  - –1 = Approximately 15% faster than Standard
  - –2 = Approximately 25% faster than Standard
  - –3 = Approximately 35% faster than Standard
- **A** — Die Revision
  - A = 1.0 mm CMOS Process
- **A14100** — Part Number
  - A1415A = 1,500 Gates
  - A14V15A = 1,500 Gates (3.3 V)
  - A1425A = 2,500 Gates
  - A14V25A = 2,500 Gates (3.3 V)
  - A1440A = 4,000 Gates
  - A14V40A = 4,000 Gates (3.3 V)
  - A1460A = 6,000 Gates
  - A14V60A = 6,000 Gates (3.3 V)
  - A14100A = 10,000 Gates
  - A14V100A = 10,000 Gates (3.3 V)

Notes:

1. *The –2 and –3 speed grades have been discontinued.*
2. *The Ceramic Pin Grid Array packages PG100, PG133, and PG175 have been discontinued in all device densities, speed grades, and temperature grades.*
3. *The Plastic Ball Grid Array package BG225 has been discontinued in all device densities (specifically for A1460A), all speed grades, and all temperature grades.*
4. *Military Grade devices are no longer available for the A1440A device.*
5. *For more information about discontinued devices, refer to the Product Discontinuation Notices (PDNs) listed below, available on the Microsemi SoC Products Group website:*
   *PDN March 2001*
   *PDN 0104*
   *PDN 0203*
   *PDN 0604*
   *PDN 1004*

The I/O module output Y is used to bring Pad signals into the array or to feed the output register back into the array. This allows the output register to be used in high-speed state machine applications. Side I/O modules have a dedicated output segment for Y extending into the routing channels above and below (similar to logic modules). Top/Bottom I/O modules have no dedicated output segment. Signals coming into the chip from the top or bottom are routed using F-fuses and LVTs (F-fuses and LVTs are explained in detail in the routing section).

## I/O Pad Drivers

All pad drivers are capable of being tristate. Each buffer connects to an associated I/O module with four signals: OE (Output Enable), IE (Input Enable), DataOut, and DataIn. Certain special signals used only during programming and test also connect to the pad drivers: OUTEN (global output enable), INEN (global input enable), and SLEW (individual slew selection). See Figure 2-5.

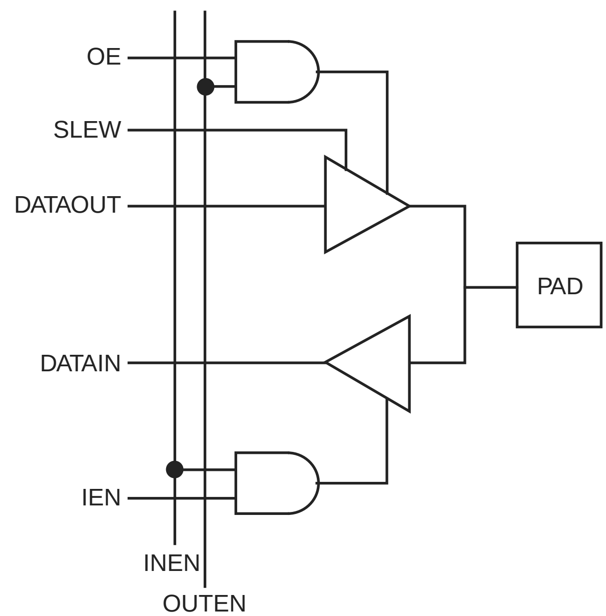



***Figure 2-5 •*** **Function Diagram for I/O Pad Driver**

## Special I/Os

The special I/Os are of two types: temporary and permanent. Temporary special I/Os are used during programming and testing. They function as normal I/Os when the MODE pin is inactive. Permanent special I/Os are user programmed as either normal I/Os or special I/Os. Their function does not change once the device has been programmed. The permanent special I/Os consist of the array clock input buffers (CLKA and CLKB), the hard-wired array clock input buffer (HCLK), the hard-wired I/O clock input buffer (IOCLK), and the hard-wired I/O register preset/clear input buffer (IOPCL). Their function is determined by the I/O macros selected.

# Clock Networks

The ACT 3 architecture contains four clock networks: two high-performance dedicated clock networks and two general purpose routed networks. The high-performance networks function up to 200 MHz, while the general purpose routed networks function up to 150 MHz.

## Horizontal Routing

Horizontal channels are located between the rows of modules and are composed of several routing tracks. The horizontal routing tracks within the channel are divided into one or more segments. The minimum horizontal segment length is the width of a module-pair, and the maximum horizontal segment length is the full length of the channel. Any segment that spans more than one-third the row length is considered a long horizontal segment. A typical channel is shown in Figure 2-7. Undedicated horizontal routing tracks are used to route signal nets. Dedicated routing tracks are used for the global clock networks and for power and ground tie-off tracks.

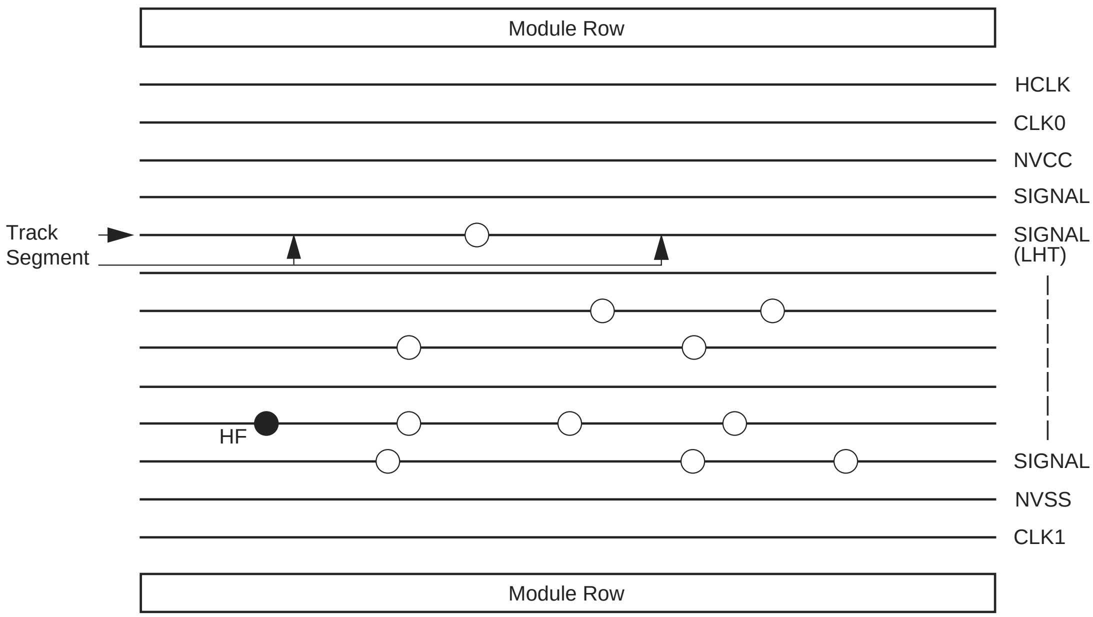



***Figure 2-7 •*** **Horizontal Routing Tracks and Segments**

## Vertical Routing

Other tracks run vertically through the modules. Vertical tracks are of three types: input, output, and long. Vertical tracks are also divided into one or more segments. Each segment in an input track is dedicated to the input of a particular module. Each segment in an output track is dedicated to the output of a particular module. Long segments are uncommitted and can be assigned during routing. Each output segment spans four channels (two above and two below), except near the top and bottom of the array where edge effects occur. LVTs contain either one or two segments. An example of vertical routing tracks and segments is shown in Figure 2-8.

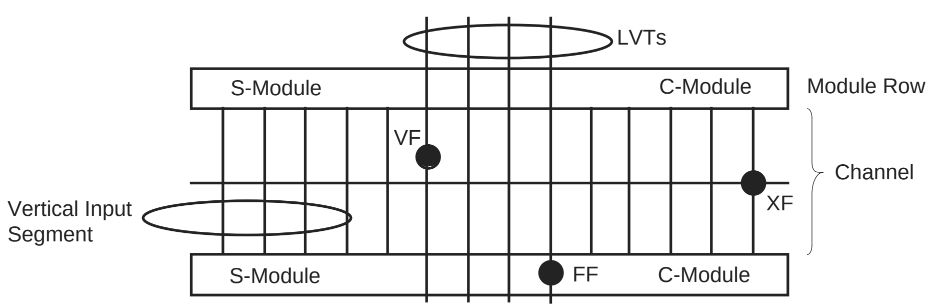



***Figure 2-8 •*** **Vertical Routing Tracks and Segments**

## Antifuse Connections

An antifuse is a “normally open” structure as opposed to the normally closed fuse structure used in PROMs or PALs. The use of antifuses to implement a programmable logic device results in highly testable structures as well as an efficient programming architecture. The structure is highly testable because there are no preexisting connections; temporary connections can be made using pass transistors. These temporary connections can isolate individual antifuses to be programmed as well as isolate individual circuit structures to be tested. This can be done both before and after programming. For example, all metal tracks can be tested for continuity and shorts between adjacent tracks, and the functionality of all logic modules can be verified.

Four types of antifuse connections are used in the routing structure of the ACT 3 array. (The physical structure of the antifuse is identical in each case; only the usage differs.)

Table 2-1 shows four types of antifuses.

***Table 2-1* •  Antifuse Types**

| Type | Description |
|---|---|
| XF | Horizontal-to-vertical connection |
| HF | Horizontal-to-horizontal connection |
| VF | Vertical-to-vertical connection |
| FF | "Fast" vertical connection |

Examples of all four types of connections are shown in Figure 2-7 on page 2-6 and Figure 2-8 on page 2-6.

## Module Interface

Connections to Logic and I/O modules are made through vertical segments that connect to the module inputs and outputs. These vertical segments lie on vertical tracks that span the entire height of the array.

### *Module Input Connections*

The tracks dedicated to module inputs are segmented by pass transistors in each module row. During normal user operation, the pass transistors are inactive, which isolates the inputs of a module from the inputs of the module directly above or below it. During certain test modes, the pass transistors are active to verify the continuity of the metal tracks. Vertical input segments span only the channel above or the channel below. The logic modules are arranged such that half of the inputs are connected to the channel above and half of the inputs to segments in the channel below, as shown in Figure 2-9.

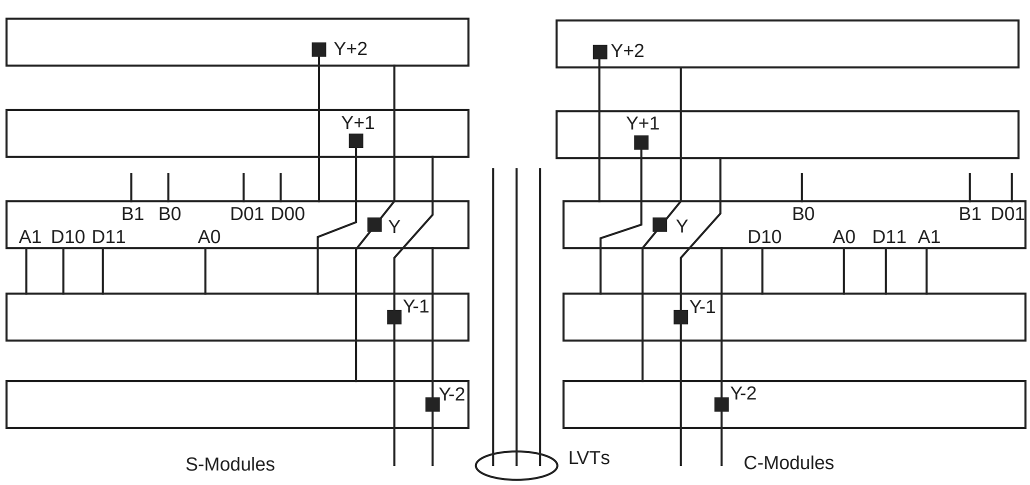



***Figure 2-9* •    Logic Module Routing Interface**

### Module Output Connections

Module outputs have dedicated output segments. Output segments extend vertically two channels above and two channels below, except at the top or bottom of the array. Output segments twist, as shown in Figure 10, so that only four vertical tracks are required.

### LVT Connections

Outputs may also connect to nondedicated segments called Long Vertical Tracks (LVTs). Each module pair in the array shares four LVTs that span the length of the column. Any module in the column pair can connect to one of the LVTs in the column using an FF connection. The FF connection uses antifuses connected directly to the driver stage of the module output, bypassing the isolation transistor. FF antifuses are programmed at a higher current level than HF, VF, or XF antifuses to produce a lower resistance value.

### Antifuse Connections

In general every intersection of a vertical segment and a horizontal segment contains an unprogrammed antifuse (XF-type). One exception is in the case of the clock networks.

### Clock Connections

To minimize loading on the clock networks, a subset of inputs has antifuses on the clock tracks. Only a few of the C-module and S-module inputs can be connected to the clock networks. To further reduce loading on the clock network, only a subset of the horizontal routing tracks can connect to the clock inputs of the S-module.

## Programming and Test Circuits

The array of logic and I/O modules is surrounded by test and programming circuits controlled by the temporary special I/O pins MODE, SDI, and DCLK. The function of these pins is similar to all ACT family devices. The ACT 3 family also includes support for two Actionprobe® circuits, allowing complete observability of any logic or I/O module in the array using the temporary special I/O pins, PRA and PRB.

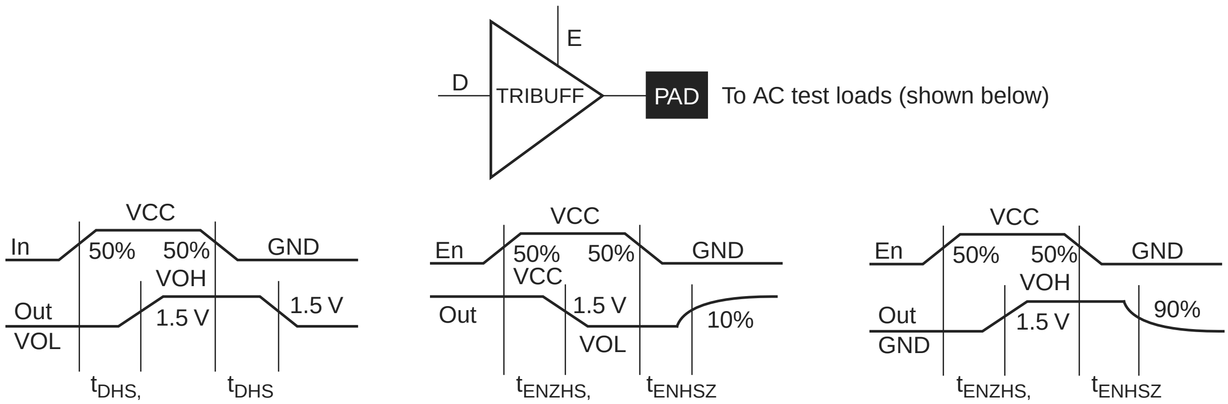



***Figure 2-11* • Output Buffers**

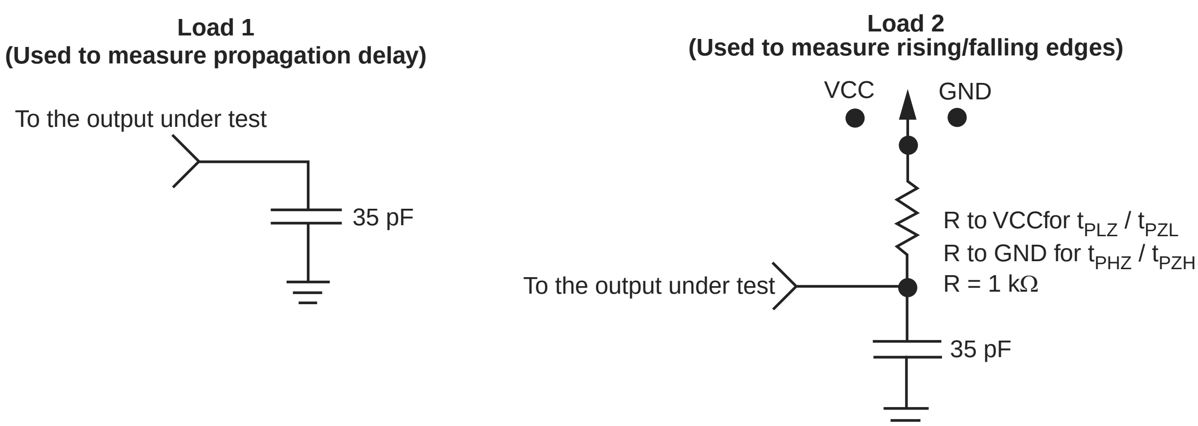



***Figure 2-12* • AC Test Loads**

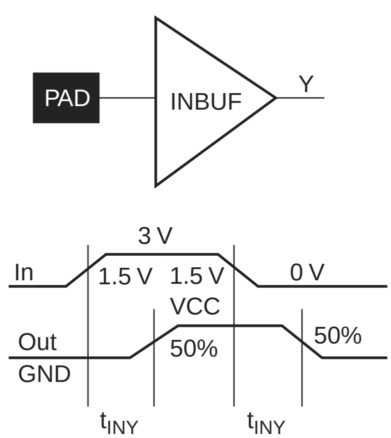



***Figure 2-13* • Input Buffer Delays**

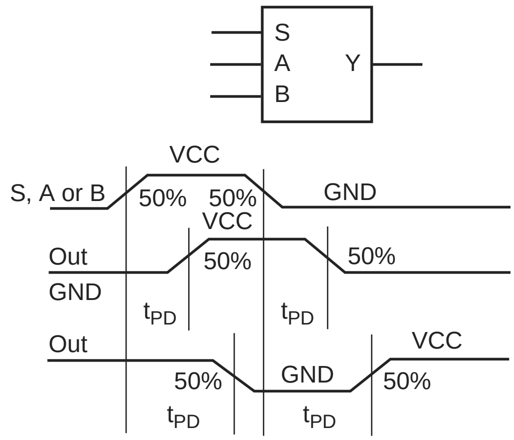



***Figure 2-14 •*** **Module Delays**

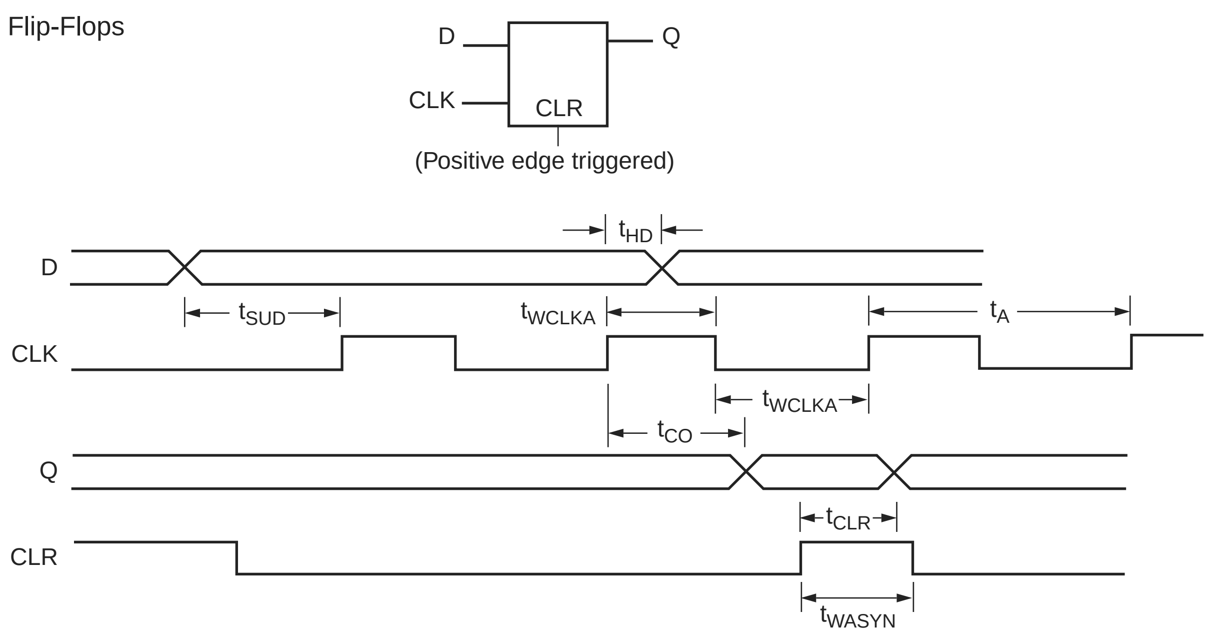



***Figure 2-15 •*** **Sequential Module Timing Characteristics**

## Timing Derating

ACT 3 devices are manufactured in a CMOS process. Therefore, device performance varies according to temperature, voltage, and process variations. Minimum timing parameters reflect maximum operating voltage, minimum operating temperature, and best-case processing. Maximum timing parameters reflect minimum operating voltage, maximum operating temperature, and worst-case processing.

***Table 2-15* • Timing Derating Factor (Temperature and Voltage)**

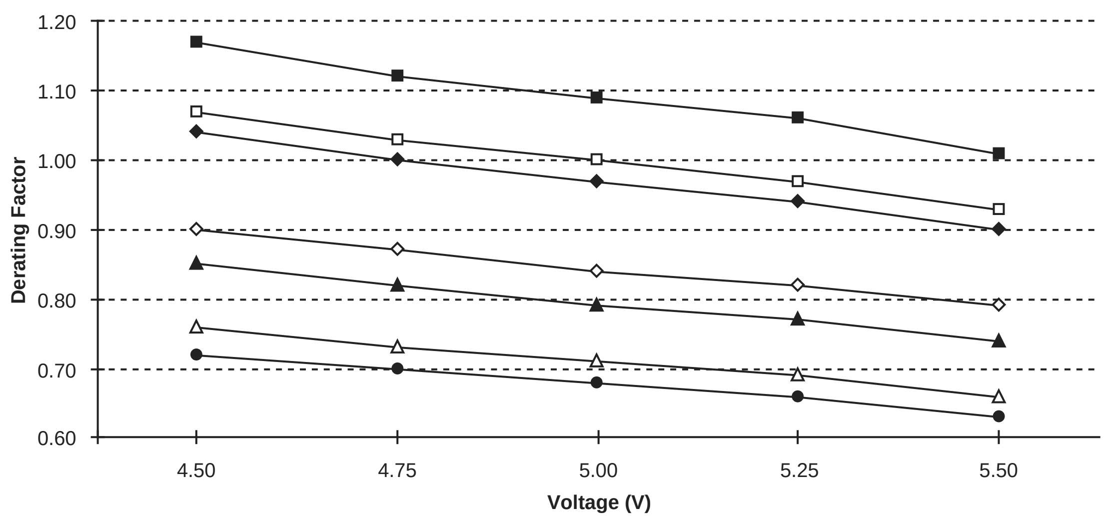
| (Commercial Minimum/Maximum Specification) x | Industrial | | Military | |
|---|---|---|---|---|
| | **Min.** | **Max.** | **Min.** | Max. |
| | 0.66 | 1.07 | 0.63 | 1.17 |

***Table 2-16* • Timing Derating Factor for Designs at Typical Temperature ($T_J$ = 25°C) and Voltage (5.0 V)**

| | |
|---|---|
| (Commercial Maximum Specification) x | 0.85 |

***Table 2-17* • Temperature and Voltage Derating Factors (normalized to Worst-Case Commercial, TJ = 4.75 V, 70°C)**

| | **–55** | **–40** | **0** | **25** | **70** | **85** | **125** |
|---|---|---|---|---|---|---|---|
| **4.50** | 0.72 | 0.76 | 0.85 | 0.90 | 1.04 | 1.07 | 1.117 |
| **4.75** | 0.70 | 0.73 | 0.82 | 0.87 | 1.00 | 1.03 | 1.12 |
| **5.00** | 0.68 | 0.71 | 0.79 | 0.84 | 0.97 | 1.00 | 1.09 |
| **5.25** | 0.66 | 0.69 | 0.77 | 0.82 | 0.94 | 0.97 | 1.06 |
| **5.50** | 0.63 | 0.66 | 0.74 | 0.79 | 0.90 | 0.93 | 1.01 |




*Note: This derating factor applies to all routing and propagation delays.*

***Figure 2-18* • Junction Temperature and Voltage Derating Curves (normalized to Worst-Case Commercial, TJ = 4.75 V, 70°C)**

## A1425A, A14V25A Timing Characteristics (continued)

***Table 2-24*** **• A1425A, A14V25A Worst-Case Commercial Conditions, VCC = 4.75 V, $T_J$ = 70°C**

| I/O Module – TTL Output Timing[1] | | –3 Speed[2] | | –2 Speed[2] | | –1 Speed | | Std. Speed | | 3.3 V Speed[1] | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Parameter/Description | | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | |
| $t_{DHS}$ | Data to Pad, High Slew | | 5.0 | | 5.6 | | 6.4 | | 7.5 | | 9.8 | ns |
| $t_{DLS}$ | Data to Pad, Low Slew | | 8.0 | | 9.0 | | 10.2 | | 12.0 | | 15.6 | ns |
| $t_{ENZHS}$ | Enable to Pad, Z to H/L, High Slew | | 4.0 | | 4.5 | | 5.1 | | 6.0 | | 7.8 | ns |
| $t_{ENZLS}$ | Enable to Pad, Z to H/L, Low Slew | | 7.4 | | 8.3 | | 9.4 | | 11.0 | | 14.3 | ns |
| $t_{ENHSZ}$ | Enable to Pad, H/L to Z, High Slew | | 6.5 | | 7.5 | | 8.5 | | 10.0 | | 13.0 | ns |
| $t_{ENLSZ}$ | Enable to Pad, H/L to Z, Low Slew | | 6.5 | | 7.5 | | 8.5 | | 10.0 | | 13.0 | ns |
| $t_{CKHS}$ | IOCLK Pad to Pad H/L, High Slew | | 7.5 | | 7.5 | | 9.0 | | 10.0 | | 13.0 | ns |
| $t_{CKLS}$ | IOCLK Pad to Pad H/L, Low Slew | | 11.3 | | 11.3 | | 13.5 | | 15.0 | | 19.5 | ns |
| $d_{TLHHS}$ | Delta Low to High, High Slew | | 0.02 | | 0.02 | | 0.03 | | 0.03 | | 0.04 | ns/pF |
| $d_{TLHLS}$ | Delta Low to High, Low Slew | | 0.05 | | 0.05 | | 0.06 | | 0.07 | | 0.09 | ns/pF |
| $d_{THLHS}$ | Delta High to Low, High Slew | | 0.04 | | 0.04 | | 0.04 | | 0.05 | | 0.07 | ns/pF |
| $d_{THLLS}$ | Delta High to Low, Low Slew | | 0.05 | | 0.05 | | 0.06 | | 0.07 | | 0.09 | ns/pF |
| **I/O Module – CMOS Output Timing[1]** | | | | | | | | | | | | |
| $t_{DHS}$ | Data to Pad, High Slew | | 6.2 | | 7.0 | | 7.9 | | 9.3 | | 12.1 | ns |
| $t_{DLS}$ | Data to Pad, Low Slew | | 11.7 | | 13.1 | | 14.9 | | 17.5 | | 22.8 | ns |
| $t_{ENZHS}$ | Enable to Pad, Z to H/L, High Slew | | 5.2 | | 5.9 | | 6.6 | | 7.8 | | 10.1 | ns |
| $t_{ENZLS}$ | Enable to Pad, Z to H/L, Low Slew | | 8.9 | | 10.0 | | 11.3 | | 13.3 | | 17.3 | ns |
| $t_{ENHSZ}$ | Enable to Pad, H/L to Z, High Slew | | 6.7 | | 7.5 | | 8.5 | | 10.0 | | 13.0 | ns |
| $t_{ENLSZ}$ | Enable to Pad, H/L to Z, Low Slew | | 6.7 | | 7.5 | | 9.0 | | 10.0 | | 13.0 | ns |
| $t_{CKHS}$ | IOCLK Pad to Pad H/L, High Slew | | 8.9 | | 8.9 | | 10.7 | | 11.8 | | 15.3 | ns |
| $t_{CKLS}$ | IOCLK Pad to Pad H/L, Low Slew | | 13.0 | | 13.0 | | 15.6 | | 17.3 | | 22.5 | ns |
| $d_{TLHHS}$ | Delta Low to High, High Slew | | 0.04 | | 0.04 | | 0.05 | | 0.06 | | 0.08 | ns/pF |
| $d_{TLHLS}$ | Delta Low to High, Low Slew | | 0.07 | | 0.08 | | 0.09 | | 0.11 | | 0.14 | ns/pF |
| $d_{THLHS}$ | Delta High to Low, High Slew | | 0.03 | | 0.03 | | 0.03 | | 0.04 | | 0.05 | ns/pF |
| $d_{THLLS}$ | Delta High to Low, Low Slew | | 0.04 | | 0.04 | | 0.04 | | 0.05 | | 0.07 | ns/pF |

*Notes: **

1. *Delays based on 35 pF loading.*
2. *The –2 and –3 speed grades have been discontinued. Refer to PDN 0104, PDN 0203, PDN 0604, and PDN 1004 at http://www.microsemi.com/soc/support/notifications/default.aspx#pdn.*

## A1440A, A14V40A Timing Characteristics

***Table 2-26*** **• A1440A, A14V40A Worst-Case Commercial Conditions, VCC = 4.75 V, $T_J$ = 70°C[1]**

| Logic Module Propagation Delays[2] | | –3 Speed[3] | | –2 Speed[3] | | –1 Speed | | Std. Speed | | 3.3 V Speed[1] | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **Parameter/Description** | | **Min.** | **Max.** | **Min.** | **Max.** | **Min.** | **Max.** | **Min.** | **Max.** | **Min.** | **Max.** | |
| $t_{PD}$ | Internal Array Module | | 2.0 | | 2.3 | | 2.6 | | 3.0 | | 3.9 | ns |
| $t_{CO}$ | Sequential Clock to Q | | 2.0 | | 2.3 | | 2.6 | | 3.0 | | 3.9 | ns |
| $t_{CLR}$ | Asynchronous Clear to Q | | 2.0 | | 2.3 | | 2.6 | | 3.0 | | 3.9 | ns |
| **Predicted Routing Delays[4]** | | | | | | | | | | | | |
| $t_{RD1}$ | FO = 1 Routing Delay | | 0.9 | | 1.0 | | 1.1 | | 1.3 | | 1.7 | ns |
| $t_{RD2}$ | FO = 2 Routing Delay | | 1.2 | | 1.4 | | 1.6 | | 1.8 | | 2.4 | ns |
| $t_{RD3}$ | FO = 3 Routing Delay | | 1.4 | | 1.6 | | 1.8 | | 2.1 | | 2.8 | ns |
| $t_{RD4}$ | FO = 4 Routing Delay | | 1.7 | | 1.9 | | 2.2 | | 2.5 | | 3.3 | ns |
| $t_{RD8}$ | FO = 8 Routing Delay | | 2.8 | | 3.2 | | 3.6 | | 4.2 | | 5.5 | ns |
| **Logic Module Sequential Timing** | | | | | | | | | | | | |
| $t_{SUD}$ | Flip-Flop Data Input Setup | 0.5 | | 0.6 | | 0.7 | | 0.8 | | 0.8 | | ns |
| $t_{HD}$ | Flip-Flop Data Input Hold | 0.0 | | 0.0 | | 0.0 | | 0.0 | | 0.0 | | ns |
| $t_{SUD}$ | Latch Data Input Setup | 0.5 | | 0.6 | | 0.7 | | 0.8 | | 0.8 | | ns |
| $t_{HD}$ | Latch Data Input Hold | 0.0 | | 0.0 | | 0.0 | | 0.0 | | 0.0 | | ns |
| $t_{WASYN}$ | Asynchronous Pulse Width | 1.9 | | 2.4 | | 3.2 | | 3.8 | | 4.8 | | ns |
| $t_{WCLKA}$ | Flip-Flop Clock Pulse Width | 1.9 | | 2.4 | | 3.2 | | 3.8 | | 4.8 | | ns |
| $t_A$ | Flip-Flop Clock Input Period | 4.0 | | 5.0 | | 6.8 | | 8.0 | | 10.0 | | ns |
| $f_{MAX}$ | Flip-Flop Clock Frequency | | 250 | | 200 | | 150 | | 125 | | 100 | MHz |

*Notes:*

1. *VCC = 3.0 V for 3.3 V specifications.*
2. *For dual-module macros, use $t_{PD} + t_{RD1} + t_{PDn} + t_{CO} + t_{RD1} + t_{PDn}$ or $t_{PD1} + t_{RD1} + t_{SUD}$, whichever is appropriate.*
3. *The –2 and –3 speed grades have been discontinued. Refer to PDN 0104, PDN 0203, PDN 0604, and PDN 1004 at http://www.microsemi.com/soc/support/notifications/default.aspx#pdn.*
4. *Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual worst-case performance. Post-route timing is based on actual routing delay measurements performed on the device prior to shipment.*

## A14100A, A14V100A Timing Characteristics (continued)

***Table 2-37*** **• A14100A, A14V100A Worst-Case Commercial Conditions, VCC = 4.75 V, $T_J$ = 70°C**

| Dedicated (hardwired) I/O Clock Network | | –3 Speed[1] | | –2 Speed[1] | | –1 Speed | | Std. Speed | | 3.3 V Speed[1] | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **Parameter/Description** | | **Min.** | **Max.** | **Min.** | **Max.** | **Min.** | **Max.** | **Min.** | **Max.** | **Min.** | **Max.** | |
| $t_{IOCKH}$ | Input Low to High (pad to I/O module input) | | 2.3 | | 2.6 | | 3.0 | | 3.5 | | 4.5 | ns |
| $t_{IOPWH}$ | Minimum Pulse Width High | 2.4 | | 3.3 | | 3.8 | | 4.8 | | 6.5 | | ns |
| $t_{IPOWL}$ | Minimum Pulse Width Low | 2.4 | | 3.3 | | 3.8 | | 4.8 | | 6.5 | | ns |
| $t_{IOSAPW}$ | Minimum Asynchronous Pulse Width | 2.4 | | 3.3 | | 3.8 | | 4.8 | | 6.5 | | ns |
| $t_{IOCKSW}$ | Maximum Skew | | 0.6 | | 0.6 | | 0.7 | | 0.8 | | 0.6 | ns |
| $t_{IOP}$ | Minimum Period | 5.0 | | 6.8 | | 8.0 | | 10.0 | | 13.4 | | ns |
| $f_{IOMAX}$ | Maximum Frequency | | 200 | | 150 | | 125 | | 100 | | 75 | MHz |
| **Dedicated (hardwired) Array Clock** | | | | | | | | | | | | |
| $t_{HCKH}$ | Input Low to High (pad to S-module input) | | 3.7 | | 4.1 | | 4.7 | | 5.5 | | 7.0 | ns |
| $t_{HCKL}$ | Input High to Low (pad to S-module input) | | 3.7 | | 4.1 | | 4.7 | | 5.5 | | 7.0 | ns |
| $t_{HPWH}$ | Minimum Pulse Width High | 2.4 | | 3.3 | | 3.8 | | 4.8 | | 6.5 | | ns |
| $t_{HPWL}$ | Minimum Pulse Width Low | 2.4 | | 3.3 | | 3.8 | | 4.8 | | 6.5 | | ns |
| $t_{HCKSW}$ | Delta High to Low, Low Slew | | 0.6 | | 0.6 | | 0.7 | | 0.8 | | 0.6 | ns |
| $t_{HP}$ | Minimum Period | 5.0 | | 6.8 | | 8.0 | | 10.0 | | 13.4 | | ns |
| $f_{HMAX}$ | Maximum Frequency | | 200 | | 150 | | 125 | | 100 | | 75 | MHz |
| **Routed Array Clock Networks** | | | | | | | | | | | | |
| $t_{RCKH}$ | Input Low to High (FO = 64) | | 6.0 | | 6.8 | | 7.7 | | 9.0 | | 11.8 | ns |
| $t_{RCKL}$ | Input High to Low (FO = 64) | | 6.0 | | 6.8 | | 7.7 | | 9.0 | | 11.8 | ns |
| $t_{RPWH}$ | Min. Pulse Width High (FO = 64) | 4.1 | | 4.5 | | 5.4 | | 6.1 | | 8.2 | | ns |
| $t_{RPWL}$ | Min. Pulse Width Low (FO = 64) | 4.1 | | 4.5 | | 5.4 | | 6.1 | | 8.2 | | ns |
| $t_{RCKSW}$ | Maximum Skew (FO = 128) | | 1.2 | | 1.4 | | 1.6 | | 1.8 | | 1.8 | ns |
| $t_{RP}$ | Minimum Period (FO = 64) | 8.3 | | 9.3 | | 11.1 | | 12.5 | | 16.7 | | ns |
| $f_{RMAX}$ | Maximum Frequency (FO = 64) | | 120 | | 105 | | 90 | | 80 | | 60 | MHz |
| **Clock-to-Clock Skews** | | | | | | | | | | | | |
| $t_{IOHCKSW}$ | I/O Clock to H-Clock Skew | 0.0 | 2.6 | 0.0 | 2.7 | 0.0 | 2.9 | 0.0 | 3.0 | 0.0 | 3.0 | ns |
| $t_{IORCKSW}$ | I/O Clock to R-Clock Skew (FO = 64)<br>(FO = 350) | 0.0<br>0.0 | 1.7<br>5.0 | 0.0<br>0.0 | 1.7<br>5.0 | 0.0<br>0.0 | 1.7<br>5.0 | 0.0<br>0.0 | 1.7<br>5.0 | 0.0<br>0.0 | 5.0<br>5.0 | ns |
| $t_{HRCKSW}$ | H-Clock to R-Clock Skew (FO = 64)<br>(FO = 350) | 0.0<br>0.0 | 1.3<br>3.0 | 0.0<br>0.0 | 1.0<br>3.0 | 0.0<br>0.0 | 1.0<br>3.0 | 0.0<br>0.0 | 1.0<br>3.0 | 0.0<br>0.0 | 1.0<br>3.0 | ns |

*Notes: **

1. *The –2 and –3 speed grades have been discontinued. Refer to PDN 0104, PDN 0203, PDN 0604, and PDN 1004 at http://www.microsemi.com/soc/support/notifications/default.aspx#pdn.*
2. *Delays based on 35 pF loading.*

# Pin Descriptions

**CLKA** **Clock A (Input)**

Clock input for clock distribution networks. The Clock input is buffered prior to clocking the logic modules. This pin can also be used as an I/O.

**CLKB** **Clock B (Input)**

Clock input for clock distribution networks. The Clock input is buffered prior to clocking the logic modules. This pin can also be used as an I/O.

**GND** **Ground**

LOW supply voltage.

**HCLK** **Dedicated (Hard-wired) Array Clock (Input)**

Clock input for sequential modules. This input is directly wired to each S-Module and offers clock speeds independent of the number of S-Modules being driven. This pin can also be used as an I/O.

**I/O** **Input/Output (Input, Output)**

The I/O pin functions as an input, output, three-state, or bidirectional buffer. Input and output levels are compatible with standard TTL and CMOS specifications. Unused I/O pins are tristated by the Designer Series software.

**IOCLK** **Dedicated (Hard-wired) I/O Clock (Input)**

Clock input for I/O modules. This input is directly wired to each I/O module and offers clock speeds independent of the number of I/O modules being driven. This pin can also be used as an I/O.

**IOPCL** **Dedicated (Hard-wired) I/O Preset/Clear (Input)**

Input for I/O preset or clear. This global input is directly wired to the preset and clear inputs of all I/O registers. This pin functions as an I/O when no I/O preset or clear macros are used.

**MODE** **Mode (Input)**

The MODE pin controls the use of diagnostic pins (DCLK, PRA, PRB, SDI). When the MODE pin is HIGH, the special functions are active. When the MODE pin is LOW, the pins function as I/Os. To provide Actionprobe capability, the MODE pin should be terminated to GND through a 10K resistor so that the MODE pin can be pulled high when required.

**NC** **No Connection**

This pin is not connected to circuitry within the device.

**PRA** **Probe A (Output)**

The Probe A pin is used to output data from any user-defined design node within the device. This independent diagnostic pin can be used in conjunction with the Probe B pin to allow real-time diagnostic output of any signal path within the device. The Probe A pin can be used as a user-defined I/O when debugging has been completed. The pin's probe capabilities can be permanently disabled to protect programmed design confidentiality. PRA is accessible when the MODE pin is HIGH. This pin functions as an I/O when the MODE pin is LOW.

**PRB** **Probe B (Output)**

The Probe B pin is used to output data from any user-defined design node within the device. This independent diagnostic pin can be used in conjunction with the Probe A pin to allow real-time diagnostic output of any signal path within the device. The Probe B pin can be used as a user-defined I/O when debugging has been completed. The pin's probe capabilities can be permanently disabled to protect programmed design confidentiality. PRB is accessible when the MODE pin is HIGH. This pin functions as an I/O when the MODE pin is LOW.

**SDI** **Serial Data Input (Input)**

Serial data input for diagnostic probe and device programming. SDI is active when the MODE pin is HIGH. This pin functions as an I/O when the MODE pin is LOW.

| PQ208, RQ208 | | |
|---|---|---|
| **Pin Number** | **A1460, A14V60 Function** | **A14100, A14V100 Function** |
| 1 | GND | GND |
| 2 | SDI, I/O | SDI, I/O |
| 11 | MODE | MODE |
| 12 | VCC | VCC |
| 25 | VCC | VCC |
| 26 | GND | GND |
| 27 | VCC | VCC |
| 28 | GND | GND |
| 40 | VCC | VCC |
| 41 | VCC | VCC |
| 52 | GND | GND |
| 53 | NC | I/O |
| 60 | VCC | VCC |
| 65 | NC | I/O |
| 76 | PRB, I/O | PRB, I/O |
| 77 | GND | GND |
| 78 | VCC | VCC |
| 79 | GND | GND |
| 80 | VCC | VCC |
| 82 | HCLK, I/O | HCLK, I/O |
| 98 | VCC | VCC |
| 102 | NC | I/O |
| 103 | SDO | SDO |
| 104 | IOPCL, I/O | IOPCL, I/O |
| 105 | GND | GND |
| 114 | VCC | VCC |

| PQ208, RQ208 | | |
|---|---|---|
| **Pin Number** | **A1460, A14V60 Function** | **A14100, A14V100 Function** |
| 115 | VCC | VCC |
| 116 | NC | I/O |
| 129 | GND | GND |
| 130 | VCC | VCC |
| 131 | GND | GND |
| 132 | VCC | VCC |
| 145 | VCC | VCC |
| 146 | GND | GND |
| 147 | NC | I/O |
| 148 | VCC | VCC |
| 156 | IOCLK, I/O | IOCLK, I/O |
| 157 | GND | GND |
| 158 | NC | I/O |
| 164 | VCC | VCC |
| 180 | CLKA, I/O | CLKA, I/O |
| 181 | CLKB, I/O | CLKB, I/O |
| 182 | VCC | VCC |
| 183 | GND | GND |
| 184 | VCC | VCC |
| 185 | GND | GND |
| 186 | PRA, I/O | PRA, I/O |
| 195 | NC | I/O |
| 201 | VCC | VCC |
| 205 | NC | I/O |
| 208 | DCLK, I/O | DCLK, I/O |

*Notes:*

1. All unlisted pin numbers are user I/Os.
2. NC denotes no connection.
3. MODE should be terminated to GND through a 10K resistor to enable Actionprobe usage; otherwise it can be terminated directly to GND.

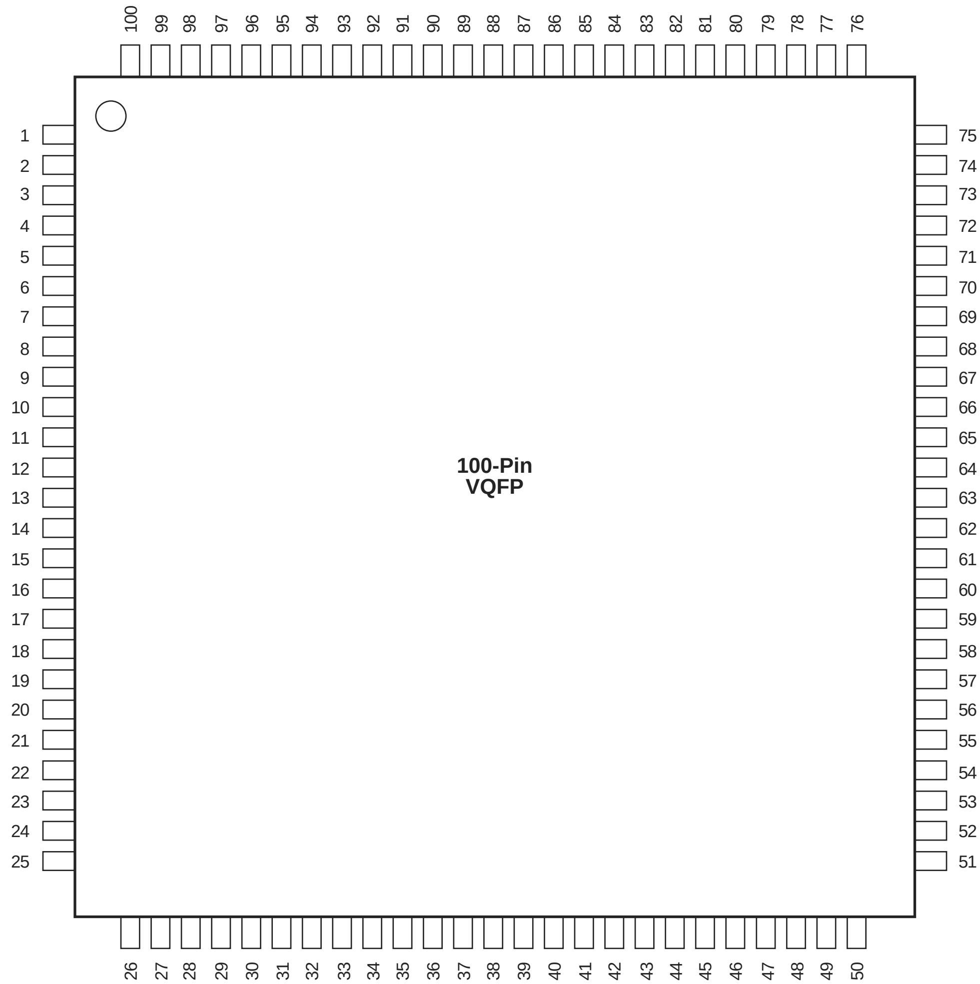
| TQ176 | | |
|---|---|---|
| Pin Number | A1440, A14V40 Function | A1460, A14V60 Function |
| 1 | GND | GND |
| 2 | SDI, I/O | SDI, I/O |
| 10 | MODE | MODE |
| 11 | VCC | VCC |
| 20 | NC | I/O |
| 21 | GND | GND |
| 22 | VCC | VCC |
| 23 | GND | GND |
| 32 | VCC | VCC |
| 33 | VCC | VCC |
| 44 | GND | GND |
| 49 | NC | I/O |
| 51 | NC | I/O |
| 63 | NC | I/O |
| 64 | PRB, I/O | PRB, I/O |
| 65 | GND | GND |
| 66 | VCC | VCC |
| 67 | VCC | VCC |
| 69 | HCLK, I/O | HCLK, I/O |
| 82 | NC | I/O |
| 83 | NC | I/O |
| 87 | SDO | SDO |
| 88 | IOPCL, I/O | IOPCL, I/O |

| TQ176 | | |
|---|---|---|
| Pin Number | A1440, A14V40 Function | A1460, A14V60 Function |
| 89 | GND | GND |
| 98 | VCC | VCC |
| 99 | VCC | VCC |
| 108 | GND | GND |
| 109 | VCC | VCC |
| 110 | GND | GND |
| 119 | NC | I/O |
| 121 | NC | I/O |
| 122 | VCC | VCC |
| 123 | GND | GND |
| 124 | VCC | VCC |
| 132 | IOCLK, I/O | IOCLK, I/O |
| 133 | GND | GND |
| 138 | NC | I/O |
| 152 | CLKA, I/O | CLKA, I/O |
| 153 | CLKB, I/O | CLKB, I/O |
| 154 | VCC | VCC |
| 155 | GND | GND |
| 156 | VCC | VCC |
| 157 | PRA, I/O | PRA, I/O |
| 158 | NC | I/O |
| 170 | NC | I/O |
| 176 | DCLK, I/O | DCLK, I/O |

*Notes:*

1. All unlisted pin numbers are user I/Os.
2. NC denotes no connection.
3. MODE should be terminated to GND through a 10K resistor to enable Actionprobe usage; otherwise it can be terminated directly to GND.

# VQ100




*Note: This is the top view.*

## *Note*

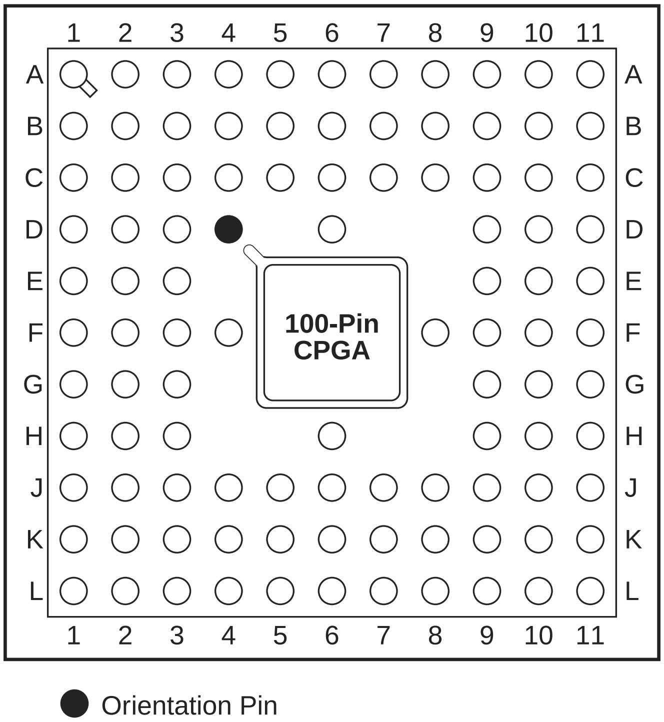
For Package Manufacturing and Environmental information, visit the Resource Center at http://www.microsemi.com/soc/products/solutions/package/docs.aspx

| CQ132 | | CQ132 | |
|---|---|---|---|
| **Pin Number** | **A1425 Function** | **Pin Number** | **A1425 Function** |
| 1 | NC | 67 | NC |
| 2 | GND | 74 | GND |
| 3 | SDI, I/O | 75 | VCC |
| 9 | MODE | 78 | VCC |
| 10 | GND | 89 | VCC |
| 11 | VCC | 90 | GND |
| 22 | VCC | 91 | VCC |
| 26 | GND | 92 | GND |
| 27 | VCC | 98 | IOCLK, I/O |
| 34 | NC | 99 | NC |
| 36 | GND | 100 | NC |
| 42 | GND | 101 | GND |
| 43 | VCC | 106 | GND |
| 48 | PRB, I/O | 107 | VCC |
| 50 | HCLK, I/O | 116 | CLKA, I/O |
| 58 | GND | 117 | CLKB, I/O |
| 59 | VCC | 118 | PRA, I/O |
| 63 | SDO | 122 | GND |
| 64 | IOPCL, I/O | 123 | VCC |
| 65 | GND | 131 | DCLK, I/O |
| 66 | NC | 132 | NC |

*Notes:*

1. All unlisted pin numbers are user I/Os.
2. NC denotes no connection.
3. MODE should be terminated to GND through a 10K resistor to enable Actionprobe usage; otherwise it can be terminated directly to GND.

# PG100

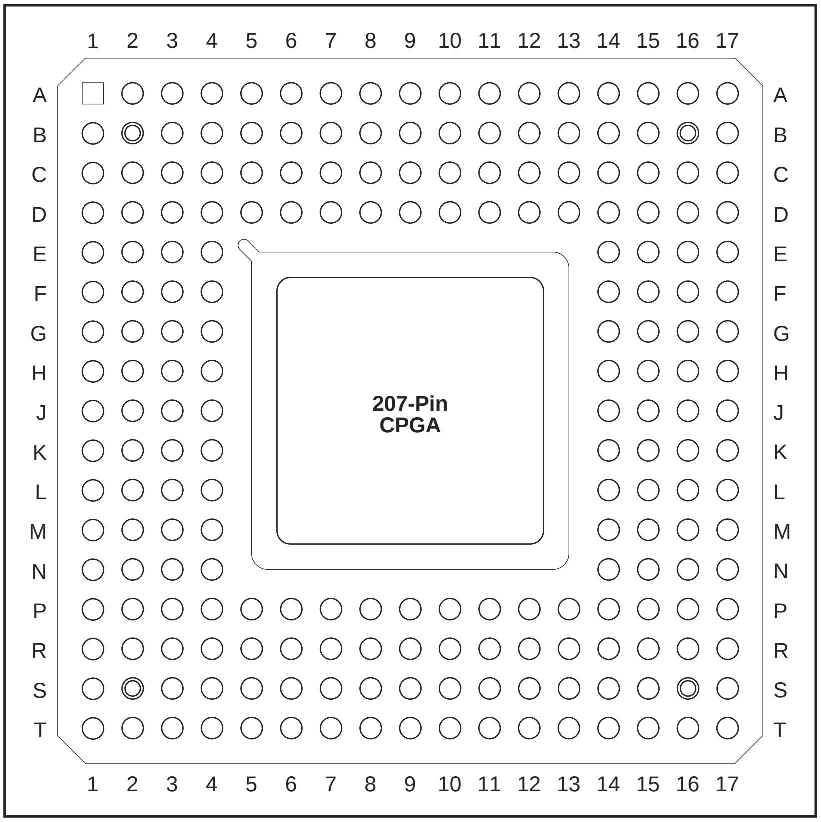



*Note: This is the top view.*

## *Note*

For Package Manufacturing and Environmental information, visit the Resource Center at http://www.microsemi.com/soc/products/solutions/package/docs.aspx

# PG207




*Note: This is the top view.*

## *Note*

For Package Manufacturing and Environmental information, visit the Resource Center at http://www.microsemi.com/soc/products/solutions/package/docs.aspx

# 4 – Datasheet Information

## List of Changes

The following table lists critical changes that were made in each version of the datasheet.

| Revision | Changes | Page |
|---|---|---|
| Revision 3 (January 2012) | The description for SDO pins had earlier been removed from the datasheet and has now been included again, in the "Pin Descriptions" section (SAR 35820). | 2-21 |
| | SDO pin numbers had earlier been removed from package pin assignment tables in the datasheet, and have now been restored to the pin tables (SAR 35820). | 3-1 |
| Revision 2 (September 2011) | The ACT 3 datasheet was formatted newly in the style used for current datasheets. The same information is present (other than noted in the list of changes for this revision) but divided into chapters. | N/A |
| | The datasheet was revised to note in multiple places that speed grades –2 and –3 have been discontinued. The following device/package combinations have been discontinued for all speed grades and temperatures (SAR 33872):<br>A1415 PG100<br>A1425 PG133<br>A1440 PG175<br>A1460 BG225<br>Refer to PDN 0104, PDN 0203, PDN 0604, and PDN 1004. | I and others |
| | The "Features" section was revised to state the clock-to-ouput time and on-chip performance for –1 speed grade as 9.0 ns and 186 MHz. The "General Description" section was revised in accordance (SAR 33872). | I |
| | The maximum performance values were updated in Table 1 • ACT 3 Family Product Information, and now reflect worst-case commercial for the –1 speed grade (SAR 33872). | I |
| | The "Product Plan" table was updated as follows to conform to current offerings (SAR 33872):<br>The A1415A device is offered in PL84, PG100, and VQ100 packages for Military application.<br>The A1440A device is offered in TQ176 and VQ100 packages for Industrial application. | III |
| | Table 1-1 • Chip-to-Chip Performance (worst-case commercial) was updated to include data for all speed grades instead of only –3 (SAR 33872). | 1-2 |
| | Figure 1-1 • Predictable Performance (worst-case commercial, –1 speed grade) was revised to reflect values for the –1 speed grade (SAR 33872). | 1-1 |
| | Figure 2-10 • Timing Model was updated to show data for the –1 speed grade instead of –3 (SAR 33872). | 2-16 |
| | Table 2-14 • Logic Module and Routing Delay by Fanout (ns); Worst-Case Commercial Conditions was updated to include data for all speed grades instead of only –3 (SAR 33872). | 2-20 |
| | Package names used in the "Package Pin Assignments" section and throughout the document were revised to match standards given in *Package Mechanical Drawings* (SAR 27395). | 3-1 |