**Welcome to E-XFL.COM**

**Understanding Embedded - FPGAs (Field Programmable Gate Array)**

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

**Applications of Embedded - FPGAs**

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications,

| Details | |
|---|---|
| Product Status | Obsolete |
| Number of LABs/CLBs | 848 |
| Number of Logic Elements/Cells | - |
| Total RAM Bits | - |
| Number of I/O | 151 |
| Number of Gates | 6000 |
| Voltage - Supply | 4.5V ~ 5.5V |
| Mounting Type | Surface Mount |
| Operating Temperature | -40°C ~ 85°C (TA) |
| Package / Case | 176-LQFP |
| Supplier Device Package | 176-TQFP (24x24) |
| Purchase URL | https://www.e-xfl.com/product-detail/microsemi/a1460a-1tqg176i |

*Table 1-1 •* **Chip-to-Chip Performance (worst-case commercial)**

| Device and Speed Grade | $t_{CKHS}$ (ns) | $t_{TRACE}$ (ns) | $t_{INSU}$ (ns) | Total (ns) | MHz |
|---|---|---|---|---|---|
| A1425A -3 | 7.5 | 1.0 | 1.8 | 10.3 | 97 |
| A1460A -3 | 9.0 | 1.0 | 1.3 | 11.3 | 88 |
| A1425A -2 | 7.5 | 1.0 | 2.0 | 10.5 | 95 |
| A1460A -2 | 9.0 | 1.0 | 1.5 | 11.5 | 87 |
| A1425A -1 | 9.0 | 1.0 | 2.3 | 12.3 | 81 |
| A1460A -1 | 10.0 | 1.0 | 1.8 | 12.8 | 78 |
| A1425A STD | 10.0 | 1.0 | 2.7 | 13.7 | 73 |
| A1460A STD | 11.5 | 1.0 | 2.0 | 14.5 | 69 |

*Note:  The –2 and –3 speed grades have been discontinued. Refer to PDN 0104, PDN 0203, PDN 0604, and PDN 1004 at http://www.microsemi.com/soc/support/notifications/default.aspx#pdn.*

# Horizontal Routing

Horizontal channels are located between the rows of modules and are composed of several routing tracks. The horizontal routing tracks within the channel are divided into one or more segments. The minimum horizontal segment length is the width of a module-pair, and the maximum horizontal segment length is the full length of the channel. Any segment that spans more than one-third the row length is considered a long horizontal segment. A typical channel is shown in Figure 2-7. Undedicated horizontal routing tracks are used to route signal nets. Dedicated routing tracks are used for the global clock networks and for power and ground tie-off tracks.
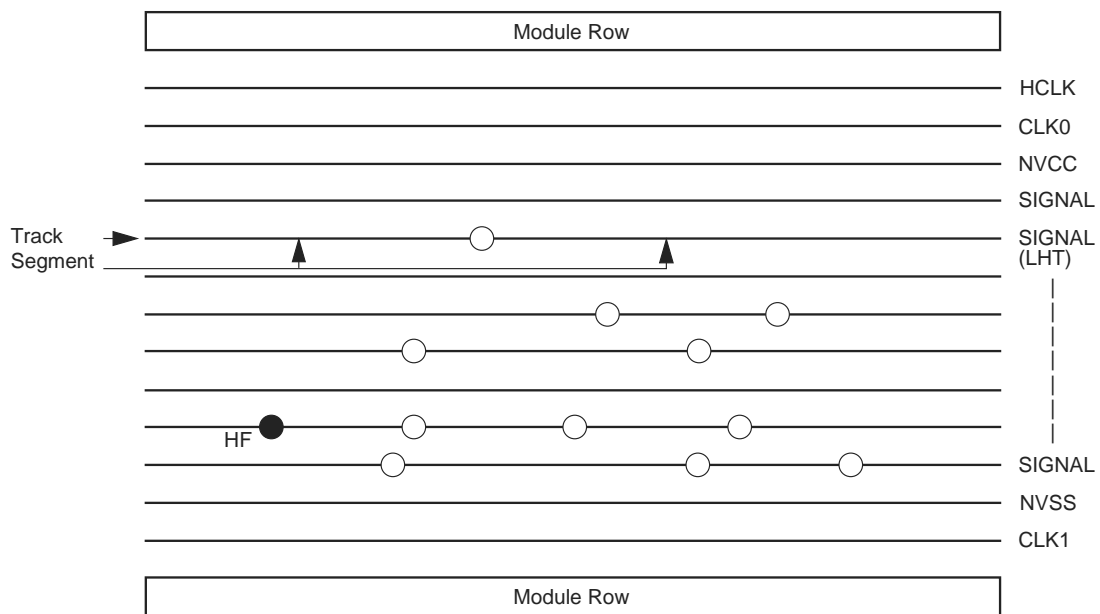


*Figure 2-7 •   Horizontal Routing Tracks and Segments*

# Vertical Routing

Other tracks run vertically through the modules. Vertical tracks are of three types: input, output, and long. Vertical tracks are also divided into one or more segments. Each segment in an input track is dedicated to the input of a particular module. Each segment in an output track is dedicated to the output of a particular module. Long segments are uncommitted and can be assigned during routing. Each output segment spans four channels (two above and two below), except near the top and bottom of the array where edge effects occur. LVTs contain either one or two segments. An example of vertical routing tracks and segments is shown in Figure 2-8.
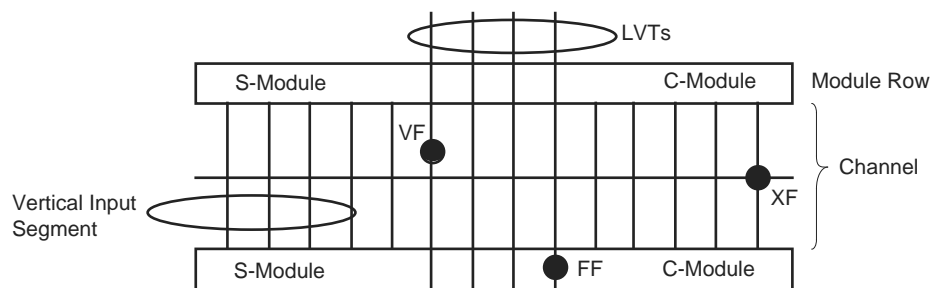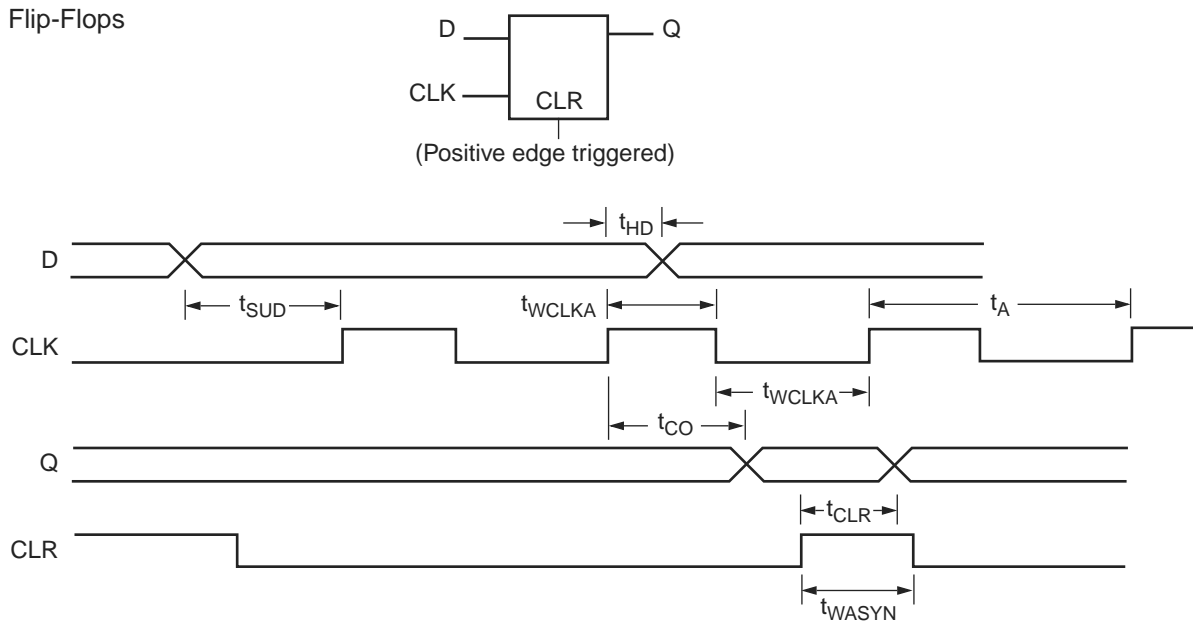


*Figure 2-8 •   Vertical Routing Tracks and Segments*
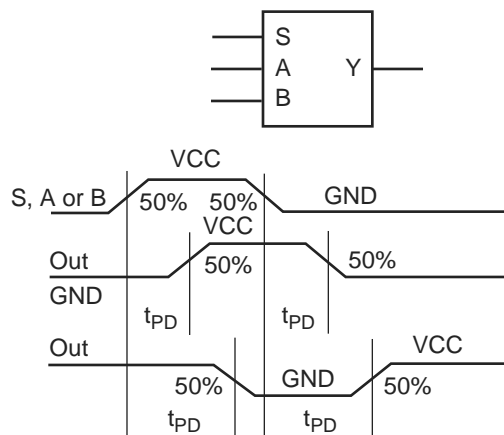
*Figure 2-14 •* **Module Delays**



*Figure 2-15 •* **Sequential Module Timing Characteristics**

## Tightest Delay Distributions

Propagation delay between logic modules depends on the resistive and capacitive loading of the routing tracks, the interconnect elements, and the module inputs being driven. Propagation delay increases as the length of routing tracks, the number of interconnect elements, or the number of inputs increases.

From a design perspective, the propagation delay can be statistically correlated or modeled by the fanout (number of loads) driven by a module. Higher fanout usually requires some paths to have longer lengths of routing track. The ACT 3 family delivers the tightest fanout delay distribution of any FPGA. This tight distribution is achieved in two ways: by decreasing the delay of the interconnect elements and by decreasing the number of interconnect elements per path.

Microsemi's patented PLICE antifuse offers a very low resistive/capacitive interconnect. The ACT 3 family's antifuses, fabricated in 0.8 micron m lithography, offer nominal levels of 200$\Omega$ resistance and 6 femtofarad (fF) capacitance per antifuse. The ACT 3 fanout distribution is also tighter than alternative devices due to the low number of antifuses required per interconnect path. The ACT 3 family's proprietary architecture limits the number of antifuses per path to only four, with 90% of interconnects using only two antifuses.

The ACT 3 family's tight fanout delay distribution offers an FPGA design environment in which fanout can be traded for the increased performance of reduced logic level designs. This also simplifies performance estimates when designing with ACT 3 devices.

*Table 2-14 • Logic Module and Routing Delay by Fanout (ns); Worst-Case Commercial Conditions*

| Speed Grade | FO = 1 | FO = 2 | FO = 3 | FO = 4 | FO = 8 |
|---|---|---|---|---|---|
| ACT 3 –3 | 2.9 | 3.2 | 3.4 | 3.7 | 4.8 |
| ACT 3 –2 | 3.3 | 3.7 | 3.9 | 4.2 | 5.5 |
| ACT 3 –1 | 3.7 | 4.2 | 4.4 | 4.8 | 6.2 |
| ACT 3 STD | 4.3 | 4.8 | 5.1 | 5.5 | 7.2 |

*Notes:*

1. *Obtained by added $t_{RD(x=FO)}$ to $t_{PD}$ from the Logic Module Timing Characteristics Tables found in this datasheet.*

2. *The –2 and –3 speed grades have been discontinued. Refer to PDN 0104, PDN 0203, PDN 0604, and PDN 1004 at http://www.microsemi.com/soc/support/notifications/default.aspx#pdn.*

## Timing Characteristics

Timing characteristics for ACT 3 devices fall into three categories: family dependent, device dependent, and design dependent. The input and output buffer characteristics are common to all ACT 3 family members. Internal routing delays are device dependent. Design dependency means actual delays are not determined until after placement and routing of the user's design is complete. Delay values may then be determined by using the ALS Timer utility or performing simulation with post-layout delays.

### Critical Nets and Typical Nets

Propagation delays are expressed only for typical nets, which are used for initial design performance evaluation. Critical net delays can then be applied to the most time-critical paths. Critical nets are determined by net property assignment prior to placement and routing. Up to 6% of the nets in a design may be designated as critical, while 90% of the nets in a design are typical.

### Long Tracks

Some nets in the design use long tracks. Long tracks are special routing resources that span multiple rows, columns, or modules. Long tracks employ three and sometimes four antifuse connections. This increases capacitance and resistance, result ng in longer net delays for macros connected to long tracks. Typically up to 6% of nets in a fully utilized device require long tracks. Long tracks contribute approximately 4 ns to 14 ns delay. This additional delay is represented statistically in higher fanout (FO = 8) routing delays in the datasheet specifications section.

### *A1415A, A14V15A Timing Characteristics (continued)*

*Table 2-19 •* **A1415A, A14V15A Worst-Case Commercial Conditions, VCC = 4.75 V, T$_J$ = 70°C**

| I/O Module Input Propagation Delays | | –3 Speed[1] | | –2 Speed[1] | | –1 Speed | | Std. Speed | | 3.3 V Speed[2] | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **Parameter/Description** | | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | |
| t$_{INY}$ | Input Data Pad to Y | | 2.8 | | 3.2 | | 3.6 | | 4.2 | | 5.5 | ns |
| t$_{ICKY}$ | Input Reg IOCLK Pad to Y | | 4.7 | | 5.3 | | 6.0 | | 7.0 | | 9.2 | ns |
| t$_{OCKY}$ | Output Reg IOCLK Pad to Y | | 4.7 | | 5.3 | | 6.0 | | 7.0 | | 9.2 | ns |
| t$_{ICLRY}$ | Input Asynchronous Clear to Y | | 4.7 | | 5.3 | | 6.0 | | 7.0 | | 9.2 | ns |
| t$_{OCLRY}$ | Output Asynchronous Clear to Y | | 4.7 | | 5.3 | | 6.0 | | 7.0 | | 9.2 | ns |
| **Predicted Input Routing Delays[2]** | | | | | | | | | | | | |
| t$_{RD1}$ | FO = 1 Routing Delay | | 0.9 | | 1.0 | | 1.1 | | 1.3 | | 1.7 | ns |
| t$_{RD2}$ | FO = 2 Routing Delay | | 1.2 | | 1.4 | | 1.6 | | 1.8 | | 2.4 | ns |
| t$_{RD3}$ | FO = 3 Routing Delay | | 1.4 | | 1.6 | | 1.8 | | 2.1 | | 2.8 | ns |
| t$_{RD4}$ | FO = 4 Routing Delay | | 1.7 | | 1.9 | | 2.2 | | 2.5 | | 3.3 | ns |
| t$_{RD8}$ | FO = 8 Routing Delay | | 2.8 | | 3.2 | | 3.6 | | 4.2 | | 5.5 | ns |
| **I/O Module Sequential Timing (wrt IOCLK pad)** | | | | | | | | | | | | |
| t$_{INH}$ | Input F-F Data Hold | 0.0 | | 0.0 | | 0.0 | | 0.0 | | 0.0 | | ns |
| t$_{INSU}$ | Input F-F Data Setup | 2.0 | | 2.3 | | 2.5 | | 3.0 | | 3.0 | | ns |
| t$_{IDEH}$ | Input Data Enable Hold | 0.0 | | 0.0 | | 0.0 | | 0.0 | | 0.0 | | ns |
| t$_{IDESU}$ | Input Data Enable Setup | 5.8 | | 6.5 | | 7.5 | | 8.6 | | 8.6 | | ns |
| t$_{OUTH}$ | Output F-F Data hold | 0.7 | | 0.8 | | 0.9 | | 1.0 | | 1.0 | | ns |
| t$_{OUTSU}$ | Output F-F Data Setup | 0.7 | | 0.8 | | 0.9 | | 1.0 | | 1.0 | | ns |
| t$_{ODEH}$ | Output Data Enable Hold | 0.3 | | 0.4 | | 0.4 | | 0.5 | | 0.5 | | ns |
| f$_{ODESU}$ | Output Data Enable Setup | 1.3 | | 1.5 | | 1.7 | | 2.0 | | 2.0 | | ns |

*Notes:*

1. *The –2 and –3 speed grades have been discontinued. Please refer to the Product Discontinuation Notices (PDNs) listed below:*

   *PDN March 2001*
   *PDN 0104*
   *PDN 0203*
   *PDN 0604*
   *PDN 1004*

2. *Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual worst-case performance. Post-route timing is based on actual routing delay measurements performed on the device prior to shipment.*

## *A1415A, A14V15A Timing Characteristics (continued)*

*Table 2-21 • A1415A, A14V15A Worst-Case Commercial Conditions, VCC = 4.75 V, T$_J$ = 70°C*

| Dedicated (hardwired) I/O Clock Network | | −3 Speed | | −2 Speed | | −1 Speed | | Std. Speed | | 3.3 V Speed[1] | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Parameter/Description | | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | |
| t$_{IOCKH}$ | Input Low to High (pad to I/O module input) | | 2.0 | | 2.3 | | 2.6 | | 3.0 | | 3.5 | ns |
| t$_{IOPWH}$ | Minimum Pulse Width High | 1.9 | | 2.4 | | 3.3 | | 3.8 | | 4.8 | | ns |
| t$_{IPOWL}$ | Minimum Pulse Width Low | 1.9 | | 2.4 | | 3.3 | | 3.8 | | 4.8 | | ns |
| t$_{IOSAPW}$ | Minimum Asynchronous Pulse Width | 1.9 | | 2.4 | | 3.3 | | 3.8 | | 4.8 | | ns |
| t$_{IOCKSW}$ | Maximum Skew | | 0.4 | | 0.4 | | 0.4 | | 0.4 | | 0.4 | ns |
| t$_{IOP}$ | Minimum Period | 4.0 | | 5.0 | | 6.8 | | 8.0 | | 10.0 | | ns |
| f$_{IOMAX}$ | Maximum Frequency | | 250 | | 200 | | 150 | | 125 | | 100 | MHz |
| **Dedicated (hardwired) Array Clock** | | | | | | | | | | | | |
| t$_{HCKH}$ | Input Low to High (pad to S-module input) | | 3.0 | | 3.4 | | 3.9 | | 4.5 | | 5.5 | ns |
| t$_{HCKL}$ | Input High to Low (pad to S-module input) | | 3.0 | | 3.4 | | 3.9 | | 4.5 | | 5.5 | ns |
| t$_{HPWH}$ | Minimum Pulse Width High | 1.9 | | 2.4 | | 3.3 | | 3.8 | | 4.8 | | ns |
| t$_{HPWL}$ | Minimum Pulse Width Low | 1.9 | | 2.4 | | 3.3 | | 3.8 | | 4.8 | | ns |
| t$_{HCKSW}$ | Delta High to Low, Low Slew | | 0.3 | | 0.3 | | 0.3 | | 0.3 | | 0.3 | ns |
| t$_{HP}$ | Minimum Period | 4.0 | | 5.0 | | 6.8 | | 8.0 | | 10.0 | | ns |
| f$_{HMAX}$ | Maximum Frequency | | 250 | | 200 | | 150 | | 125 | | 100 | MHz |
| **Routed Array Clock Networks** | | | | | | | | | | | | |
| t$_{RCKH}$ | Input Low to High (FO = 64) | | 3.7 | | 4.1 | | 4.7 | | 5.5 | | 9.0 | ns |
| t$_{RCKL}$ | Input High to Low (FO = 64) | | 4.0 | | 4.5 | | 5.1 | | 6.0 | | 9.0 | ns |
| t$_{RPWH}$ | Min. Pulse Width High (FO = 64) | 3.3 | | 3.8 | | 4.2 | | 4.9 | | 6.5 | | ns |
| t$_{RPWL}$ | Min. Pulse Width Low (FO = 64) | 3.3 | | 3.8 | | 4.2 | | 4.9 | | 6.5 | | ns |
| t$_{RCKSW}$ | Maximum Skew (FO = 128) | | 0.7 | | 0.8 | | 0.9 | | 1.0 | | 1.0 | ns |
| t$_{RP}$ | Minimum Period (FO = 64) | 6.8 | | 8.0 | | 8.7 | | 10.0 | | 13.4 | | ns |
| f$_{RMAX}$ | Maximum Frequency (FO = 64) | | 150 | | 125 | | 115 | | 100 | | 75 | MHz |
| **Clock-to-Clock Skews** | | | | | | | | | | | | |
| t$_{IOHCKSW}$ | I/O Clock to H-Clock Skew | 0.0 | 1.7 | 0.0 | 1.8 | 0.0 | 2.0 | 0.0 | 2.2 | 0.0 | 3.0 | ns |
| t$_{IORCKSW}$ | I/O Clock to R-Clock Skew (FO = 64) | 0.0 | 1.0 | 0.0 | 1.0 | 0.0 | 1.0 | 0.0 | 1.0 | 0.0 | 3.0 | ns |
| t$_{HRCKSW}$ | H-Clock to R-Clock Skew (FO = 64) (FO = 50% maximum) | 0.0 | 1.0 | 0.0 | 1.0 | 0.0 | 1.0 | 0.0 | 1.0 | 0.0<br>0.0 | 3.0<br>3.0 | ns |

*Notes:*

*1. Delays based on 35 pF loading.*

*2. The −2 and −3 speed grades have been discontinued. Refer to PDN 0104, PDN 0203, PDN 0604, and PDN 1004 at http://www.microsemi.com/soc/support/notifications/default.aspx#pdn.*

## *A1440A, A14V40A Timing Characteristics (continued)*

*Table 2-27 •* **A1440A, A14V40A Worst-Case Commercial Conditions, VCC = 4.75 V, T$_J$ = 70°C**

| I/O Module Input Propagation Delays | | –3 Speed[1] | | –2 Speed[1] | | –1 Speed | | Std. Speed | | 3.3 V Speed[1] | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **Parameter/Description** | | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | |
| t$_{INY}$ | Input Data Pad to Y | | 2.8 | | 3.2 | | 3.6 | | 4.2 | | 5.5 | ns |
| t$_{ICKY}$ | Input Reg IOCLK Pad to Y | | 4.7 | | 5.3 | | 6.0 | | 7.0 | | 9.2 | ns |
| t$_{OCKY}$ | Output Reg IOCLK Pad to Y | | 4.7 | | 5.3 | | 6.0 | | 7.0 | | 9.2 | ns |
| t$_{ICLRY}$ | Input Asynchronous Clear to Y | | 4.7 | | 5.3 | | 6.0 | | 7.0 | | 9.2 | ns |
| t$_{OCLRY}$ | Output Asynchronous Clear to Y | | 4.7 | | 5.3 | | 6.0 | | 7.0 | | 9.2 | ns |
| **Predicted Input Routing Delays[2]** | | | | | | | | | | | | |
| t$_{RD1}$ | FO = 1 Routing Delay | | 0.9 | | 1.0 | | 1.1 | | 1.3 | | 1.7 | ns |
| t$_{RD2}$ | FO = 2 Routing Delay | | 1.2 | | 1.4 | | 1.6 | | 1.8 | | 2.4 | ns |
| t$_{RD3}$ | FO = 3 Routing Delay | | 1.4 | | 1.6 | | 1.8 | | 2.1 | | 2.8 | ns |
| t$_{RD4}$ | FO = 4 Routing Delay | | 1.7 | | 1.9 | | 2.2 | | 2.5 | | 3.3 | ns |
| t$_{RD8}$ | FO = 8 Routing Delay | | 2.8 | | 3.2 | | 3.6 | | 4.2 | | 5.5 | ns |
| **I/O Module Sequential Timing (wrt IOCLK pad)** | | | | | | | | | | | | |
| t$_{INH}$ | Input F-F Data Hold | 0.0 | | 0.0 | | 0.0 | | 0.0 | | 0.0 | | ns |
| t$_{INSU}$ | Input F-F Data Setup | 1.8 | | 1.7 | | 2.0 | | 2.3 | | 2.3 | | ns |
| t$_{IDEH}$ | Input Data Enable Hold | 0.0 | | 0.0 | | 0.0 | | 0.0 | | 0.0 | | ns |
| t$_{IDESU}$ | Input Data Enable Setup | 5.8 | | 6.5 | | 7.5 | | 8.6 | | 8.6 | | ns |
| t$_{OUTH}$ | Output F-F Data hold | 0.7 | | 0.8 | | 0.9 | | 1.0 | | 1.0 | | ns |
| t$_{OUTSU}$ | Output F-F Data Setup | 0.7 | | 0.8 | | 0.9 | | 1.0 | | 1.0 | | ns |
| t$_{ODEH}$ | Output Data Enable Hold | 0.3 | | 0.4 | | 0.4 | | 0.5 | | 0.5 | | ns |
| f$_{ODESU}$ | Output Data Enable Setup | 1.3 | | 1.5 | | 1.7 | | 2.0 | | 2.0 | | ns |

*Notes:*

1. *The –2 and –3 speed grades have been discontinued. Refer to PDN 0104, PDN 0203, PDN 0604, and PDN 1004 at http://www.microsemi.com/soc/support/notifications/default.aspx#pdn.*

2. *Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual worst-case performance. Post-route timing is based on actual routing delay measurements performed on the device prior to shipment.*

## A1460A, A14V60A Timing Characteristics (continued)

*Table 2-32 •* **A1460A, A14V60A Worst-Case Commercial Conditions, VCC = 4.75 V, $T_J$ = 70°C**

| I/O Module – TTL Output Timing[1] | | –3 Speed[2] | | –2 Speed[2] | | –1 Speed | | Std. Speed | | 3.3 V Speed[1] | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **Parameter/Description** | | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | |
| $t_{DHS}$ | Data to Pad, High Slew | | 5.0 | | 5.6 | | 6.4 | | 7.5 | | 9.8 | ns |
| $t_{DLS}$ | Data to Pad, Low Slew | | 8.0 | | 9.0 | | 10.2 | | 12.0 | | 15.6 | ns |
| $t_{ENZHS}$ | Enable to Pad, Z to H/L, High Slew | | 4.0 | | 4.5 | | 5.1 | | 6.0 | | 7.8 | ns |
| $t_{ENZLS}$ | Enable to Pad, Z to H/L, Low Slew | | 7.4 | | 8.3 | | 9.4 | | 11.0 | | 14.3 | ns |
| $t_{ENHSZ}$ | Enable to Pad, H/L to Z, High Slew | | 7.8 | | 8.7 | | 9.9 | | 11.6 | | 15.1 | ns |
| $t_{ENLSZ}$ | Enable to Pad, H/L to Z, Low Slew | | 7.4 | | 8.3 | | 9.4 | | 11.0 | | 14.3 | ns |
| $t_{CKHS}$ | IOCLK Pad to Pad H/L, High Slew | | 9.0 | | 9.0 | | 10.0 | | 11.5 | | 15.0 | ns |
| $t_{CKLS}$ | IOCLK Pad to Pad H/L, Low Slew | | 12.8 | | 12.8 | | 15.3 | | 17.0 | | 22.1 | ns |
| $d_{TLHHS}$ | Delta Low to High, High Slew | | 0.02 | | 0.02 | | 0.03 | | 0.03 | | 0.04 | ns/pF |
| $d_{TLHLS}$ | Delta Low to High, Low Slew | | 0.05 | | 0.05 | | 0.06 | | 0.07 | | 0.09 | ns/pF |
| $d_{THLHS}$ | Delta High to Low, High Slew | | 0.04 | | 0.04 | | 0.04 | | 0.05 | | 0.07 | ns/pF |
| $d_{THLLS}$ | Delta High to Low, Low Slew | | 0.05 | | 0.05 | | 0.06 | | 0.07 | | 0.09 | ns/pF |
| **I/O Module – CMOS Output Timing[1]** | | | | | | | | | | | | |
| $t_{DHS}$ | Data to Pad, High Slew | | 6.2 | | 7.0 | | 7.9 | | 9.3 | | 12.1 | ns |
| $t_{DLS}$ | Data to Pad, Low Slew | | 11.7 | | 13.1 | | 14.9 | | 17.5 | | 22.8 | ns |
| $t_{ENZHS}$ | Enable to Pad, Z to H/L, High Slew | | 5.2 | | 5.9 | | 6.6 | | 7.8 | | 10.1 | ns |
| $t_{ENZLS}$ | Enable to Pad, Z to H/L, Low Slew | | 8.9 | | 10.0 | | 11.3 | | 13.3 | | 17.3 | ns |
| $t_{ENHSZ}$ | Enable to Pad, H/L to Z, High Slew | | 7.4 | | 8.3 | | 9.4 | | 11.0 | | 14.3 | ns |
| $t_{ENLSZ}$ | Enable to Pad, H/L to Z, Low Slew | | 7.4 | | 8.3 | | 9.4 | | 11.0 | | 14.3 | ns |
| $t_{CKHS}$ | IOCLK Pad to Pad H/L, High Slew | | 10.4 | | 10.4 | | 12.1 | | 13.8 | | 17.9 | ns |
| $t_{CKLS}$ | IOCLK Pad to Pad H/L, Low Slew | | 14.5 | | 14.5 | | 17.4 | | 19.3 | | 25.1 | ns |
| $d_{TLHHS}$ | Delta Low to High, High Slew | | 0.04 | | 0.04 | | 0.05 | | 0.06 | | 0.08 | ns/pF |
| $d_{TLHLS}$ | Delta Low to High, Low Slew | | 0.07 | | 0.08 | | 0.09 | | 0.11 | | 0.14 | ns/pF |
| $d_{THLHS}$ | Delta High to Low, High Slew | | 0.03 | | 0.03 | | 0.03 | | 0.04 | | 0.05 | ns/pF |
| $d_{THLLS}$ | Delta High to Low, Low Slew | | 0.04 | | 0.04 | | 0.04 | | 0.05 | | 0.07 | ns/pF |

*Notes:*

1. *Delays based on 35 pF loading.*
2. *The –2 and –3 speed grades have been discontinued. Refer to PDN 0104, PDN 0203, PDN 0604, and PDN 1004 at http://www.microsemi.com/soc/support/notifications/default.aspx#pdn.*

## *A14100A, A14V100A Timing Characteristics (continued)*

*Table 2-37 •* **A14100A, A14V100A Worst-Case Commercial Conditions, VCC = 4.75 V, T$_J$ = 70°C**

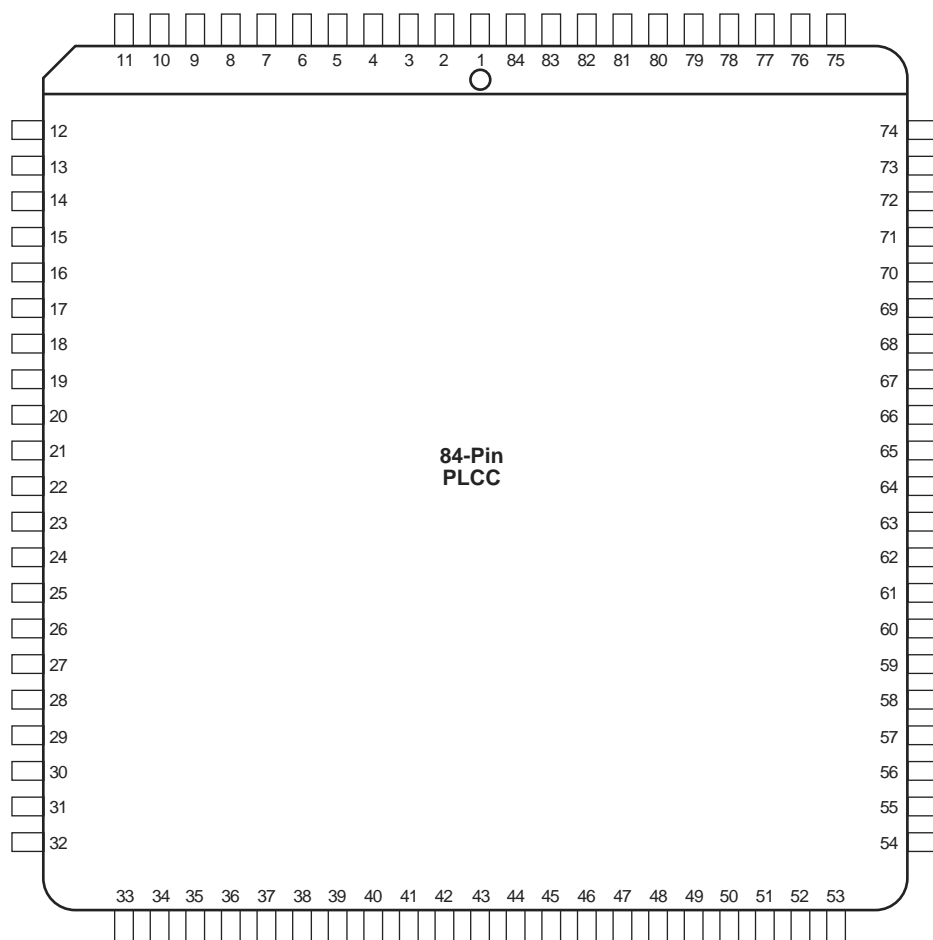| Dedicated (hardwired) I/O Clock Network | | –3 Speed[1] | | –2 Speed[1] | | –1 Speed | | Std. Speed | | 3.3 V Speed[1] | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **Parameter/Description** | | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | |
| t$_{IOCKH}$ | Input Low to High (pad to I/O module input) | | 2.3 | | 2.6 | | 3.0 | | 3.5 | | 4.5 | ns |
| t$_{IOPWH}$ | Minimum Pulse Width High | 2.4 | | 3.3 | | 3.8 | | 4.8 | | 6.5 | | ns |
| t$_{IPOWL}$ | Minimum Pulse Width Low | 2.4 | | 3.3 | | 3.8 | | 4.8 | | 6.5 | | ns |
| t$_{IOSAPW}$ | Minimum Asynchronous Pulse Width | 2.4 | | 3.3 | | 3.8 | | 4.8 | | 6.5 | | ns |
| t$_{IOCKSW}$ | Maximum Skew | | 0.6 | | 0.6 | | 0.7 | | 0.8 | | 0.6 | ns |
| t$_{IOP}$ | Minimum Period | 5.0 | | 6.8 | | 8.0 | | 10.0 | | 13.4 | | ns |
| f$_{IOMAX}$ | Maximum Frequency | | 200 | | 150 | | 125 | | 100 | | 75 | MHz |
| **Dedicated (hardwired) Array Clock** | | | | | | | | | | | | |
| t$_{HCKH}$ | Input Low to High (pad to S-module input) | | 3.7 | | 4.1 | | 4.7 | | 5.5 | | 7.0 | ns |
| t$_{HCKL}$ | Input High to Low (pad to S-module input) | | 3.7 | | 4.1 | | 4.7 | | 5.5 | | 7.0 | ns |
| t$_{HPWH}$ | Minimum Pulse Width High | 2.4 | | 3.3 | | 3.8 | | 4.8 | | 6.5 | | ns |
| t$_{HPWL}$ | Minimum Pulse Width Low | 2.4 | | 3.3 | | 3.8 | | 4.8 | | 6.5 | | ns |
| t$_{HCKSW}$ | Delta High to Low, Low Slew | | 0.6 | | 0.6 | | 0.7 | | 0.8 | | 0.6 | ns |
| t$_{HP}$ | Minimum Period | 5.0 | | 6.8 | | 8.0 | | 10.0 | | 13.4 | | ns |
| f$_{HMAX}$ | Maximum Frequency | | 200 | | 150 | | 125 | | 100 | | 75 | MHz |
| **Routed Array Clock Networks** | | | | | | | | | | | | |
| t$_{RCKH}$ | Input Low to High (FO = 64) | | 6.0 | | 6.8 | | 7.7 | | 9.0 | | 11.8 | ns |
| t$_{RCKL}$ | Input High to Low (FO = 64) | | 6.0 | | 6.8 | | 7.7 | | 9.0 | | 11.8 | ns |
| t$_{RPWH}$ | Min. Pulse Width High (FO = 64) | 4.1 | | 4.5 | | 5.4 | | 6.1 | | 8.2 | | ns |
| t$_{RPWL}$ | Min. Pulse Width Low (FO = 64) | 4.1 | | 4.5 | | 5.4 | | 6.1 | | 8.2 | | ns |
| t$_{RCKSW}$ | Maximum Skew (FO = 128) | | 1.2 | | 1.4 | | 1.6 | | 1.8 | | 1.8 | ns |
| t$_{RP}$ | Minimum Period (FO = 64) | 8.3 | | 9.3 | | 11.1 | | 12.5 | | 16.7 | | Units |
| f$_{RMAX}$ | Maximum Frequency (FO = 64) | | 120 | | 105 | | 90 | | 80 | | 60 | MHz |
| **Clock-to-Clock Skews** | | | | | | | | | | | | |
| t$_{IOHCKSW}$ | I/O Clock to H-Clock Skew | 0.0 | 2.6 | 0.0 | 2.7 | 0.0 | 2.9 | 0.0 | 3.0 | 0.0 | 3.0 | ns |
| t$_{IORCKSW}$ | I/O Clock to R-Clock Skew (FO = 64) (FO = 350) | 0.0 0.0 | 1.7 5.0 | 0.0 0.0 | 1.7 5.0 | 0.0 0.0 | 1.7 5.0 | 0.0 0.0 | 1.7 5.0 | 0.0 0.0 | 5.0 5.0 | ns |
| t$_{HRCKSW}$ | H-Clock to R-Clock Skew (FO = 64) (FO = 350) | 0.0 0.0 | 1.3 3.0 | 0.0 0.0 | 1.0 3.0 | 0.0 0.0 | 1.0 3.0 | 0.0 0.0 | 1.0 3.0 | 0.0 0.0 | 1.0 3.0 | ns |

*Notes:* *

1.  *The –2 and –3 speed grades have been discontinued. Refer to PDN 0104, PDN 0203, PDN 0604, and PDN 1004 at http://www.microsemi.com/soc/support/notifications/default.aspx#pdn.*

2.  *Delays based on 35 pF loading.*

# 3 – Package Pin Assignments

## PL84

```
                11  10  9  8  7  6  5  4  3  2  1  84 83 82 81 80 79 78 77 76 75

        12                                                                    74
        13                                                                    73
        14                                                                    72
        15                                                                    71
        16                                                                    70
        17                                                                    69
        18                                                                    68
        19                                                                    67
        20                                                                    66
        21                            84-Pin                                  65
        22                            PLCC                                    64
        23                                                                    63
        24                                                                    62
        25                                                                    61
        26                                                                    60
        27                                                                    59
        28                                                                    58
        29                                                                    57
        30                                                                    56
        31                                                                    55
        32                                                                    54

                33 34 35 36 37 38 39 40 41 42 43 44 45 46 47 48 49 50 51 52 53
```

*Note:    This is the top view of the package.*

## Note

For Package Manufacturing and Environmental information, visit the Resource Center at
http://www.microsemi.com/soc/products/solutions/package/docs.aspx.

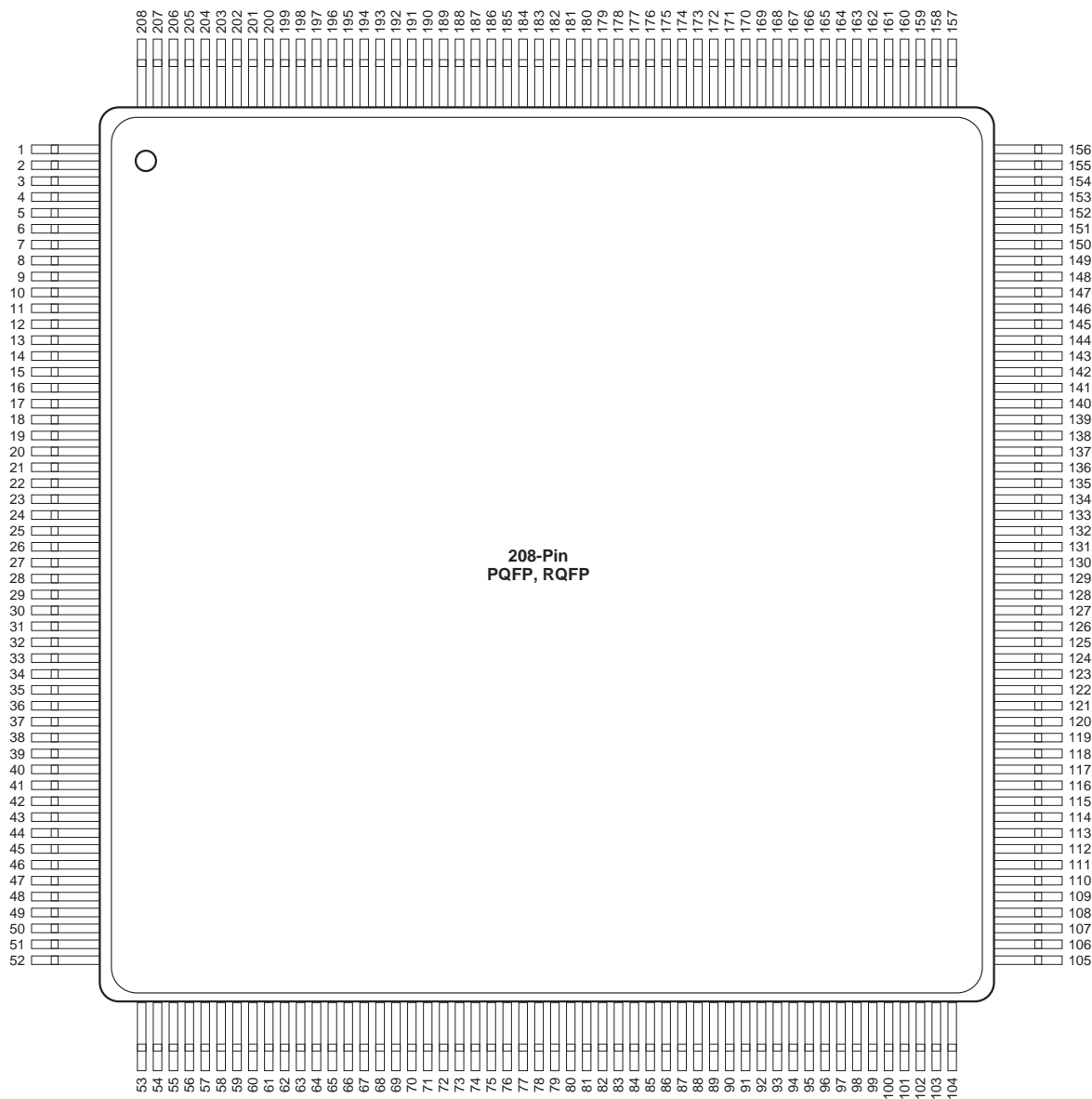| PL84 | | | |
|---|---|---|---|
| **Pin Number** | **A1415, A14V15 Function** | **A1425, A14V25 Function** | **A1440, A14V40 Function** |
| 1 | VCC | VCC | VCC |
| 2 | GND | GND | GND |
| 3 | VCC | VCC | VCC |
| 4 | PRA, I/O | PRA, I/O | PRA, I/O |
| 11 | DCLK, I/O | DCLK, I/O | DCLK, I/O |
| 12 | SDI, I/O | SDI, I/O | SDI, I/O |
| 16 | MODE | MODE | MODE |
| 27 | GND | GND | GND |
| 28 | VCC | VCC | VCC |
| 40 | PRB, I/O | PRB, I/O | PRB, I/O |
| 41 | VCC | VCC | VCC |
| 42 | GND | GND | GND |
| 43 | VCC | VCC | VCC |
| 45 | HCLK, I/O | HCLK, I/O | HCLK, I/O |
| 52 | SDO | SDO | SDO |
| 53 | IOPCL, I/O | IOPCL, I/O | IOPCL, I/O |
| 59 | VCC | VCC | VCC |
| 60 | VCC | VCC | VCC |
| 61 | GND | GND | GND |
| 68 | VCC | VCC | VCC |
| 69 | GND | GND | GND |
| 74 | IOCLK, I/O | IOCLK, I/O | IOCLK, I/O |
| 83 | CLKA, I/O | CLKA, I/O | CLKA, I/O |
| 84 | CLKB, I/O | CLKB, I/O | CLKB, I/O |

*Notes:*

1. All unlisted pin numbers are user I/Os.
2. NC denotes no connection.
3. MODE should be terminated to GND through a 10K resistor to enable Actionprobe usage; otherwise it can be terminated directly to GND.

| PQ100 | | |
|---|---|---|
| Pin Number | A1415 Function | A1425 Function |
| 2 | IOCLK, I/O | IOCLK, I/O |
| 14 | CLKA, I/O | CLKA, I/O |
| 15 | CLKB, I/O | CLKB, I/O |
| 16 | VCC | VCC |
| 17 | GND | GND |
| 18 | VCC | VCC |
| 19 | GND | GND |
| 20 | PRA, I/O | PRA, I/O |
| 27 | DCLK, I/O | DCLK, I/O |
| 28 | GND | GND |
| 29 | SDI, I/O | SDI, I/O |
| 34 | MODE | MODE |
| 35 | VCC | VCC |
| 36 | GND | GND |
| 47 | GND | GND |
| 48 | VCC | VCC |
| 61 | PRB, I/O | PRB, I/O |
| 62 | GND | GND |
| 63 | VCC | VCC |
| 64 | GND | GND |
| 65 | VCC | VCC |
| 67 | HCLK, I/O | HCLK, I/O |
| 77 | SDO | SDO |
| 78 | IOPCL, I/O | IOPCL, I/O |
| 79 | GND | GND |
| 85 | VCC | VCC |
| 86 | VCC | VCC |
| 87 | GND | GND |
| 96 | VCC | VCC |
| 97 | GND | GND |

*Notes:*

1. All unlisted pin numbers are user I/Os.
2. NC denotes no connection.
3. MODE should be terminated to GND through a 10K resistor to enable Actionprobe usage; otherwise it can be terminated directly to GND.
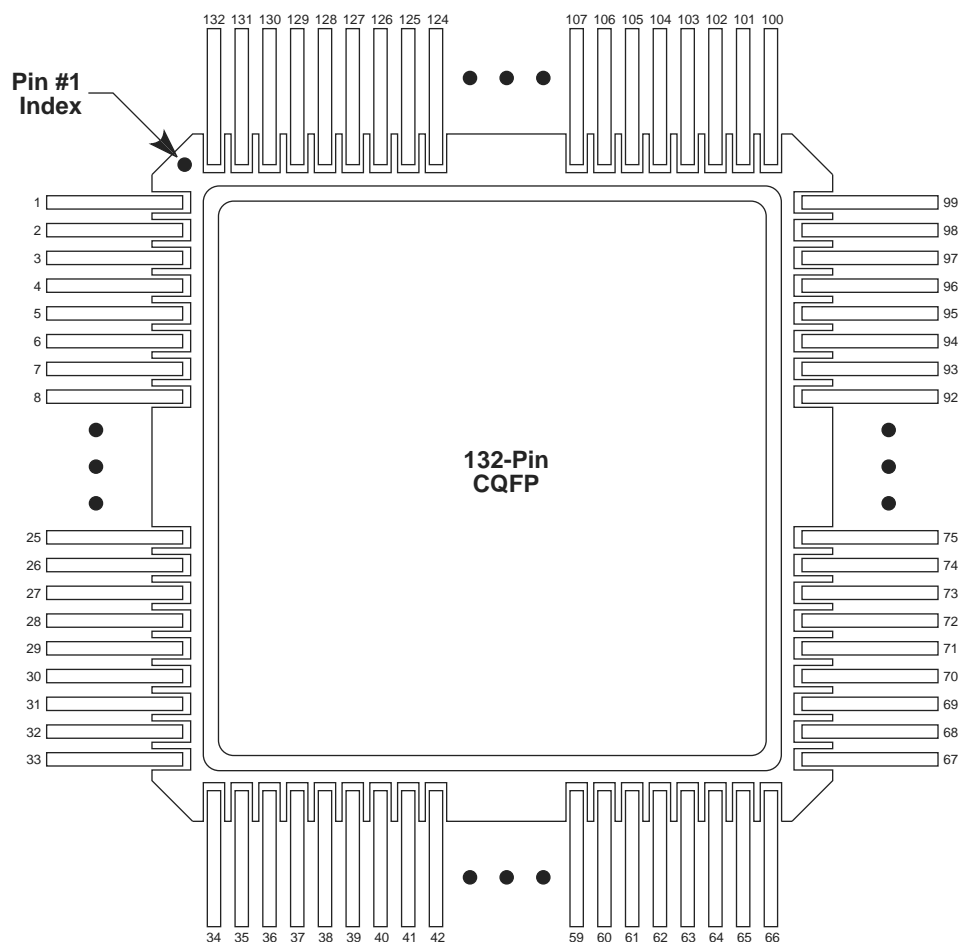
# PQ208, RQ208

**208-Pin
PQFP, RQFP**

*Note:   This is the top view of the package*

## Note

For Package Manufacturing and Environmental information, visit the Resource Center at
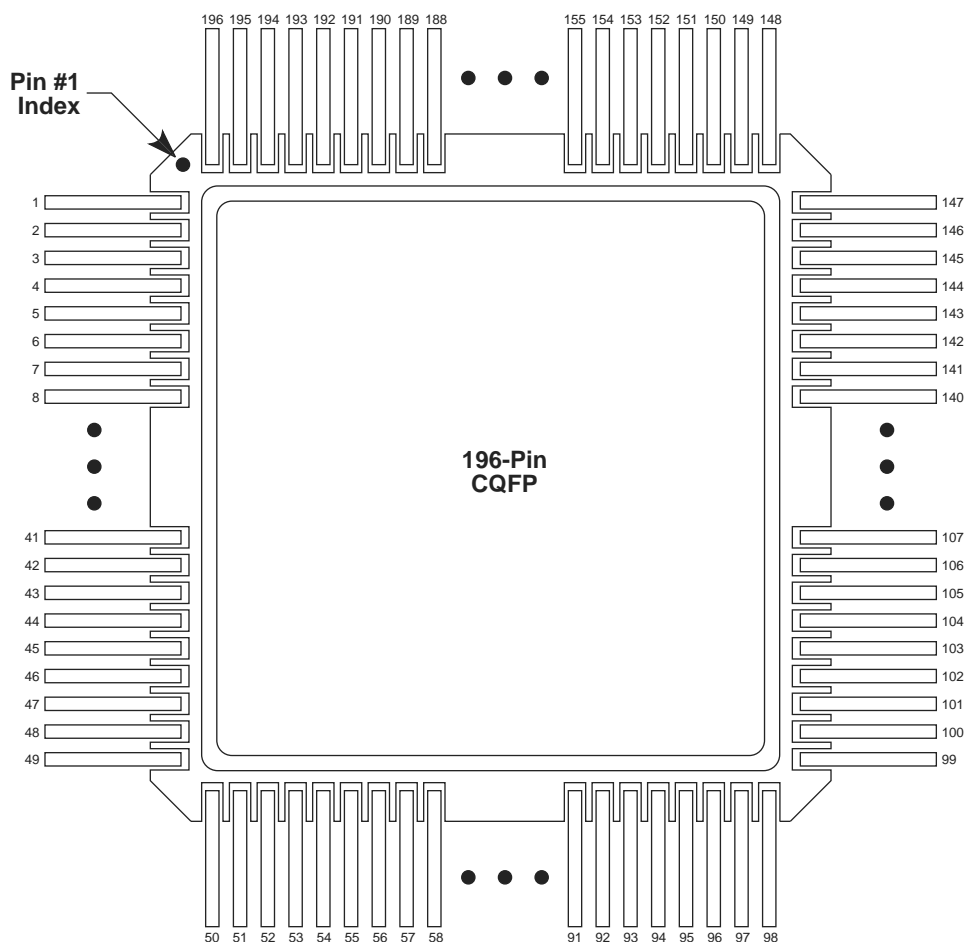http://www.microsemi.com/soc/products/solutions/package/docs.aspx

# CQ132



*Note: This is the top view*

## Note

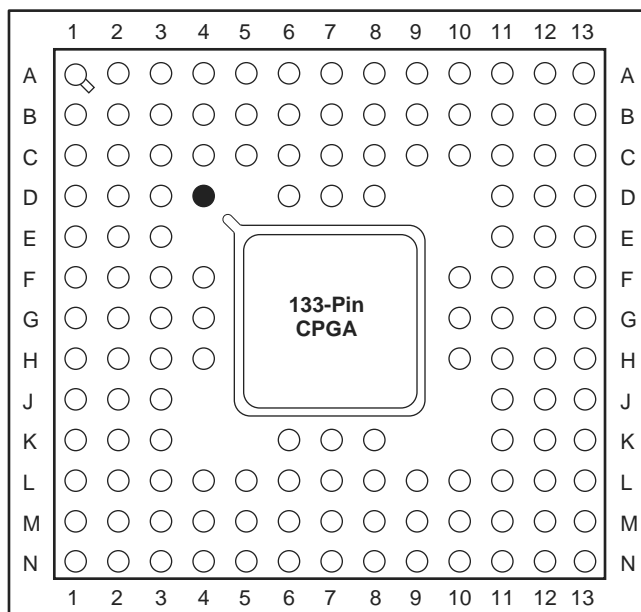For Package Manufacturing and Environmental information, visit the Resource Center at
http://www.microsemi.com/soc/products/solutions/package/docs.aspx

**Microsemi.**

# CQ196



*Note:   This is the top view.*

## Note

For Package Manufacturing and Environmental information, visit the Resource Center at
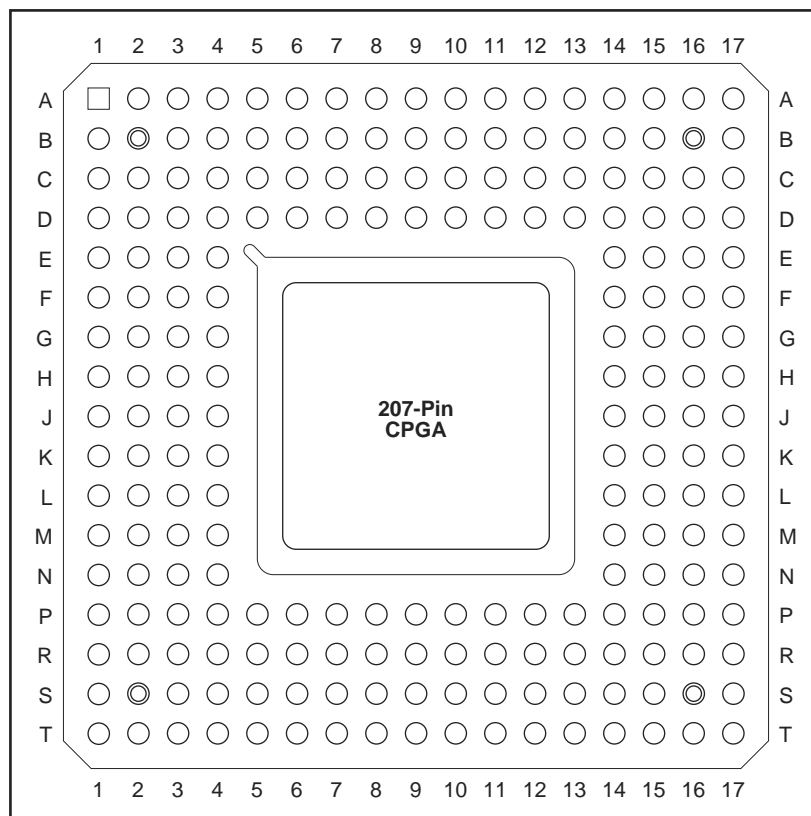http://www.microsemi.com/soc/products/solutions/package/docs.aspx

# PG133



*Note:   This is the top view.*

## Note

For Package Manufacturing and Environmental information, visit the Resource Center at
http://www.microsemi.com/soc/products/solutions/package/docs.aspx

# PG207



*Note:   This is the top view.*

## Note

For Package Manufacturing and Environmental information, visit the Resource Center at
http://www.microsemi.com/soc/products/solutions/package/docs.aspx

| PG207 | |
|---|---|
| **A1460 Function** | **Location** |
| CLKA or I/O | K1 |
| CLKB or I/O | J3 |
| DCLK or I/O | E4 |
| GND | C14, D4, D5, D9, D14, J4, J14, P3, P4, P7, P9, P14, R15 |
| HCLK or I/O | J15 |
| IOCLK or I/O | P5 |
| IOPCL or I/O | N14 |
| MODE | D7 |
| NC | A1, A2, A16, A17, B1, B17, C1, C2, S1, S3, S17, T1, T2, T16, T17 |
| PRA or I/O | H1 |
| PRB or I/O | K16 |
| SDI or I/O | C3 |
| SDO | P15 |
| VCC | B2, B9, B16, D11, J2, J16, P12, S2, S9, S16, T5 |

*Notes:*

1. All unlisted pin numbers are user I/Os.
2. NC denotes no connection.
3. MODE should be terminated to GND through a 10K resistor to enable Actionprobe usage; otherwise it can be terminated directly to GND.

| Revision | Changes | Page |
|---|---|---|
| Revision 2 (continued) | In the "Package Pin Assignments" section, notes were added to the pin tables for the following packages, stating that they are discontinued:<br>"BG225"<br>"PG100"<br>"PG133"<br>"PG175" | <br><br>3-20<br>3-24<br>3-26<br>3-28 |
| Revision 1 (June 2006) | RoHS compliant information was added to the "Ordering Information" section. | II |