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#### Understanding <u>Embedded - FPGAs (Field</u> <u>Programmable Gate Array)</u>

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

#### **Applications of Embedded - FPGAs**

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

#### Details

Details	
Product Status	Obsolete
Number of LABs/CLBs	848
Number of Logic Elements/Cells	-
Total RAM Bits	-
Number of I/O	168
Number of Gates	6000
Voltage - Supply	4.5V ~ 5.5V
Mounting Type	Surface Mount
Operating Temperature	-55°C ~ 125°C (TJ)
Package / Case	196-BCQFP with Tie Bar
Supplier Device Package	196-CQFP (63.5x63.5)
Purchase URL	https://www.e-xfl.com/product-detail/microsemi/a1460a-cq196b

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

The S-module contains a full implementation of the C-module plus a clearable sequential element that can either implement a latch or flip-flop function. The S-module can therefore implement any function implemented by the C-module. This allows complex combinatorial-sequential functions to be implemented with no delay penalty. The Designer Series Development System will automatically combine any C-module macro driving an S-module macro into the S-module, thereby freeing up a logic module and eliminating a module delay.

The clear input CLR is accessible from the routing channel. In addition, the clock input may be connected to one of three clock networks: CLKA, CLKB, or HCLK. The C-module and S-module functional descriptions are shown in Figure 2-2 and Figure 2-3 on page 2-2. The clock selection is determined by a multiplexer select at the clock input to the S-module.

## I/Os

## I/O Modules

I/O modules provide an interface between the array and the I/O Pad Drivers. I/O modules are located in the array and access the routing channels in a similar fashion to logic modules. The I/O module schematic is shown in Figure 4. The signals DataIn and DataOut connect to the I/O pad driver.



#### *Figure 2-4* • Functional Diagram for I/O Module

Each I/O module contains two D-type flip-flops. Each flip-flop is connected to the dedicated I/O clock (IOCLK). Each flip-flop can be bypassed by nonsequential I/Os. In addition, each flip-flop contains a data enable input that can be accessed from the routing channels (ODE and IDE). The asynchronous preset/clear input is driven by the dedicated preset/clear network (IOPCL). Either preset or clear can be selected individually on an I/O module by I/O module basis.



## 3.3 V Operating Conditions

Table 2-3 • Apsolute Maximum Ratings , Free Air Temperature Rang	Table 2-5 •	Absolute Maximum	Ratings <sup>1</sup> . Free Air	r Temperature Range
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Symbol	Parameter	Limits	Units
VCC	DC supply voltage	-0.5 to +7.0	V
VI	Input voltage	-0.5 to VCC + 0.5	V
VO	Output voltage	-0.5 to VCC + 0.5	V
IIO	I/O source sink current <sup>2</sup>	±20	mA
T <sub>STG</sub>	Storage temperature	-65 to +150	°C

Notes:

1. Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum rated conditions for extended periods may affect device reliability. Device should not be operated outside the recommended operating conditions.

2. Device inputs are normally high impedance and draw extremely low current. However, when input voltage is greater than VCC + 0.5 V for less than GND –0.5 V, the internal protection diodes will forward bias and can draw excessive current.

Table 2-6 • Recommended Operating Conditions

Parameter	Commercial	Units
Temperature range*	0 to +70	°C
Power supply tolerance	3.0 to 3.6	V

Note: \*Ambient temperature  $(T_A)$  is used for commercial.

Table 2-7 • Elec	ctrical Sr	oecifications
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		C	Commercial				
Parameter		Min.	Max.	Units			
VOH <sup>1</sup>	IOH = -4 mA	2.15	_	V			
	IOH = -3.2 mA	2.4		V			
VOL <sup>1</sup>	IOL = 6 mA		0.4	V			
VIL		-0.3	0.8	V			
VIH		2.0	VCC + 0.3	V			
Input transition time t <sub>R</sub> , t <sub>F</sub> <sup>2</sup>	VI = VCC or GND	-10	+10	μA			
C <sub>IO</sub> I/O Capacitance <sup>2,3</sup>			10	pF			
Standby current, ICC <sup>4</sup> (typical = 0	).3 mA)		0.75	mA			
Leakage current <sup>5</sup>		-10	10	μA			

1. Only one output tested at a time. VCC = minimum.

2. Not tested; for information only.

3. Includes worst-case 84-pin PLCC package capacitance. VOUT = 0 V, f - 1 MHz.

4. Typical standby current = 0.3 mA. All outputs unloaded. All inputs = VCC or GND.

5. VO, VIN = VCC or GND

## **Determining Average Switching Frequency**

To determine the switching frequency for a design, you must have a detailed understanding of the data input values to the circuit. The following guidelines are meant to represent worst-case scenarios so that they can be generally used to predict the upper limits of power dissipation. These guidelines are as follows:

Tahle	2-13	Guidelines	for	Predicting	Power	Dissination
lable	2-13	Ouldennes	101	rieuleung	I OWEI	Dissipation

Data	Value
Logic Modules (m)	80% of modules
Inputs switching (n)	# inputs/4
Outputs switching (p)	# output/4
First routed array clock loads (q1)	40% of sequential modules
Second routed array clock loads (q2)	40% of sequential modules
Load capacitance (CL)	35 pF
Average logic module switching rate (fm)	F/10
Average input switching rate (fn)	F/5
Average output switching rate (fp)	F/10
Average first routed array clock rate (fq1)	F/2
Average second routed array clock rate (fq2)	F/2
Average dedicated array clock rate (fs1)	F
Average dedicated I/O clock rate (fs2)	F

## **Timing Derating**

ACT 3 devices are manufactured in a CMOS process. Therefore, device performance varies according to temperature, voltage, and process variations. Minimum timing parameters reflect maximum operating voltage, minimum operating temperature, and best-case processing. Maximum timing parameters reflect minimum operating voltage, maximum operating temperature, and worst-case processing.

#### Table 2-15 • Timing Derating Factor (Temperature and Voltage)

(Commercial Minimum/Maximum Specification) x	Indus	strial	Military		
	Min.	Max.	Min.	Max.	
	0.66	1.07	0.63	1.17	

#### Table 2-16 • Timing Derating Factor for Designs at Typical Temperature ( $T_J = 25^{\circ}C$ ) and Voltage (5.0 V)

(Commercial Maximum Specification) x	0.85

#### Table 2-17 • Temperature and Voltage Derating Factors

(normalized to Worst-Case Commercial, TJ = 4.75 V, 70°C)

	-55	-40	0	25	70	85	125
4.50	0.72	0.76	0.85	0.90	1.04	1.07	1.117
4.75	0.70	0.73	0.82	0.87	1.00	1.03	1.12
5.00	0.68	0.71	0.79	0.84	0.97	1.00	1.09
5.25	0.66	0.69	0.77	0.82	0.94	0.97	1.06
5.50	0.63	0.66	0.74	0.79	0.90	0.93	1.01



Note: This derating factor applies to all routing and propagation delays.





### A1415A, A14V15A Timing Characteristics

Table 2-18 • A1415A, A14V15A Worst-Case Commercial Conditions, VCC = 4.75 V, T<sub>J</sub> = 70°C<sup>1</sup>

Logic Module Propagation Delays <sup>2</sup>		–3 Speed <sup>3</sup> –2 Spe		beed <sup>3</sup>	<sup>3</sup> −1 Speed		Std. Speed		3.3 V Speed <sup>1</sup>		Units	
Parame	eter/Description	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t <sub>PD</sub>	Internal Array Module		2.0		2.3		2.6		3.0		3.9	ns
t <sub>CO</sub>	Sequential Clock to Q		2.0		2.3		2.6		3.0		3.9	ns
t <sub>CLR</sub>	Asynchronous Clear to Q		2.0		2.3		2.6		3.0		3.9	ns
Predict	ed Routing Delays <sup>4</sup>			-								
t <sub>RD1</sub>	FO = 1 Routing Delay		0.9		1.0		1.1		1.3		1.7	ns
t <sub>RD2</sub>	FO = 2 Routing Delay		1.2		1.4		1.6		1.8		2.4	ns
t <sub>RD3</sub>	FO = 3 Routing Delay		1.4		1.6		1.8		2.1		2.8	ns
t <sub>RD4</sub>	FO = 4 Routing Delay		1.7		1.9		2.2		2.5		3.3	ns
t <sub>RD8</sub>	FO = 8 Routing Delay		2.8		3.2		3.6		4.2		5.5	ns
Logic N	Iodule Sequential Timing			-			-		-	-		-
t <sub>SUD</sub>	Flip-Flop Data Input Setup	0.5		0.6		0.7		0.8		0.8		ns
t <sub>HD</sub>	Flip-Flop Data Input Hold	0.0		0.0		0.0		0.0		0.0		ns
t <sub>SUD</sub>	Latch Data Input Setup	0.5		0.6		0.7		0.8		0.8		ns
t <sub>HD</sub>	Latch Data Input Hold	0.0		0.0		0.0		0.0		0.0		ns
t <sub>WASYN</sub>	Asynchronous Pulse Width	1.9		2.4		3.2		3.8		4.8		ns
t <sub>WCLKA</sub>	Flip-Flop Clock Pulse Width	1.9		2.4		3.2		3.8		4.8		ns
t <sub>A</sub>	Flip-Flop Clock Input Period	4.0		5.0		6.8		8.0		10.0		ns
f <sub>MAX</sub>	Flip-Flop Clock Frequency		250		200		150		125		100	MHz

Notes:

1. VCC = 3.0 V for 3.3 V specifications.

2. For dual-module macros, use  $t_{PD} + t_{RD1} + t_{PDn} + t_{CO} + t_{RD1} + t_{PDn}$  or  $t_{PD1} + t_{RD1} + t_{SUD}$ , whichever is appropriate.

3. The –2 and –3 speed grades have been discontinued. Please refer to the Product Discontinuation Notices (PDNs) listed below:

PDN March 2001 PDN 0104 PDN 0203 PDN 0604 PDN 1004

4. Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual worst-case performance. Post-route timing is based on actual routing delay measurements performed on the device prior to shipment.

## A1415A, A14V15A Timing Characteristics (continued)

### *Table 2-21* • A1415A, A14V15A Worst-Case Commercial Conditions, VCC = 4.75 V, T<sub>J</sub> = 70°C

Dedicate	d (hardwired) I/O Clock Network	-3 Speed		-2 Speed		-1 Speed		Std. Speed		3.3 V Speed <sup>1</sup>		Units
Paramete	er/Description	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t <sub>IOCKH</sub>	Input Low to High (pad to I/O module input)		2.0		2.3		2.6		3.0		3.5	ns
t <sub>IOPWH</sub>	Minimum Pulse Width High	1.9		2.4		3.3		3.8		4.8		ns
t <sub>IPOWL</sub>	Minimum Pulse Width Low	1.9		2.4		3.3		3.8		4.8		ns
t <sub>IOSAPW</sub>	Minimum Asynchronous Pulse Width	1.9		2.4		3.3		3.8		4.8		ns
t <sub>IOCKSW</sub>	Maximum Skew		0.4		0.4		0.4		0.4		0.4	ns
t <sub>IOP</sub>	Minimum Period	4.0		5.0		6.8		8.0		10.0		ns
f <sub>IOMAX</sub>	Maximum Frequency		250		200		150		125		100	MHz
Dedicate	d (hardwired) Array Clock			•			•					
<sup>t</sup> нскн	Input Low to High (pad to S-module input)		3.0		3.4		3.9		4.5		5.5	ns
t <sub>HCKL</sub>	Input High to Low (pad to S-module input)		3.0		3.4		3.9		4.5		5.5	ns
t <sub>HPWH</sub>	Minimum Pulse Width High	1.9		2.4		3.3		3.8		4.8		ns
t <sub>HPWL</sub>	Minimum Pulse Width Low	1.9		2.4		3.3		3.8		4.8		ns
t <sub>HCKSW</sub>	Delta High to Low, Low Slew		0.3		0.3		0.3		0.3		0.3	ns
t <sub>HP</sub>	Minimum Period	4.0		5.0		6.8		8.0		10.0		ns
f <sub>HMAX</sub>	Maximum Frequency		250		200		150		125		100	MHz
Routed A	rray Clock Networks			-								
t <sub>RCKH</sub>	Input Low to High (FO = 64)		3.7		4.1		4.7		5.5		9.0	ns
t <sub>RCKL</sub>	Input High to Low (FO = 64)		4.0		4.5		5.1		6.0		9.0	ns
t <sub>RPWH</sub>	Min. Pulse Width High (FO = 64)	3.3		3.8		4.2		4.9		6.5		ns
t <sub>RPWL</sub>	Min. Pulse Width Low (FO = 64)	3.3		3.8		4.2		4.9		6.5		ns
t <sub>RCKSW</sub>	Maximum Skew (FO = 128)		0.7		0.8		0.9		1.0		1.0	ns
t <sub>RP</sub>	Minimum Period (FO = 64)	6.8		8.0		8.7		10.0		13.4		ns
f <sub>RMAX</sub>	Maximum Frequency (FO = 64)		150		125		115		100		75	MHz
Clock-to-	Clock Skews											
t <sub>IOHCKSW</sub>	I/O Clock to H-Clock Skew	0.0	1.7	0.0	1.8	0.0	2.0	0.0	2.2	0.0	3.0	ns
t <sub>IORCKS</sub> W	I/O Clock to R-Clock Skew (FO = 64)	0.0	1.0	0.0	1.0	0.0	1.0	0.0	1.0	0.0	3.0	ns
t <sub>HRCKSW</sub>	H-Clock to R-Clock Skew (FO = 64) (FO = 50% maximum)	0.0	1.0	0.0	1.0	0.0	1.0	0.0	1.0	0.0 0.0	3.0 3.0	ns

Notes:

1. Delays based on 35 pF loading.

2. The –2 and –3 speed grades have been discontinued. Refer to PDN 0104, PDN 0203, PDN 0604, and PDN 1004 at http://www.microsemi.com/soc/support/notifications/default.aspx#pdn.



## A1460A, A14V60A Timing Characteristics (continued)

Table 2-32 • A1460A, A14V60A Worst-Case Commercial Conditions, VCC = 4.75 V, T<sub>J</sub> = 70°C

I/O Mod	dule – TTL Output Timing <sup>1</sup>	-3 Sp	beed <sup>2</sup>	-2 S	beed <sup>2</sup>	–1 S	peed	Std.	Speed	3.3 V	Speed <sup>1</sup>	Units
Parame	eter/Description	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t <sub>DHS</sub>	Data to Pad, High Slew		5.0		5.6		6.4		7.5		9.8	ns
t <sub>DLS</sub>	Data to Pad, Low Slew		8.0		9.0		10.2		12.0		15.6	ns
t <sub>ENZHS</sub>	Enable to Pad, Z to H/L, High Slew		4.0		4.5		5.1		6.0		7.8	ns
t <sub>ENZLS</sub>	Enable to Pad, Z to H/L, Low Slew		7.4		8.3		9.4		11.0		14.3	ns
t <sub>ENHSZ</sub>	Enable to Pad, H/L to Z, High Slew		7.8		8.7		9.9		11.6		15.1	ns
t <sub>ENLSZ</sub>	Enable to Pad, H/L to Z, Low Slew		7.4		8.3		9.4		11.0		14.3	ns
t <sub>CKHS</sub>	IOCLK Pad to Pad H/L, High Slew		9.0		9.0		10.0		11.5		15.0	ns
t <sub>CKLS</sub>	IOCLK Pad to Pad H/L, Low Slew		12.8		12.8		15.3		17.0		22.1	ns
d <sub>TLHHS</sub>	Delta Low to High, High Slew		0.02		0.02		0.03		0.03		0.04	ns/pF
d <sub>TLHLS</sub>	Delta Low to High, Low Slew		0.05		0.05		0.06		0.07		0.09	ns/pF
d <sub>THLHS</sub>	Delta High to Low, High Slew		0.04		0.04		0.04		0.05		0.07	ns/pF
d <sub>THLLS</sub>	Delta High to Low, Low Slew		0.05		0.05		0.06		0.07		0.09	ns/pF
I/O Mod	dule – CMOS Output Timing <sup>1</sup>											
t <sub>DHS</sub>	Data to Pad, High Slew		6.2		7.0		7.9		9.3		12.1	ns
t <sub>DLS</sub>	Data to Pad, Low Slew		11.7		13.1		14.9		17.5		22.8	ns
t <sub>ENZHS</sub>	Enable to Pad, Z to H/L, High Slew		5.2		5.9		6.6		7.8		10.1	ns
t <sub>ENZLS</sub>	Enable to Pad, Z to H/L, Low Slew		8.9		10.0		11.3		13.3		17.3	ns
t <sub>ENHSZ</sub>	Enable to Pad, H/L to Z, High Slew		7.4		8.3		9.4		11.0		14.3	ns
t <sub>ENLSZ</sub>	Enable to Pad, H/L to Z, Low Slew		7.4		8.3		9.4		11.0		14.3	ns
t <sub>CKHS</sub>	IOCLK Pad to Pad H/L, High Slew		10.4		10.4		12.1		13.8		17.9	ns
t <sub>CKLS</sub>	IOCLK Pad to Pad H/L, Low Slew		14.5		14.5		17.4		19.3		25.1	ns
d <sub>TLHHS</sub>	Delta Low to High, High Slew		0.04		0.04		0.05		0.06		0.08	ns/pF
d <sub>TLHLS</sub>	Delta Low to High, Low Slew		0.07		0.08		0.09		0.11		0.14	ns/pF
d <sub>THLHS</sub>	Delta High to Low, High Slew		0.03		0.03		0.03		0.04		0.05	ns/pF
d <sub>THLLS</sub>	Delta High to Low, Low Slew		0.04		0.04		0.04		0.05		0.07	ns/pF

Notes:

1. Delays based on 35 pF loading.

2. The –2 and –3 speed grades have been discontinued. Refer to PDN 0104, PDN 0203, PDN 0604, and PDN 1004 at http://www.microsemi.com/soc/support/notifications/default.aspx#pdn.



### A14100A, A14V100A Timing Characteristics

Logic N	Iodule Propagation Delays <sup>2</sup>	–3 S	peed <sup>3</sup>	-2 Sp	-2 Speed <sup>3</sup>		-1 Speed		speed	3.3 V Speed <sup>1</sup>		Units
Parame	eter/Description	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t <sub>PD</sub>	Internal Array Module		2.0		2.3		2.6		3.0		3.9	ns
t <sub>CO</sub>	Sequential Clock to Q		2.0		2.3		2.6		3.0		3.9	ns
t <sub>CLR</sub>	Asynchronous Clear to Q		2.0		2.3		2.6		3.0		3.9	ns
Predict	ed Routing Delays <sup>4</sup>			-								
t <sub>RD1</sub>	FO = 1 Routing Delay		0.9		1.0		1.1		1.3		1.7	ns
t <sub>RD2</sub>	FO = 2 Routing Delay		1.2		1.4		1.6		1.8		2.4	ns
t <sub>RD3</sub>	FO = 3 Routing Delay		1.4		1.6		1.8		2.1		2.8	ns
t <sub>RD4</sub>	FO = 4 Routing Delay		1.7		1.9		2.2		2.5		3.3	ns
t <sub>RD8</sub>	FO = 8 Routing Delay		2.8		3.2		3.6		4.2		5.5	ns
Logic N	Iodule Sequential Timing			-								
t <sub>SUD</sub>	Flip-Flop Data Input Setup	0.5		0.6		0.8		0.8		0.8		ns
t <sub>HD</sub>	Flip-Flop Data Input Hold	0.0		0.0		0.5		0.5		0.5		ns
t <sub>SUD</sub>	Latch Data Input Setup	0.5		0.6		0.8		0.8		0.8		ns
t <sub>HD</sub>	Latch Data Input Hold	0.0		0.0		0.5		0.5		0.5		ns
t <sub>WASYN</sub>	Asynchronous Pulse Width	2.4		3.2		3.8		4.8		6.5		ns
t <sub>WCLKA</sub>	Flip-Flop Clock Pulse Width	2.4		3.2		3.8		4.8		6.5		ns
t <sub>A</sub>	Flip-Flop Clock Input Period	5.0		6.8		8.0		10.0		13.4		ns
f <sub>MAX</sub>	Flip-Flop Clock Frequency		200		150		125		100		75	MHz

Notes:

1. VCC = 3.0 V for 3.3 V specifications.

2. For dual-module macros, use  $t_{PD} + t_{RD1} + t_{PDn} + t_{CO} + t_{RD1} + t_{PDn}$  or  $t_{PD1} + t_{RD1} + t_{SUD}$ , whichever is appropriate.

3. The –2 and –3 speed grades have been discontinued. Refer to PDN 0104, PDN 0203, PDN 0604, and PDN 1004 at http://www.microsemi.com/soc/support/notifications/default.aspx#pdn.

4. Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual worst-case performance. Post-route timing is based on actual routing delay measurements performed on the device prior to shipment.

### A14100A, A14V100A Timing Characteristics (continued)

Table 2-37 • A14100A	, A14V100A Worst-Case	Commercial Conditions,	$VCC = 4.75 V, T_{J} = 70^{\circ}C$
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Dedicate	Dedicated (hardwired) I/O Clock Network		-3 Speed <sup>1</sup>		–2 Speed <sup>1</sup>		-1 Speed		Std. Speed		3.3 V Speed <sup>1</sup>	
Paramete	er/Description	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t <sub>IOCKH</sub>	Input Low to High (pad to I/O module input)		2.3		2.6		3.0		3.5		4.5	ns
t <sub>IOPWH</sub>	Minimum Pulse Width High	2.4		3.3		3.8		4.8		6.5		ns
t <sub>IPOWL</sub>	Minimum Pulse Width Low	2.4		3.3		3.8		4.8		6.5		ns
t <sub>IOSAPW</sub>	Minimum Asynchronous Pulse Width	2.4		3.3		3.8		4.8		6.5		ns
t <sub>IOCKSW</sub>	Maximum Skew		0.6		0.6		0.7		0.8		0.6	ns
t <sub>IOP</sub>	Minimum Period	5.0		6.8		8.0		10.0		13.4		ns
f <sub>IOMAX</sub>	Maximum Frequency		200		150		125		100		75	MHz
Dedicate	d (hardwired) Array Clock			-								
t <sub>нскн</sub>	Input Low to High (pad to S-module input)		3.7		4.1		4.7		5.5		7.0	ns
t <sub>HCKL</sub>	Input High to Low (pad to S-module input)		3.7		4.1		4.7		5.5		7.0	ns
t <sub>HPWH</sub>	Minimum Pulse Width High	2.4		3.3		3.8		4.8		6.5		ns
t <sub>HPWL</sub>	Minimum Pulse Width Low	2.4		3.3		3.8		4.8		6.5		ns
t <sub>HCKSW</sub>	Delta High to Low, Low Slew		0.6		0.6		0.7		0.8		0.6	ns
t <sub>HP</sub>	Minimum Period	5.0		6.8		8.0		10.0		13.4		ns
f <sub>HMAX</sub>	Maximum Frequency		200		150		125		100		75	MHz
Routed A	rray Clock Networks			-								
t <sub>RCKH</sub>	Input Low to High (FO = 64)		6.0		6.8		7.7		9.0		11.8	ns
t <sub>RCKL</sub>	Input High to Low (FO = 64)		6.0		6.8		7.7		9.0		11.8	ns
t <sub>RPWH</sub>	Min. Pulse Width High (FO = 64)	4.1		4.5		5.4		6.1		8.2		ns
t <sub>RPWL</sub>	Min. Pulse Width Low (FO = 64)	4.1		4.5		5.4		6.1		8.2		ns
t <sub>RCKSW</sub>	Maximum Skew (FO = 128)		1.2		1.4		1.6		1.8		1.8	ns
t <sub>RP</sub>	Minimum Period (FO = 64)	8.3		9.3		11.1		12.5		16.7		ns
f <sub>RMAX</sub>	Maximum Frequency (FO = 64)		120		105		90		80		60	MHz
Clock-to-Clock Skews												
t <sub>IOHCKSW</sub>	I/O Clock to H-Clock Skew	0.0	2.6	0.0	2.7	0.0	2.9	0.0	3.0	0.0	3.0	ns
t <sub>IORCKSW</sub>	I/O Clock to R-Clock Skew (FO = 64) (FO = 350)	0.0 0.0	1.7 5.0	0.0 0.0	1.7 5.0	0.0 0.0	1.7 5.0	0.0 0.0	1.7 5.0	0.0 0.0	5.0 5.0	ns
t <sub>HRCKSW</sub>	H-Clock to R-Clock Skew (FO = 64) (FO = 350)	0.0 0.0	1.3 3.0	0.0 0.0	1.0 3.0	0.0 0.0	1.0 3.0	0.0 0.0	1.0 3.0	0.0 0.0	1.0 3.0	ns

Notes: \*

1. The -2 and -3 speed grades have been discontinued. Refer to PDN 0104, PDN 0203, PDN 0604, and PDN 1004 at http://www.microsemi.com/soc/support/notifications/default.aspx#pdn.

2. Delays based on 35 pF loading.



## **Pin Descriptions**

#### CLKA Clock A (Input)

Clock input for clock distribution networks. The Clock input is buffered prior to clocking the logic modules. This pin can also be used as an I/O.

#### CLKB Clock B (Input)

Clock input for clock distribution networks. The Clock input is buffered prior to clocking the logic modules. This pin can also be used as an I/O.

#### GND Ground

LOW supply voltage.

#### HCLK Dedicated (Hard-wired) Array Clock (Input)

Clock input for sequential modules. This input is directly wired to each S-Module and offers clock speeds independent of the number of S-Modules being driven. This pin can also be used as an I/O.

#### I/O Input/Output (Input, Output)

The I/O pin functions as an input, output, three-state, or bidirectional buffer. Input and output levels are compatible with standard TTL and CMOS specifications. Unused I/O pins are tristated by the Designer Series software.

#### IOCLK Dedicated (Hard-wired) I/O Clock (Input)

Clock input for I/O modules. This input is directly wired to each I/O module and offers clock speeds independent of the number of I/O modules being driven. This pin can also be used as an I/O.

#### IOPCL Dedicated (Hard-wired) I/O Preset/Clear (Input)

Input for I/O preset or clear. This global input is directly wired to the preset and clear inputs of all I/O registers. This pin functions as an I/O when no I/O preset or clear macros are used.

#### MODE Mode (Input)

The MODE pin controls the use of diagnostic pins (DCLK, PRA, PRB, SDI). When the MODE pin is HIGH, the special functions are active. When the MODE pin is LOW, the pins function as I/Os. To provide Actionprobe capability, the MODE pin should be terminated to GND through a 10K resistor so that the MODE pin can be pulled high when required.

#### NC No Connection

This pin is not connected to circuitry within the device.

#### PRA Probe A (Output)

The Probe A pin is used to output data from any user-defined design node within the device. This independent diagnostic pin can be used in conjunction with the Probe B pin to allow real-time diagnostic output of any signal path within the device. The Probe A pin can be used as a user-defined I/O when debugging has been completed. The pin's probe capabilities can be permanently disabled to protect programmed design confidentiality. PRA is accessible when the MODE pin is HIGH. This pin functions as an I/O when the MODE pin is LOW.

#### PRB Probe B (Output)

The Probe B pin is used to output data from any user-defined design node within the device. This independent diagnostic pin can be used in conjunction with the Probe A pin to allow real-time diagnostic output of any signal path within the device. The Probe B pin can be used as a user-defined I/O when debugging has been completed. The pin's probe capabilities can be permanently disabled to protect programmed design confidentiality. PRB is accessible when the MODE pin is HIGH. This pin functions as an I/O when the MODE pin is LOW.

#### SDI Serial Data Input (Input)

Serial data input for diagnostic probe and device programming. SDI is active when the MODE pin is HIGH. This pin functions as an I/O when the MODE pin is LOW.

# 3 – Package Pin Assignments

## **PL84**



Note: This is the top view of the package.

### Note

For Package Manufacturing and Environmental information, visit the Resource Center at http://www.microsemi.com/soc/products/solutions/package/docs.aspx.

## PQ100



Note: This is the top view of the package.

### Note

For Package Manufacturing and Environmental information, visit the Resource Center at http://www.microsemi.com/soc/products/solutions/package/docs.aspx

Accelerator Series FPGAs – ACT 3 Family

	PQ208, RQ208	3	PQ208, RQ208					
Pin Number	A1460, A14V60 Function	A14100, A14V100 Function	Pin Number	A1460, A14V60 Function	A14100, A14V100 Function			
1	GND	GND	115	VCC	VCC			
2	SDI, I/O	SDI, I/O	116	NC	I/O			
11	MODE	MODE	129	GND	GND			
12	VCC	VCC	130	VCC	VCC			
25	VCC	VCC	131	GND	GND			
26	GND	GND	132	VCC	VCC			
27	VCC	VCC	145	VCC	VCC			
28	GND	GND	146	GND	GND			
40	VCC	VCC	147	NC	I/O			
41	VCC	VCC	148	VCC	VCC			
52	GND	GND	156	IOCLK, I/O	IOCLK, I/O			
53	NC	I/O	157	GND	GND			
60	VCC	VCC	158	NC	I/O			
65	NC	I/O	164	VCC	VCC			
76	PRB, I/O	PRB, I/O	180	CLKA, I/O	CLKA, I/O			
77	GND	GND	181	CLKB, I/O	CLKB, I/O			
78	VCC	VCC	182	VCC	VCC			
79	GND	GND	183	GND	GND			
80	VCC	VCC	184	VCC	VCC			
82	HCLK, I/O	HCLK, I/O	185	GND	GND			
98	VCC	VCC	186	PRA, I/O	PRA, I/O			
102	NC	I/O	195	NC	I/O			
103	SDO	SDO	201	VCC	VCC			
104	IOPCL, I/O	IOPCL, I/O	205	NC	I/O			
105	GND	GND	208	DCLK, I/O	DCLK, I/O			
114	VCC	VCC						

Notes:

1. All unlisted pin numbers are user I/Os.

2. NC denotes no connection.

3. MODE should be terminated to GND through a 10K resistor to enable Actionprobe usage; otherwise it can be terminated directly to GND.

Accelerator Series FPGAs – ACT 3 Family

	VQ100				
Pin Number	A1415, A14V15 Function	A1425, A14V25 Function	A1440, A14V40 Function		
1	GND	GND	GND		
2	SDI, I/O	SDI, I/O	SDI, I/O		
7	MODE	MODE	MODE		
8	VCC	VCC	VCC		
9	GND	GND	GND		
20	VCC	VCC	VCC		
21	NC	I/O	I/O		
34	PRB, I/O	PRB, I/O	PRB, I/O		
35	VCC	VCC	VCC		
36	GND	GND	GND		
37	VCC	VCC	VCC		
39	HCLK, I/O	HCLK, I/O	HCLK, I/O		
49	SDO	SDO	SDO		
50	IOPCL, I/O	IOPCL, I/O	IOPCL, I/O		
51	GND	GND	GND		
57	VCC	VCC	VCC		
58	VCC	VCC	VCC		
67	VCC	VCC	VCC		
68	GND	GND	GND		
69	GND	GND	GND		
74	NC	I/O	I/O		
75	IOCLK, I/O	IOCLK, I/O	IOCLK, I/O		
87	CLKA, I/O	CLKA, I/O	CLKA, I/O		
88	CLKB, I/O	CLKB, I/O	CLKB, I/O		
89	VCC	VCC	VCC		
90	VCC	VCC	VCC		
91	GND	GND	GND		
92	PRA, I/O	PRA, I/O	PRA, I/O		
93	NC	I/O	I/O		
100	DCLK, I/O	DCLK, I/O	DCLK, I/O		

- 1. All unlisted pin numbers are user I/Os.
- 2. NC denotes no connection.
- 3. MODE should be terminated to GND through a 10K resistor to enable Actionprobe usage; otherwise it can be terminated directly to GND.

Accelerator Series FPGAs - ACT 3 Family

	CQ196	] [	CQ196
Pin Number	A1460 Function	Pin Number	A1460 Function
1	GND	101	GND
2	SDI, I/O	110	VCC
11	MODE	111	VCC
12	VCC	112	GND
13	GND	137	VCC
37	GND	138	GND
38	VCC	139	GND
39	VCC	140	VCC
51	GND	148	IOCLK, I/O
52	GND	149	GND
59	VCC	155	VCC
64	GND	162	GND
77	HCLK, I/O	172	CLKA, I/O
79	PRB, I/O	173	CLKB, I/O
86	GND	174	PRA, I/O
94	VCC	183	GND
98	GND	189	VCC
99	SDO	193	GND
100	IOPCL, I/O	196	DCLK, I/O

- 1. All unlisted pin numbers are user I/Os.
- 2. NC denotes no connection.
- 3. MODE should be terminated to GND through a 10K resistor to enable Actionprobe usage; otherwise it can be terminated directly to GND.

Accelerator Series FPGAs - ACT 3 Family

	CQ256		CQ256
Pin Number	A14100 Function	Pin Number	A14100 Function
1	GND	141	VCC
2	SDI, I/O	158	GND
11	MODE	159	VCC
28	VCC	160	GND
29	GND	161	VCC
30	VCC	174	VCC
31	GND	175	GND
46	VCC	176	GND
59	GND	188	IOCLK, I/O
90	PRB, I/O	189	GND
91	GND	219	CLKA, I/O
92	VCC	220	CLKB, I/O
93	GND	221	VCC
94	VCC	222	GND
96	HCLK, I/O	223	VCC
110	GND	224	GND
126	SDO	225	PRA, I/O
127	IOPCL, I/O	240	GND
128	GND	256	DCLK, I/O

- 1. All unlisted pin numbers are user I/Os.
- 2. NC denotes no connection.
- 3. MODE should be terminated to GND through a 10K resistor to enable Actionprobe usage; otherwise it can be terminated directly to GND.



Package Pin Assignments

## PG100





#### Note

For Package Manufacturing and Environmental information, visit the Resource Center at http://www.microsemi.com/soc/products/solutions/package/docs.aspx



Package Pin Assignments

## PG133



Note: This is the top view.

#### Note

For Package Manufacturing and Environmental information, visit the Resource Center at http://www.microsemi.com/soc/products/solutions/package/docs.aspx

Accelerator Series FPGAs – ACT 3 Family

	PG133			
A1425 Function	Location			
CLKA or I/O	D7			
CLKB or I/O	B6			
DCLK or I/O	D4			
GND	A2, C3, C7, C11, C12, F10, G3, G11, L3, L7, L11, M3, N12			
HCLK or I/O	К7			
IOCLK or I/O	C10			
IOPCL or I/O	L10			
MODE	E3			
NC	A1, A7, A13, G1, G13, N1, N7, N13			
PRA or I/O	A6			
PRB or I/O	L6			
SDI or I/O	C2			
SDO	M11			
VCC	B2, B7, B12, E11, G2, G12, J2, J12, M2, M7, M12			

- 1. All unlisted pin numbers are user I/Os.
- 2. NC denotes no connection.
- 3. MODE should be terminated to GND through a 10K resistor to enable Actionprobe usage; otherwise it can be terminated directly to GND.
- 4. The PG133 package has been discontinued.

Accelerator Series FPGAs – ACT 3 Family

	PG175				
A1440 Function	Location				
CLKA or I/O	C9				
CLKB or I/O	A9				
DCLK or I/O	D5				
GND	D4, D8, D11, D12, E4, E14, H4, H12, L4, L12, M4, M8, M12				
HCLK or I/O	R8				
IOCLK or I/O	E12				
IOPCL or I/O	P13				
MODE	F3				
NC	A1, A2, A15, B2, B3, P2, P14, R1, R2, R14, R15				
PRA or I/O	B8				
PRB or I/O	R7				
SDI or I/O	D3				
SDO	N12				
VCC	C3, C8, C13, E15, H3, H13, L1, L14, N3, N8, N13				

- 1. All unlisted pin numbers are user I/Os.
- 2. NC denotes no connection.
- 3. MODE should be terminated to GND through a 10K resistor to enable Actionprobe usage; otherwise it can be terminated directly to GND.
- 4. The PG175 package has been discontinued.