Microsemi Corporation - A1460A-PQG160I Datasheet

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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications,

Details	
Product Status	Obsolete
Number of LABs/CLBs	848
Number of Logic Elements/Cells	-
Total RAM Bits	-
Number of I/O	131
Number of Gates	6000
Voltage - Supply	4.5V ~ 5.5V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 85°C (TA)
Package / Case	160-BQFP
Supplier Device Package	160-PQFP (28x28)
Purchase URL	https://www.e-xfl.com/product-detail/microsemi/a1460a-pqg160i

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

Product Plan

Device/Package	Speed Grade[1]				Application[1]			
	Std.	–1	–2	–3	C	I	M	B
A1415A Device								
84-Pin Plastic Leaded Chip Carrier (PLCC)	✓	✓	D	D	✓	✓	✓	–
100-Pin Plastic Quad Flatpack (PQFP)	✓	✓	D	D	✓	✓	✓	–
100-Pin Very Thin Quad Flatpack (VQFP)	✓	✓	D	D	✓	✓	✓	–
100-Pin Ceramic Pin Grid Array (CPGA)	D	D	D	D	D	–	–	–
A14V15A Device								
84-Pin Plastic Leaded Chip Carrier (PLCC)	✓	–	–	–	✓	–	–	–
100-Pin Very Thin Quad Flatpack (VQFP)	✓	–	–	–	✓	–	–	–
A1425A Device								
84-Pin Plastic Leaded Chip Carrier (PLCC)	✓	✓	D	D	✓	✓		
100-Pin Plastic Quad Flatpack (PQFP)	✓	✓	D	D	✓	✓	–	–
100-Pin Very Thin Quad Flatpack (VQFP)	✓	✓	D	D	✓	✓	–	–
132-Pin Ceramic Quad Flatpack (CQFP)	✓	✓	–	–	✓	–	✓	✓
133-Pin Ceramic Pin Grid Array (CPGA)	D	D	D	D	D	–	D	D
160-Pin Plastic Quad Flatpack (PQFP)	✓	✓	D	D	✓	✓	–	–
A14V25A Device								
84-Pin Plastic Leaded Chip Carrier (PLCC)	✓	–	–	–	✓	–	–	–
100-Pin Very Thin Quad Flatpack (VQFP)	✓	–	–	–	✓	–	–	–
160-Pin Plastic Quad Flatpack (PQFP)	✓	–	–	–	✓	–	–	–
A1440A Device								
84-Pin Plastic Leaded Chip Carrier (PLCC)	✓	✓	D	D	✓	✓	–	–
100-Pin Very Thin Quad Flatpack (VQFP)	✓	✓	D	D	✓	✓	–	–
160-Pin Plastic Quad Flatpack (PQFP)	✓	✓	D	D	✓	✓	–	–
175-Pin Ceramic Pin Grid Array (CPGA)	D	D	D	D	D	–	–	–
176-Pin Thin Quad Flatpack (TQFP)	✓	✓	D	D	✓	✓	–	–

Notes:

1. *Applications:*
   C = Commercial
   I = Industrial
   M = Military
2. *Commercial only*

Availability:
✓ = Available
P = Planned
– = Not planned
D = Discontinued

Speed Grade:
–1 = Approx. 15% faster than Std.
–2 = Approx. 25% faster than Std.
–3 = Approx. 35% faster than Std.
(–2 and –3 speed grades have been discontinued.)

Device/Package	Speed Grade[1]				Application[1]			
	Std.	**–1**	**–2**	**–3**	**C**	**I**	**M**	**B**
A14V40A Device								
84-Pin Plastic Leaded Chip Carrier (PLCC)	✓	–	–	–	✓	–	–	–
100-Pin Very Thin Quad Flatpack (VQFP)	✓	–	–	–	✓	–	–	–
160-Pin Plastic Quad Flatpack (PQFP)	✓	–	–	–	✓	–	–	–
176-Pin Thin Quad Flatpack (TQFP)	✓	–	–	–	✓	–	–	–
A1460A Device								
160-Pin Plastic Quad Flatpack (PQFP)	✓	✓	D	D	✓	✓	–	–
176-Pin Thin Quad Flatpack (TQFP)	✓	✓	D	D	✓	✓	–	–
196-Pin Ceramic Quad Flatpack (CQFP)	✓	✓	–	–	✓	–	✓	✓
207-Pin Ceramic Pin Grid Array (CPGA)	✓	✓	D	D	✓	–	✓	✓
208-Pin Plastic Quad Flatpack (PQFP)	✓	✓	D	D	✓	✓	–	–
225-Pin Plastic Ball Grid Array (BGA)	D	D	D	D	D	–	–	–
A14V60A Device								
160-Pin Plastic Quad Flatpack (PQFP)	✓	–	–	–	✓	–	–	–
176-Pin Thin Quad Flatpack (TQFP)	✓	–	–	–	✓	–	–	–
208-Pin Plastic Quad Flatpack (PQFP)	✓	–	–	–	✓	–	–	–
A14100A Device								
208-Pin Power Quad Flatpack (RQFP)	✓	✓	D	D	✓	✓	–	–
257-Pin Ceramic Pin Grid Array (CPGA)	✓	✓	D	D	✓	–	✓	✓
313-Pin Plastic Ball Grid Array (BGA)	✓	✓	D	D	✓	–	–	–
256-Pin Ceramic Quad Flatpack (CQFP)	✓	✓	–	–	✓	–	✓	✓
A14V100A Device								
208-Pin Power Quad Flatpack (RQFP)	✓	–	–	–	✓	–	–	–
313-Pin Plastic Ball Grid Array (BGA)	✓	–	–	–	✓	–	–	–

Notes:

1. *Applications:*
   C = Commercial
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–1 = Approx. 15% faster than Std.
–2 = Approx. 25% faster than Std.
–3 = Approx. 35% faster than Std.
(–2 and –3 speed grades have been discontinued.)

ACT 3 Family Overview

Detailed Specifications

Package Pin Assignments

Datasheet Information

2 – Detailed Specifications

This section of the datasheet is meant to familiarize the user with the architecture of the ACT 3 family of FPGA devices. A generic description of the family will be presented first, followed by a detailed description of the logic blocks, the routing structure, the antifuses, and the special function circuits. The on-chip circuitry required to program the devices is not covered.

Topology

The ACT 3 family architecture is composed of six key elements: Logic modules, I/O modules, I/O Pad Drivers, Routing Tracks, Clock Networks, and Programming and Test Circuits. The basic structure is similar for all devices in the family, differing only in the number of rows, columns, and I/Os. The array itself consists of alternating rows of modules and channels. The logic modules and channels are in the center of the array; the I/O modules are located along the array periphery. A simplified floor plan is depicted in Figure 2-1.

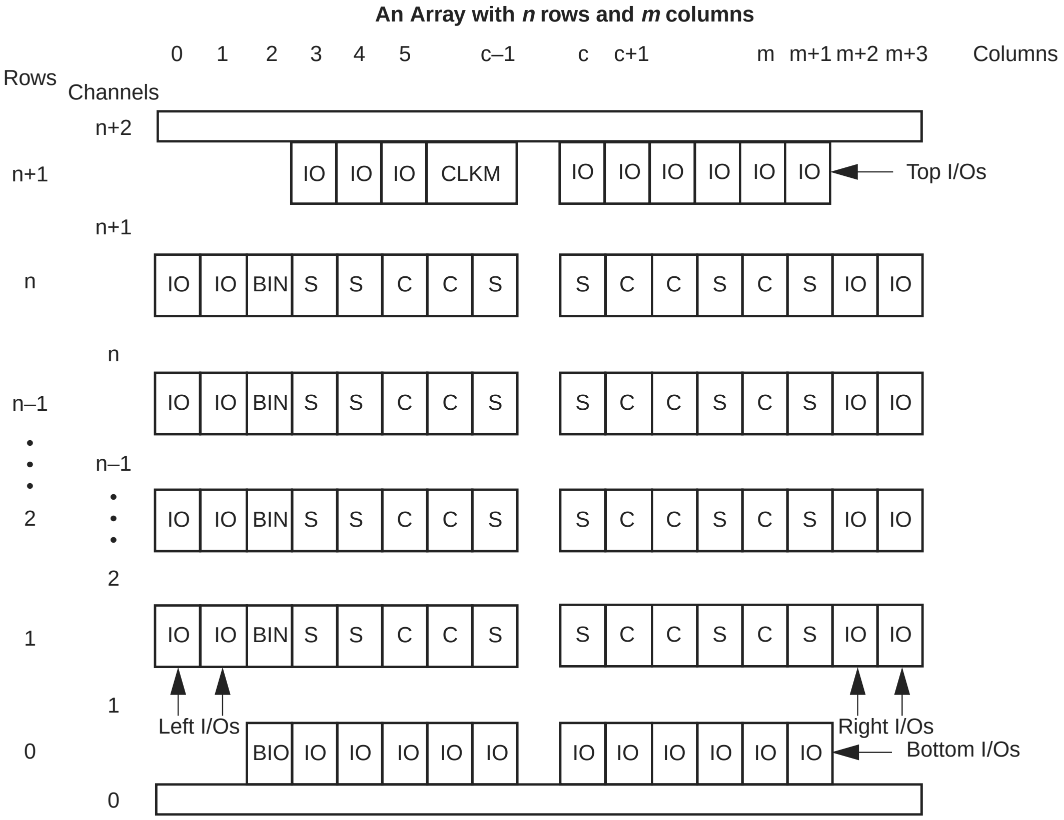


Figure 2-1 • **Generalized Floor Plan of ACT 3 Device**

The S-module contains a full implementation of the C-module plus a clearable sequential element that can either implement a latch or flip-flop function. The S-module can therefore implement any function implemented by the C-module. This allows complex combinatorial-sequential functions to be implemented with no delay penalty. The Designer Series Development System will automatically combine any C-module macro driving an S-module macro into the S-module, thereby freeing up a logic module and eliminating a module delay.

The clear input CLR is accessible from the routing channel. In addition, the clock input may be connected to one of three clock networks: CLKA, CLKB, or HCLK. The C-module and S-module functional descriptions are shown in Figure 2-2 and Figure 2-3 on page 2-2. The clock selection is determined by a multiplexer select at the clock input to the S-module.

I/Os

I/O Modules

I/O modules provide an interface between the array and the I/O Pad Drivers. I/O modules are located in the array and access the routing channels in a similar fashion to logic modules. The I/O module schematic is shown in Figure 4. The signals DataIn and DataOut connect to the I/O pad driver.

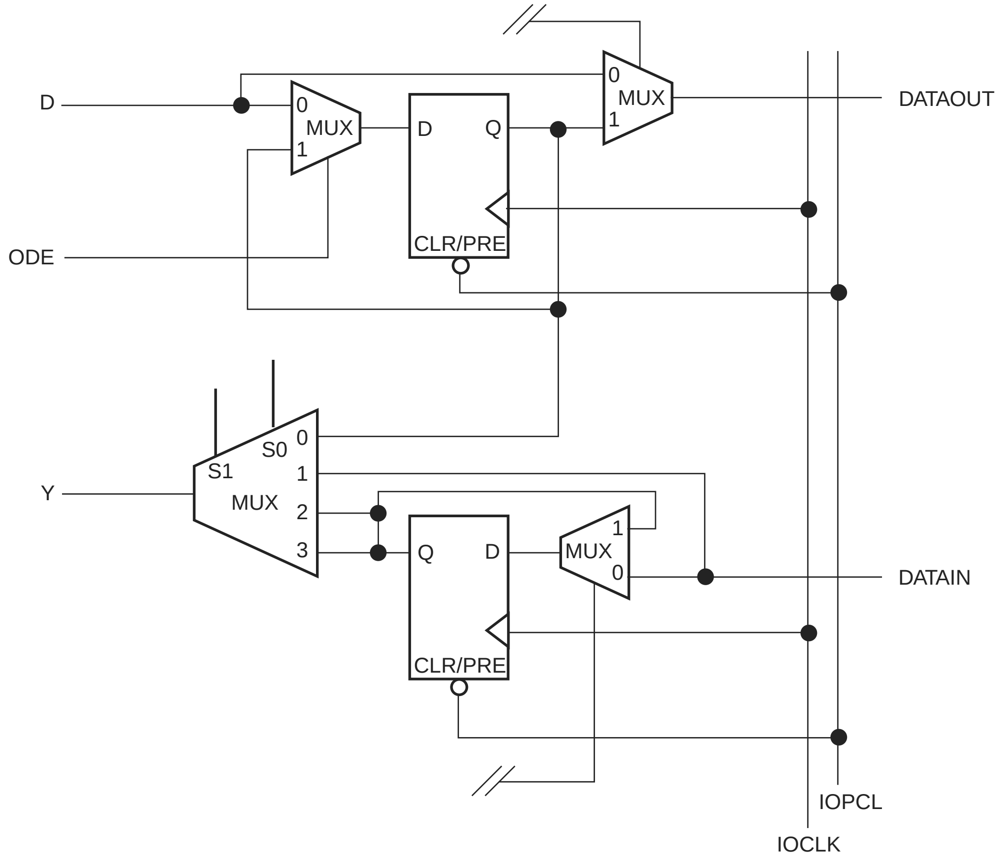


Figure 2-4 • **Functional Diagram for I/O Module**

Each I/O module contains two D-type flip-flops. Each flip-flop is connected to the dedicated I/O clock (IOCLK). Each flip-flop can be bypassed by nonsequential I/Os. In addition, each flip-flop contains a data enable input that can be accessed from the routing channels (ODE and IDE). The asynchronous preset/clear input is driven by the dedicated preset/clear network (IOPCL). Either preset or clear can be selected individually on an I/O module by I/O module basis.

Dedicated Clocks

Dedicated clock networks support high performance by providing sub-nanosecond skew and guaranteed performance. Dedicated clock networks contain no programming elements in the path from the I/O Pad Driver to the input of S-modules or I/O modules. There are two dedicated clock networks: one for the array registers (HCLK), and one for the I/O registers (IOCLK). The clock networks are accessed by special I/Os.

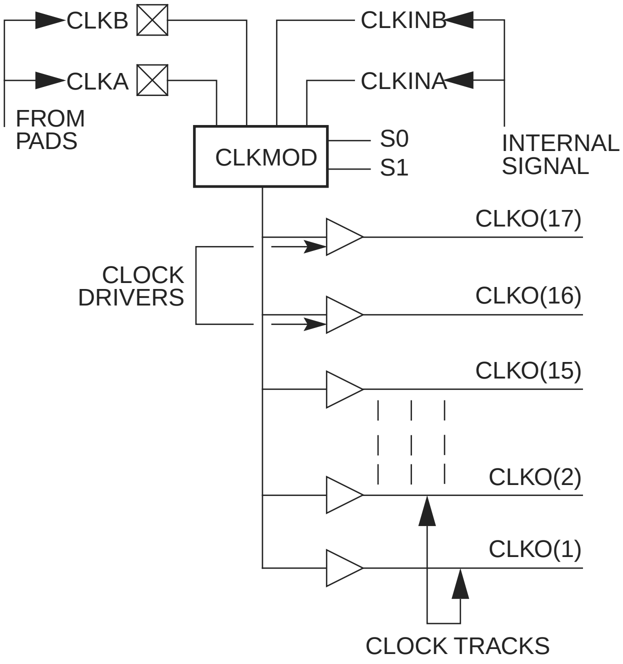


Figure 2-6 • **Clock Networks**

The routed clock networks are referred to as CLK0 and CLK1. Each network is connected to a clock module (CLKMOD) that selects the source of the clock signal and may be driven as follows (Figure 2-6):

- Externally from the CLKA pad
- Externally from the CLKB pad
- Internally from the CLKINA input
- Internally from the CLKINB input

The clock modules are located in the top row of I/O modules. Clock drivers and a dedicated horizontal clock track are located in each horizontal routing channel. The function of the clock module is determined by the selection of clock macros from the macro library. The macro CLKBUF is used to connect one of the two external clock pins to a clock network, and the macro CLKINT is used to connect an internally generated clock signal to a clock network. Since both clock networks are identical, the user does not care whether CLK0 or CLK1 is being used. Routed clocks can also be used to drive high fanout nets like resets, output enables, or data enables. This saves logic modules and results in performance increases in some cases.

Routing Structure

The ACT 3 architecture uses vertical and horizontal routing tracks to connect the various logic and I/O modules. These routing tracks are metal interconnects that may either be of continuous length or broken into segments. Segments can be joined together at the ends using antifuses to increase their lengths up to the full length of the track.

3.3 V Operating Conditions

***Table 2-5* • Absolute Maximum Ratings[1], Free Air Temperature Range**

Symbol	Parameter	Limits	Units
VCC	DC supply voltage	–0.5 to +7.0	V
VI	Input voltage	–0.5 to VCC + 0.5	V
VO	Output voltage	–0.5 to VCC + 0.5	V
IIO	I/O source sink current[2]	±20	mA
T_{STG}	Storage temperature	–65 to +150	°C

Notes:

1. *Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum rated conditions for extended periods may affect device reliability. Device should not be operated outside the recommended operating conditions.*
2. *Device inputs are normally high impedance and draw extremely low current. However, when input voltage is greater than VCC + 0.5 V for less than GND –0.5 V, the internal protection diodes will forward bias and can draw excessive current.*

***Table 2-6* • Recommended Operating Conditions**

Parameter	Commercial	Units
Temperature range*	0 to +70	°C
Power supply tolerance	3.0 to 3.6	V

*Note: *Ambient temperature (T_A) is used for commercial.*

***Table 2-7* • Electrical Specifications**

Parameter		Commercial		Units
		Min.	Max.	
VOH[1]	IOH = –4 mA	2.15	–	V
	IOH = –3.2 mA	2.4		V
VOL[1]	IOL = 6 mA		0.4	V
VIL		–0.3	0.8	V
VIH		2.0	VCC + 0.3	V
Input transition time t_R, t_F[2]	VI = VCC or GND	–10	+10	µA
C_{IO} I/O Capacitance[2,3]			10	pF
Standby current, ICC[4] (typical = 0.3 mA)			0.75	mA
Leakage current[5]		–10	10	µA

1. *Only one output tested at a time. VCC = minimum.*
2. *Not tested; for information only.*
3. *Includes worst-case 84-pin PLCC package capacitance. VOUT = 0 V, f - 1 MHz.*
4. *Typical standby current = 0.3 mA. All outputs unloaded. All inputs = VCC or GND.*
5. *VO, VIN = VCC or GND*

A1415A, A14V15A Timing Characteristics (continued)

Table 2-19 **• A1415A, A14V15A Worst-Case Commercial Conditions, VCC = 4.75 V, T_J = 70°C**

I/O Module Input Propagation Delays		**–3 Speed[1]**		**–2 Speed[1]**		**–1 Speed**		**Std. Speed**		**3.3 V Speed[2]**		**Units**
Parameter/Description		**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	
t_{INY}	Input Data Pad to Y		2.8		3.2		3.6		4.2		5.5	ns
t_{ICKY}	Input Reg IOCLK Pad to Y		4.7		5.3		6.0		7.0		9.2	ns
t_{OCKY}	Output Reg IOCLK Pad to Y		4.7		5.3		6.0		7.0		9.2	ns
t_{ICLRY}	Input Asynchronous Clear to Y		4.7		5.3		6.0		7.0		9.2	ns
t_{OCLRY}	Output Asynchronous Clear to Y		4.7		5.3		6.0		7.0		9.2	ns
Predicted Input Routing Delays[2]												
t_{RD1}	FO = 1 Routing Delay		0.9		1.0		1.1		1.3		1.7	ns
t_{RD2}	FO = 2 Routing Delay		1.2		1.4		1.6		1.8		2.4	ns
t_{RD3}	FO = 3 Routing Delay		1.4		1.6		1.8		2.1		2.8	ns
t_{RD4}	FO = 4 Routing Delay		1.7		1.9		2.2		2.5		3.3	ns
t_{RD8}	FO = 8 Routing Delay		2.8		3.2		3.6		4.2		5.5	ns
I/O Module Sequential Timing (wrt IOCLK pad)												
t_{INH}	Input F-F Data Hold	0.0		0.0		0.0		0.0		0.0		ns
t_{INSU}	Input F-F Data Setup	2.0		2.3		2.5		3.0		3.0		ns
t_{IDEH}	Input Data Enable Hold	0.0		0.0		0.0		0.0		0.0		ns
t_{IDESU}	Input Data Enable Setup	5.8		6.5		7.5		8.6		8.6		ns
t_{OUTH}	Output F-F Data hold	0.7		0.8		0.9		1.0		1.0		ns
t_{OUTSU}	Output F-F Data Setup	0.7		0.8		0.9		1.0		1.0		ns
t_{ODEH}	Output Data Enable Hold	0.3		0.4		0.4		0.5		0.5		ns
f_{ODESU}	Output Data Enable Setup	1.3		1.5		1.7		2.0		2.0		ns

Notes:

1. *The –2 and –3 speed grades have been discontinued. Please refer to the Product Discontinuation Notices (PDNs) listed below:*

   PDN March 2001
   PDN 0104
   PDN 0203
   PDN 0604
   PDN 1004

2. *Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual worst-case performance. Post-route timing is based on actual routing delay measurements performed on the device prior to shipment.*

A1415A, A14V15A Timing Characteristics (continued)

***Table 2-21* • A1415A, A14V15A Worst-Case Commercial Conditions, VCC = 4.75 V, T_J = 70°C**

Dedicated (hardwired) I/O Clock Network		**–3 Speed**		**–2 Speed**		**–1 Speed**		**Std. Speed**		**3.3 V Speed[1]**		**Units**
Parameter/Description		**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	
t_{IOCKH}	Input Low to High (pad to I/O module input)		2.0		2.3		2.6		3.0		3.5	ns
t_{IOPWH}	Minimum Pulse Width High	1.9		2.4		3.3		3.8		4.8		ns
t_{IPOWL}	Minimum Pulse Width Low	1.9		2.4		3.3		3.8		4.8		ns
t_{IOSAPW}	Minimum Asynchronous Pulse Width	1.9		2.4		3.3		3.8		4.8		ns
t_{IOCKSW}	Maximum Skew		0.4		0.4		0.4		0.4		0.4	ns
t_{IOP}	Minimum Period	4.0		5.0		6.8		8.0		10.0		ns
f_{IOMAX}	Maximum Frequency		250		200		150		125		100	MHz
Dedicated (hardwired) Array Clock												
t_{HCKH}	Input Low to High (pad to S-module input)		3.0		3.4		3.9		4.5		5.5	ns
t_{HCKL}	Input High to Low (pad to S-module input)		3.0		3.4		3.9		4.5		5.5	ns
t_{HPWH}	Minimum Pulse Width High	1.9		2.4		3.3		3.8		4.8		ns
t_{HPWL}	Minimum Pulse Width Low	1.9		2.4		3.3		3.8		4.8		ns
t_{HCKSW}	Delta High to Low, Low Slew		0.3		0.3		0.3		0.3		0.3	ns
t_{HP}	Minimum Period	4.0		5.0		6.8		8.0		10.0		ns
f_{HMAX}	Maximum Frequency		250		200		150		125		100	MHz
Routed Array Clock Networks												
t_{RCKH}	Input Low to High (FO = 64)		3.7		4.1		4.7		5.5		9.0	ns
t_{RCKL}	Input High to Low (FO = 64)		4.0		4.5		5.1		6.0		9.0	ns
t_{RPWH}	Min. Pulse Width High (FO = 64)	3.3		3.8		4.2		4.9		6.5		ns
t_{RPWL}	Min. Pulse Width Low (FO = 64)	3.3		3.8		4.2		4.9		6.5		ns
t_{RCKSW}	Maximum Skew (FO = 128)		0.7		0.8		0.9		1.0		1.0	ns
t_{RP}	Minimum Period (FO = 64)	6.8		8.0		8.7		10.0		13.4		ns
f_{RMAX}	Maximum Frequency (FO = 64)		150		125		115		100		75	MHz
Clock-to-Clock Skews												
$t_{IOHCKSW}$	I/O Clock to H-Clock Skew	0.0	1.7	0.0	1.8	0.0	2.0	0.0	2.2	0.0	3.0	ns
$t_{IORCKSW}$	I/O Clock to R-Clock Skew (FO = 64)	0.0	1.0	0.0	1.0	0.0	1.0	0.0	1.0	0.0	3.0	ns
t_{HRCKSW}	H-Clock to R-Clock Skew (FO = 64) (FO = 50% maximum)	0.0	1.0	0.0	1.0	0.0	1.0	0.0	1.0	0.0 0.0	3.0 3.0	ns

Notes:

1. *Delays based on 35 pF loading.*
2. *The –2 and –3 speed grades have been discontinued. Refer to PDN 0104, PDN 0203, PDN 0604, and PDN 1004 at http://www.microsemi.com/soc/support/notifications/default.aspx#pdn.*

A1440A, A14V40A Timing Characteristics (continued)

***Table 2-28* • A1440A, A14V40A Worst-Case Commercial Conditions, VCC = 4.75 V, T_J = 70°C**

I/O Module – TTL Output Timing[1]		**–3 Speed[2]**		**–2 Speed[2]**		**–1 Speed**		**Std. Speed**		**3.3 V Speed[1]**		**Units**
Parameter/Description		**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	
t_{DHS}	Data to Pad, High Slew		5.0		5.6		6.4		7.5		9.8	ns
t_{DLS}	Data to Pad, Low Slew		8.0		9.0		10.2		12.0		15.6	ns
t_{ENZHS}	Enable to Pad, Z to H/L, High Slew		4.0		4.5		5.1		6.0		7.8	ns
t_{ENZLS}	Enable to Pad, Z to H/L, Low Slew		7.4		8.3		9.4		11.0		14.3	ns
t_{ENHSZ}	Enable to Pad, H/L to Z, High Slew		7.4		8.3		9.4		11.0		14.3	ns
t_{ENLSZ}	Enable to Pad, H/L to Z, Low Slew		7.4		8.3		9.4		11.0		14.3	ns
t_{CKHS}	IOCLK Pad to Pad H/L, High Slew		8.5		8.5		9.5		11.0		14.3	ns
t_{CKLS}	IOCLK Pad to Pad H/L, Low Slew		11.3		11.3		13.5		15.0		19.5	ns
d_{TLHHS}	Delta Low to High, High Slew		0.02		0.02		0.03		0.03		0.04	ns/pF
d_{TLHLS}	Delta Low to High, Low Slew		0.05		0.05		0.06		0.07		0.09	ns/pF
d_{THLHS}	Delta High to Low, High Slew		0.04		0.04		0.04		0.05		0.07	ns/pF
d_{THLLS}	Delta High to Low, Low Slew		0.05		0.05		0.06		0.07		0.09	ns/pF
I/O Module – CMOS Output Timing[1]												
t_{DHS}	Data to Pad, High Slew		6.2		7.0		7.9		9.3		12.1	ns
t_{DLS}	Data to Pad, Low Slew		11.7		13.1		14.9		17.5		22.8	ns
t_{ENZHS}	Enable to Pad, Z to H/L, High Slew		5.2		5.9		6.6		7.8		10.1	ns
t_{ENZLS}	Enable to Pad, Z to H/L, Low Slew		8.9		10.0		11.3		13.3		17.3	ns
t_{ENHSZ}	Enable to Pad, H/L to Z, High Slew		7.4		8.3		9.4		11.0		14.3	ns
t_{ENLSZ}	Enable to Pad, H/L to Z, Low Slew		7.4		8.3		9.4		11.0		14.3	ns
t_{CKHS}	IOCLK Pad to Pad H/L, High Slew		9.0		9.0		10.1		11.8		14.3	ns
t_{CKLS}	IOCLK Pad to Pad H/L, Low Slew		13.0		13.0		15.6		17.3		22.5	ns
d_{TLHHS}	Delta Low to High, High Slew		0.04		0.04		0.05		0.06		0.08	ns/pF
d_{TLHLS}	Delta Low to High, Low Slew		0.07		0.08		0.09		0.11		0.14	ns/pF
d_{THLHS}	Delta High to Low, High Slew		0.03		0.03		0.03		0.04		0.05	ns/pF
d_{THLLS}	Delta High to Low, Low Slew		0.04		0.04		0.04		0.05		0.07	ns/pF

Notes:

1. *Delays based on 35 pF loading.*
2. *The –2 and –3 speed grades have been discontinued. Refer to PDN 0104, PDN 0203, PDN 0604, and PDN 1004 at http://www.microsemi.com/soc/support/notifications/default.aspx#pdn.*

A14100A, A14V100A Timing Characteristics (continued)

***Table 2-37* • A14100A, A14V100A Worst-Case Commercial Conditions, VCC = 4.75 V, T_J = 70°C**

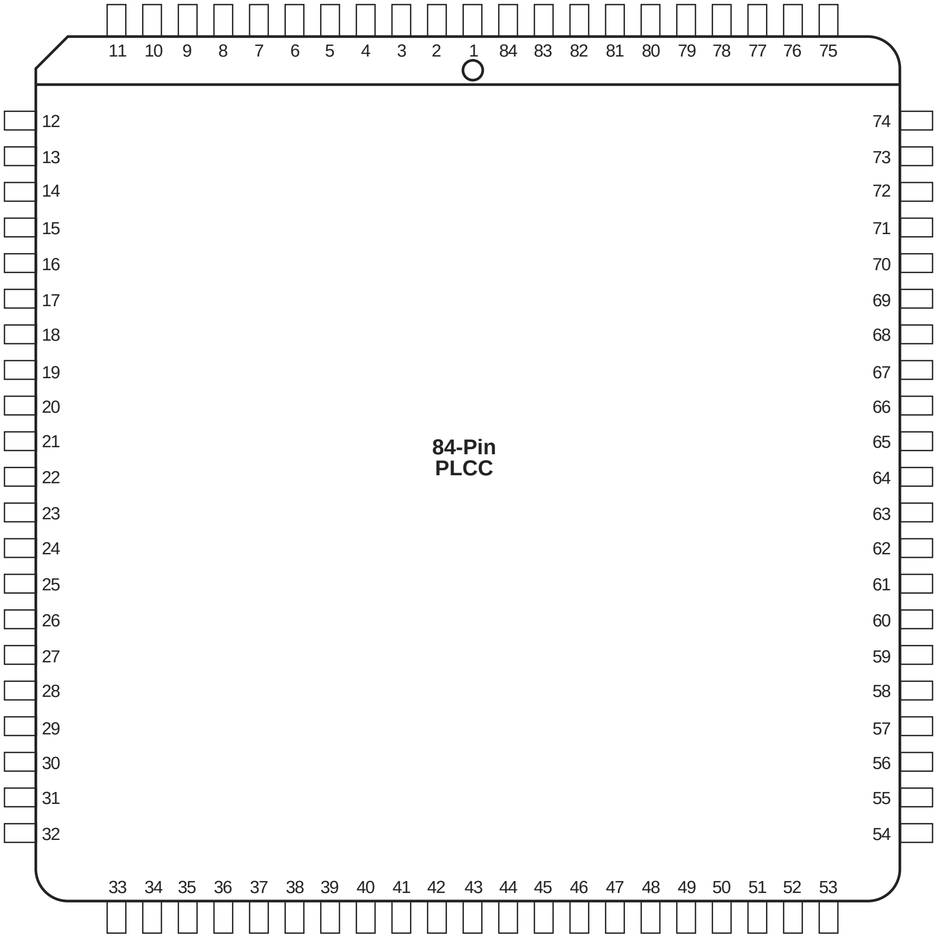
Dedicated (hardwired) I/O Clock Network		**–3 Speed[1]**		**–2 Speed[1]**		**–1 Speed**		**Std. Speed**		**3.3 V Speed[1]**		**Units**
Parameter/Description		**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	
t_{IOCKH}	Input Low to High (pad to I/O module input)		2.3		2.6		3.0		3.5		4.5	ns
t_{IOPWH}	Minimum Pulse Width High	2.4		3.3		3.8		4.8		6.5		ns
t_{IPOWL}	Minimum Pulse Width Low	2.4		3.3		3.8		4.8		6.5		ns
t_{IOSAPW}	Minimum Asynchronous Pulse Width	2.4		3.3		3.8		4.8		6.5		ns
t_{IOCKSW}	Maximum Skew		0.6		0.6		0.7		0.8		0.6	ns
t_{IOP}	Minimum Period	5.0		6.8		8.0		10.0		13.4		ns
f_{IOMAX}	Maximum Frequency		200		150		125		100		75	MHz
Dedicated (hardwired) Array Clock												
t_{HCKH}	Input Low to High (pad to S-module input)		3.7		4.1		4.7		5.5		7.0	ns
t_{HCKL}	Input High to Low (pad to S-module input)		3.7		4.1		4.7		5.5		7.0	ns
t_{HPWH}	Minimum Pulse Width High	2.4		3.3		3.8		4.8		6.5		ns
t_{HPWL}	Minimum Pulse Width Low	2.4		3.3		3.8		4.8		6.5		ns
t_{HCKSW}	Delta High to Low, Low Slew		0.6		0.6		0.7		0.8		0.6	ns
t_{HP}	Minimum Period	5.0		6.8		8.0		10.0		13.4		ns
f_{HMAX}	Maximum Frequency		200		150		125		100		75	MHz
Routed Array Clock Networks												
t_{RCKH}	Input Low to High (FO = 64)		6.0		6.8		7.7		9.0		11.8	ns
t_{RCKL}	Input High to Low (FO = 64)		6.0		6.8		7.7		9.0		11.8	ns
t_{RPWH}	Min. Pulse Width High (FO = 64)	4.1		4.5		5.4		6.1		8.2		ns
t_{RPWL}	Min. Pulse Width Low (FO = 64)	4.1		4.5		5.4		6.1		8.2		ns
t_{RCKSW}	Maximum Skew (FO = 128)		1.2		1.4		1.6		1.8		1.8	ns
t_{RP}	Minimum Period (FO = 64)	8.3		9.3		11.1		12.5		16.7		ns
f_{RMAX}	Maximum Frequency (FO = 64)		120		105		90		80		60	MHz
Clock-to-Clock Skews												
$t_{IOHCKSW}$	I/O Clock to H-Clock Skew	0.0	2.6	0.0	2.7	0.0	2.9	0.0	3.0	0.0	3.0	ns
$t_{IORCKSW}$	I/O Clock to R-Clock Skew (FO = 64) (FO = 350)	0.0 0.0	1.7 5.0	0.0 0.0	1.7 5.0	0.0 0.0	1.7 5.0	0.0 0.0	1.7 5.0	0.0 0.0	5.0 5.0	ns
t_{HRCKSW}	H-Clock to R-Clock Skew (FO = 64) (FO = 350)	0.0 0.0	1.3 3.0	0.0 0.0	1.0 3.0	0.0 0.0	1.0 3.0	0.0 0.0	1.0 3.0	0.0 0.0	1.0 3.0	ns

*Notes: **

1. *The –2 and –3 speed grades have been discontinued. Refer to PDN 0104, PDN 0203, PDN 0604, and PDN 1004 at http://www.microsemi.com/soc/support/notifications/default.aspx#pdn.*
2. *Delays based on 35 pF loading.*

3 – Package Pin Assignments

PL84



Note: This is the top view of the package.

Note

For Package Manufacturing and Environmental information, visit the Resource Center at http://www.microsemi.com/soc/products/solutions/package/docs.aspx.

PQ100		
Pin Number	**A1415 Function**	**A1425 Function**
2	IOCLK, I/O	IOCLK, I/O
14	CLKA, I/O	CLKA, I/O
15	CLKB, I/O	CLKB, I/O
16	VCC	VCC
17	GND	GND
18	VCC	VCC
19	GND	GND
20	PRA, I/O	PRA, I/O
27	DCLK, I/O	DCLK, I/O
28	GND	GND
29	SDI, I/O	SDI, I/O
34	MODE	MODE
35	VCC	VCC
36	GND	GND
47	GND	GND
48	VCC	VCC
61	PRB, I/O	PRB, I/O
62	GND	GND
63	VCC	VCC
64	GND	GND
65	VCC	VCC
67	HCLK, I/O	HCLK, I/O
77	SDO	SDO
78	IOPCL, I/O	IOPCL, I/O
79	GND	GND
85	VCC	VCC
86	VCC	VCC
87	GND	GND
96	VCC	VCC
97	GND	GND

Notes:

1. All unlisted pin numbers are user I/Os.
2. NC denotes no connection.
3. MODE should be terminated to GND through a 10K resistor to enable Actionprobe usage; otherwise it can be terminated directly to GND.

PQ160			
Pin Number	**A1425, A14V25 Function**	**A1440, A14V40 Function**	**A1460, A14V60 Function**
1	GND	GND	GND
2	SDI, I/O	SDI, I/O	SDI, I/O
5	NC	I/O	I/O
9	MODE	MODE	MODE
10	VCC	VCC	VCC
14	NC	I/O	I/O
15	GND	GND	GND
18	VCC	VCC	VCC
19	GND	GND	GND
20	NC	I/O	I/O
24	NC	I/O	I/O
27	NC	I/O	I/O
28	VCC	VCC	VCC
29	VCC	VCC	VCC
40	GND	GND	GND
41	NC	I/O	I/O
43	NC	I/O	I/O
45	NC	I/O	I/O
46	VCC	VCC	VCC
47	NC	I/O	I/O
49	NC	I/O	I/O
51	NC	I/O	I/O
53	NC	I/O	I/O
58	PRB, I/O	PRB, I/O	PRB, I/O
59	GND	GND	GND
60	VCC	VCC	VCC
62	HCLK, I/O	HCLK, I/O	HCLK, I/O
63	GND	GND	GND
74	NC	I/O	I/O
75	VCC	VCC	VCC
76	NC	I/O	I/O
77	NC	I/O	I/O
78	NC	I/O	I/O
79	SDO	SDO	SDO
80	IOPCL, I/O	IOPCL, I/O	IOPCL, I/O
81	GND	GND	GND
90	VCC	VCC	VCC
91	VCC	VCC	VCC

PG100	
A1415 Function	**Location**
CLKA or I/O	C7
CLKB or I/O	D6
DCLK or I/O	C4
GND	C3, C6, C9, E9, F3, F9, J3, J6, J8, J9
HCLK or I/O	H6
IOCLK or I/O	C10
IOPCL or I/O	K9
MODE	C2
PRA or I/O	A6
PRB or I/O	L3
SDI or I/O	B3
SDO	L9
VCC	B6, B10, E11, F2, F10, G2, K2, K6, K10

Notes:

1. All unlisted pin numbers are user I/Os.
2. NC denotes no connection.
3. MODE should be terminated to GND through a 10K resistor to enable Actionprobe usage; otherwise it can be terminated directly to GND.
4. The PG100 package has been discontinued.

PG175	
A1440 Function	**Location**
CLKA or I/O	C9
CLKB or I/O	A9
DCLK or I/O	D5
GND	D4, D8, D11, D12, E4, E14, H4, H12, L4, L12, M4, M8, M12
HCLK or I/O	R8
IOCLK or I/O	E12
IOPCL or I/O	P13
MODE	F3
NC	A1, A2, A15, B2, B3, P2, P14, R1, R2, R14, R15
PRA or I/O	B8
PRB or I/O	R7
SDI or I/O	D3
SDO	N12
VCC	C3, C8, C13, E15, H3, H13, L1, L14, N3, N8, N13

Notes:

1. All unlisted pin numbers are user I/Os.
2. NC denotes no connection.
3. MODE should be terminated to GND through a 10K resistor to enable Actionprobe usage; otherwise it can be terminated directly to GND.
4. The PG175 package has been discontinued.

PG207	
A1460 Function	**Location**
CLKA or I/O	K1
CLKB or I/O	J3
DCLK or I/O	E4
GND	C14, D4, D5, D9, D14, J4, J14, P3, P4, P7, P9, P14, R15
HCLK or I/O	J15
IOCLK or I/O	P5
IOPCL or I/O	N14
MODE	D7
NC	A1, A2, A16, A17, B1, B17, C1, C2, S1, S3, S17, T1, T2, T16, T17
PRA or I/O	H1
PRB or I/O	K16
SDI or I/O	C3
SDO	P15
VCC	B2, B9, B16, D11, J2, J16, P12, S2, S9, S16, T5

Notes:

1. All unlisted pin numbers are user I/Os.
2. NC denotes no connection.
3. MODE should be terminated to GND through a 10K resistor to enable Actionprobe usage; otherwise it can be terminated directly to GND.

4 – Datasheet Information

List of Changes

The following table lists critical changes that were made in each version of the datasheet.

Revision	Changes	Page
Revision 3 (January 2012)	The description for SDO pins had earlier been removed from the datasheet and has now been included again, in the "Pin Descriptions" section (SAR 35820).	2-21
	SDO pin numbers had earlier been removed from package pin assignment tables in the datasheet, and have now been restored to the pin tables (SAR 35820).	3-1
Revision 2 (September 2011)	The ACT 3 datasheet was formatted newly in the style used for current datasheets. The same information is present (other than noted in the list of changes for this revision) but divided into chapters.	N/A
	The datasheet was revised to note in multiple places that speed grades –2 and –3 have been discontinued. The following device/package combinations have been discontinued for all speed grades and temperatures (SAR 33872): A1415 PG100 A1425 PG133 A1440 PG175 A1460 BG225 Refer to PDN 0104, PDN 0203, PDN 0604, and PDN 1004.	I and others
	The "Features" section was revised to state the clock-to-ouput time and on-chip performance for –1 speed grade as 9.0 ns and 186 MHz. The "General Description" section was revised in accordance (SAR 33872).	I
	The maximum performance values were updated in Table 1 • ACT 3 Family Product Information, and now reflect worst-case commercial for the –1 speed grade (SAR 33872).	I
	The "Product Plan" table was updated as follows to conform to current offerings (SAR 33872): The A1415A device is offered in PL84, PG100, and VQ100 packages for Military application. The A1440A device is offered in TQ176 and VQ100 packages for Industrial application.	III
	Table 1-1 • Chip-to-Chip Performance (worst-case commercial) was updated to include data for all speed grades instead of only –3 (SAR 33872).	1-2
	Figure 1-1 • Predictable Performance (worst-case commercial, –1 speed grade) was revised to reflect values for the –1 speed grade (SAR 33872).	1-1
	Figure 2-10 • Timing Model was updated to show data for the –1 speed grade instead of –3 (SAR 33872).	2-16
	Table 2-14 • Logic Module and Routing Delay by Fanout (ns); Worst-Case Commercial Conditions was updated to include data for all speed grades instead of only –3 (SAR 33872).	2-20
	Package names used in the "Package Pin Assignments" section and throughout the document were revised to match standards given in *Package Mechanical Drawings* (SAR 27395).	3-1

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