

Welcome to E-XFL.COM

#### Understanding <u>Embedded - FPGAs (Field</u> <u>Programmable Gate Array)</u>

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

#### **Applications of Embedded - FPGAs**

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

#### Details

Details	
Product Status	Obsolete
Number of LABs/CLBs	848
Number of Logic Elements/Cells	-
Total RAM Bits	-
Number of I/O	167
Number of Gates	6000
Voltage - Supply	4.5V ~ 5.5V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 70°C (TA)
Package / Case	208-BFQFP
Supplier Device Package	208-PQFP (28x28)
Purchase URL	https://www.e-xfl.com/product-detail/microsemi/a1460a-pqg208c

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

Accelerator Series FPGAs – ACT 3 Family

	Speed Grade <sup>1</sup>			Application <sup>1</sup>				
Device/Package	Std.	-1	-2	-3	С	I	м	В
A14V40A Device								
84-Pin Plastic Leaded Chip Carrier (PLCC)	1	-	-	_	1	_	_	_
100-Pin Very Thin Quad Flatpack (VQFP)	✓	-	-	-	1	-	-	-
160-Pin Plastic Quad Flatpack (PQFP)	~	-	-	-	✓	-	-	-
176-Pin Thin Quad Flatpack (TQFP)	~	-	-	-	✓	-	-	-
A1460A Device		•		I			1	
160-Pin Plastic Quad Flatpack (PQFP)	✓	✓	D	D	1	~	-	-
176-Pin Thin Quad Flatpack (TQFP)	✓	~	D	D	✓	✓	-	-
196-Pin Ceramic Quad Flatpack (CQFP)	1	1	-	_	1	-	1	1
207-Pin Ceramic Pin Grid Array (CPGA)	1	1	D	D	1	-	1	1
208-Pin Plastic Quad Flatpack (PQFP)	1	<ul> <li>✓</li> </ul>	D	D	1	1	-	_
225-Pin Plastic Ball Grid Array (BGA)	D	D	D	D	D	-	-	-
A14V60A Device					-		-	
160-Pin Plastic Quad Flatpack (PQFP)	✓	-	-	_	~	-	_	-
176-Pin Thin Quad Flatpack (TQFP)	✓	-	-	-	1	-	-	-
208-Pin Plastic Quad Flatpack (PQFP)	✓	-	-	_	~	-	_	_
A14100A Device								
208-Pin Power Quad Flatpack (RQFP)	✓	~	D	D	~	~	_	_
257-Pin Ceramic Pin Grid Array (CPGA)	✓	~	D	D	~	-	~	~
313-Pin Plastic Ball Grid Array (BGA)	✓	~	D	D	~	-	_	-
256-Pin Ceramic Quad Flatpack (CQFP)	✓	~	-	_	~	-	~	~
A14V100A Device								
208-Pin Power Quad Flatpack (RQFP)	$\checkmark$	_	_	_	1	_	_	_
313-Pin Plastic Ball Grid Array (BGA)	✓	-	-	-	1	-	-	-

Notes:

1. Applications: C = CommercialI = Industrial
M = Military
Commercial only

- Availability:
- ✓ = Available
- P = Planned- = Not planned
- D = Discontinued

Speed Grade:

-1 = Approx. 15% faster than Std. -2 = Approx. 25% faster than Std. -3 = Approx. 35% faster than Std. (-2 and -3 speed grades have been discontinued.)

# 1 – ACT 3 Family Overview

# **General Description**

Microsemi's ACT 3 Accelerator Series of FPGAs offers the industry's fastest high-capacity programmable logic device. ACT 3 FPGAs offer a high performance, PCI compliant programmable solution capable of 186 MHz on-chip performance and 9.0 nanosecond clock-to-output (-1 speed grade), with capacities spanning from 1,500 to 10,000 gate array equivalent gates.

The ACT 3 family builds on the proven two-module architecture consisting of combinatorial and sequential logic modules used in Microsemi's 3200DX and 1200XL families. In addition, the ACT 3 I/O modules contain registers which deliver 9.0 nanosecond clock-to-out times (-1 speed grade). The devices contain four clock distribution networks, including dedicated array and I/O clocks, supporting very fast synchronous and asynchronous designs. In addition, routed clocks can be used to drive high fanout signals such as flip-flop resets and output.

The ACT 3 family is supported by Microsemi's Designer Series Development System which offers automatic placement and routing (with automatic or fixed pin assignments), static timing analysis, user programming, and debug and diagnostic probe capabilities.



*Figure 1-1* • Predictable Performance (worst-case commercial, –1 speed grade)

## System Performance Model





ACT 3 Family Overview

Device and Speed Grade	t <sub>CKHS</sub> (ns)	t <sub>TRACE</sub> (ns)	t <sub>INSU</sub> (ns)	Total (ns)	MHz
A1425A -3	7.5	1.0	1.8	10.3	97
A1460A -3	9.0	1.0	1.3	11.3	88
A1425A -2	7.5	1.0	2.0	10.5	95
A1460A -2	9.0	1.0	1.5	11.5	87
A1425A -1	9.0	1.0	2.3	12.3	81
A1460A -1	10.0	1.0	1.8	12.8	78
A1425A STD	10.0	1.0	2.7	13.7	73
A1460A STD	11.5	1.0	2.0	14.5	69

#### Table 1-1 • Chip-to-Chip Performance (worst-case commercial)

Note: The –2 and –3 speed grades have been discontinued. Refer to PDN 0104, PDN 0203, PDN 0604, and PDN 1004 at http://www.microsemi.com/soc/support/notifications/default.aspx#pdn.



The I/O module output Y is used to bring Pad signals into the array or to feed the output register back into the array. This allows the output register to be used in high-speed state machine applications. Side I/O modules have a dedicated output segment for Y extending into the routing channels above and below (similar to logic modules). Top/Bottom I/O modules have no dedicated output segment. Signals coming into the chip from the top or bottom are routed using F-fuses and LVTs (F-fuses and LVTs are explained in detail in the routing section).

## I/O Pad Drivers

All pad drivers are capable of being tristate. Each buffer connects to an associated I/O module with four signals: OE (Output Enable), IE (Input Enable), DataOut, and DataIn. Certain special signals used only during programming and test also connect to the pad drivers: OUTEN (global output enable), INEN (global input enable), and SLEW (individual slew selection). See Figure 2-5.



*Figure 2-5* • Function Diagram for I/O Pad Driver

## **Special I/Os**

The special I/Os are of two types: temporary and permanent. Temporary special I/Os are used during programming and testing. They function as normal I/Os when the MODE pin is inactive. Permanent special I/Os are user programmed as either normal I/Os or special I/Os. Their function does not change once the device has been programmed. The permanent special I/Os consist of the array clock input buffers (CLKA and CLKB), the hard-wired array clock input buffer (HCLK), the hard-wired I/O clock input buffer (IOCLK), and the hard-wired I/O register preset/clear input buffer (IOPCL). Their function is determined by the I/O macros selected.

# **Clock Networks**

The ACT 3 architecture contains four clock networks: two high-performance dedicated clock networks and two general purpose routed networks. The high-performance networks function up to 200 MHz, while the general purpose routed networks function up to 150 MHz.

# Dedicated Clocks

Dedicated clock networks support high performance by providing sub-nanosecond skew and guaranteed performance. Dedicated clock networks contain no programming elements in the path from the I/O Pad Driver to the input of S-modules or I/O modules. There are two dedicated clock networks: one for the array registers (HCLK), and one for the I/O registers (IOCLK). The clock networks are accessed by special I/Os.



Figure 2-6 • Clock Networks

The routed clock networks are referred to as CLK0 and CLK1. Each network is connected to a clock module (CLKMOD) that selects the source of the clock signal and may be driven as follows (Figure 2-6):

- Externally from the CLKA pad
- Externally from the CLKB pad
- Internally from the CLKINA input
- Internally from the CLKINB input

The clock modules are located in the top row of I/O modules. Clock drivers and a dedicated horizontal clock track are located in each horizontal routing channel. The function of the clock module is determined by the selection of clock macros from the macro library. The macro CLKBUF is used to connect one of the two external clock pins to a clock network, and the macro CLKINT is used to connect an internally generated clock signal to a clock network. Since both clock networks are identical, the user does not care whether CLK0 or CLK1 is being used. Routed clocks can also be used to drive high fanout nets like resets, output enables, or data enables. This saves logic modules and results in performance increases in some cases.

# **Routing Structure**

The ACT 3 architecture uses vertical and horizontal routing tracks to connect the various logic and I/O modules. These routing tracks are metal interconnects that may either be of continuous length or broken into segments. Segments can be joined together at the ends using antifuses to increase their lengths up to the full length of the track.



# 3.3 V Operating Conditions

Table 2-3 • Apsolute Maximum Ratings , Free Air Temperature Rang	Table 2-5 •	Absolute Maximum	Ratings <sup>1</sup> . Free Air	r Temperature Range
--	-------------	------------------	---------------------------------	---------------------

Symbol	Parameter	Limits	Units
VCC	DC supply voltage	-0.5 to +7.0	V
VI	Input voltage	-0.5 to VCC + 0.5	V
VO	Output voltage	-0.5 to VCC + 0.5	V
IIO	I/O source sink current <sup>2</sup>	±20	mA
T <sub>STG</sub>	Storage temperature	-65 to +150	°C

Notes:

1. Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum rated conditions for extended periods may affect device reliability. Device should not be operated outside the recommended operating conditions.

2. Device inputs are normally high impedance and draw extremely low current. However, when input voltage is greater than VCC + 0.5 V for less than GND –0.5 V, the internal protection diodes will forward bias and can draw excessive current.

Table 2-6 • Recommended Operating Conditions

Parameter	Commercial	Units
Temperature range*	0 to +70	°C
Power supply tolerance	3.0 to 3.6	V

Note: \*Ambient temperature  $(T_A)$  is used for commercial.

Table 2-7 • Elec	ctrical Sr	oecifications
------------------	------------	---------------

	C	Commercial			
Parameter	Min.	Max.	Units		
VOH <sup>1</sup>	IOH = -4 mA	2.15	_	V	
	IOH = -3.2 mA	2.4		V	
VOL <sup>1</sup>	IOL = 6 mA		0.4	V	
VIL		-0.3	0.8	V	
VIH		2.0	VCC + 0.3	V	
Input transition time t <sub>R</sub> , t <sub>F</sub> <sup>2</sup>	VI = VCC or GND	-10	+10	μA	
C <sub>IO</sub> I/O Capacitance <sup>2,3</sup>			10	pF	
Standby current, ICC <sup>4</sup> (typical = 0	).3 mA)		0.75	mA	
Leakage current <sup>5</sup>		-10	10	μA	

1. Only one output tested at a time. VCC = minimum.

2. Not tested; for information only.

3. Includes worst-case 84-pin PLCC package capacitance. VOUT = 0 V, f - 1 MHz.

4. Typical standby current = 0.3 mA. All outputs unloaded. All inputs = VCC or GND.

5. VO, VIN = VCC or GND

Accelerator Series FPGAs – ACT 3 Family

Equivalent capacitance is calculated by measuring ICC active at a specified frequency and voltage for each circuit component of interest. Measurements have been made over a range of frequencies at a fixed value of VCC. Equivalent capacitance is frequency independent so that the results may be used over a wide range of operating conditions. Equivalent capacitance values are shown in Figure 2-10.

Item	CEQ Value
Modules (C <sub>EQM</sub> )	6.7
Input Buffers (C <sub>EQI</sub> )	7.2
Output Buffers (C <sub>EQO</sub> )	10.4
Routed Array Clock Buffer Loads (C <sub>EQCR</sub> )	1.6
Dedicated Clock Buffer Loads (C <sub>EQCD</sub> )	0.7
I/O Clock Buffer Loads (C <sub>EQCI)</sub>	0.9

To calculate the active power dissipated from the complete design, the switching frequency of each part of the logic must be known. EQ 5 shows a piece-wise linear summation over all components.

Power =VCC<sup>2</sup> \* [(m \* C<sub>EQM</sub> \* f<sub>m</sub>)<sub>modules</sub> + (n \* C<sub>EQI</sub> \* f<sub>n</sub>) inputs

+ ( $p * (C_{EQO} + C_L) * f_p$ )outputs

+ 0.5 \* (q1 \* C<sub>EQCR</sub> \* f<sub>q1</sub>)<sub>routed\_Clk1</sub> + (r1 \* fq1)<sub>routed\_Clk1</sub>

+ 0.5 \* (q2 \* C<sub>EQCR</sub> \* fq2)<sub>routed\_Clk2</sub>

+  $(r_2 * f_{q2})_{routed\_Clk2}$  + 0.5 \*  $(s_1 * C_{EQCD} * f_{s1})_{dedicated\_Clk}$ 

+ (s<sub>2</sub> \* C<sub>EQCI</sub> \* f<sub>s2</sub>)<sub>IO\_CIk</sub>]

Where: m = Number of logic modules switching at fm n = Number of input buffers switching at fn p = Number of output buffers switching at  $f_p$ q1 = Number of clock loads on the first routed array clock q2 = Number of clock loads on the second routed array clock  $r_1$  = Fixed capacitance due to first routed array clock r<sub>2</sub> = Fixed capacitance due to second routed array clock s<sub>1</sub> = Fixed number of clock loads on the dedicated array clock s2 = Fixed number of clock loads on the dedicated I/O clock C<sub>FOM</sub> = Equivalent capacitance of logic modules in pF C<sub>EQI</sub> = Equivalent capacitance of input buffers in pF C<sub>EOO</sub> = Equivalent capacitance of output buffers in pF C<sub>EOCR</sub> = Equivalent capacitance of routed array clock in pF C<sub>EQCD</sub> = Equivalent capacitance of dedicated array clock in pF C<sub>EOCI</sub> = Equivalent capacitance of dedicated I/O clock in pF C<sub>1</sub> = Output lead capacitance in pF f<sub>m</sub> = Average logic module switching rate in MHz fn = Average input buffer switching rate in MHz f<sub>p</sub> = Average output buffer switching rate in MHz  $f_{q1}$  = Average first routed array clock rate in MHz  $f_{\alpha 2}$  = Average second routed array clock rate in MHz f<sub>s1</sub> = Average dedicated array clock rate in MHz f<sub>s2</sub> = Average dedicated I/O clock rate in MHz

EQ 5

# **Determining Average Switching Frequency**

To determine the switching frequency for a design, you must have a detailed understanding of the data input values to the circuit. The following guidelines are meant to represent worst-case scenarios so that they can be generally used to predict the upper limits of power dissipation. These guidelines are as follows:

Tahle	2-13	Guidelines	for	Predicting	Power	Dissination
lable	2-13	Ouldennes	101	rieuleung	I OWEI	Dissipation

Data	Value
Logic Modules (m)	80% of modules
Inputs switching (n)	# inputs/4
Outputs switching (p)	# output/4
First routed array clock loads (q1)	40% of sequential modules
Second routed array clock loads (q2)	40% of sequential modules
Load capacitance (CL)	35 pF
Average logic module switching rate (fm)	F/10
Average input switching rate (fn)	F/5
Average output switching rate (fp)	F/10
Average first routed array clock rate (fq1)	F/2
Average second routed array clock rate (fq2)	F/2
Average dedicated array clock rate (fs1)	F
Average dedicated I/O clock rate (fs2)	F

## **Timing Derating**

ACT 3 devices are manufactured in a CMOS process. Therefore, device performance varies according to temperature, voltage, and process variations. Minimum timing parameters reflect maximum operating voltage, minimum operating temperature, and best-case processing. Maximum timing parameters reflect minimum operating voltage, maximum operating temperature, and worst-case processing.

#### Table 2-15 • Timing Derating Factor (Temperature and Voltage)

(Commercial Minimum/Maximum Specification) x	Indus	strial	Military		
	Min.	Max.	Min.	Max.	
	0.66	1.07	0.63	1.17	

#### Table 2-16 • Timing Derating Factor for Designs at Typical Temperature ( $T_J = 25^{\circ}C$ ) and Voltage (5.0 V)

(Commercial Maximum Specification) x	0.85

#### Table 2-17 • Temperature and Voltage Derating Factors

(normalized to Worst-Case Commercial, TJ = 4.75 V, 70°C)

	-55	-40	0	25	70	85	125
4.50	0.72	0.76	0.85	0.90	1.04	1.07	1.117
4.75	0.70	0.73	0.82	0.87	1.00	1.03	1.12
5.00	0.68	0.71	0.79	0.84	0.97	1.00	1.09
5.25	0.66	0.69	0.77	0.82	0.94	0.97	1.06
5.50	0.63	0.66	0.74	0.79	0.90	0.93	1.01



Note: This derating factor applies to all routing and propagation delays.





## A1440A, A14V40A Timing Characteristics

Table 2-26 • A1440A, A14V40A Worst-Case Commercial Conditions, VCC = 4.75 V, T<sub>J</sub> = 70°C<sup>1</sup>

Logic Module Propagation Delays <sup>2</sup>		-3 Speed <sup>3</sup> -2 Speed <sup>3</sup>		-1 Speed		Std. Speed		3.3 V Speed <sup>1</sup>		Units		
Parame	eter/Description	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t <sub>PD</sub>	Internal Array Module		2.0		2.3		2.6		3.0		3.9	ns
t <sub>CO</sub>	Sequential Clock to Q		2.0		2.3		2.6		3.0		3.9	ns
t <sub>CLR</sub>	Asynchronous Clear to Q		2.0		2.3		2.6		3.0		3.9	ns
Predict	ed Routing Delays <sup>4</sup>											•
t <sub>RD1</sub>	FO = 1 Routing Delay		0.9		1.0		1.1		1.3		1.7	ns
t <sub>RD2</sub>	FO = 2 Routing Delay		1.2		1.4		1.6		1.8		2.4	ns
t <sub>RD3</sub>	FO = 3 Routing Delay		1.4		1.6		1.8		2.1		2.8	ns
t <sub>RD4</sub>	FO = 4 Routing Delay		1.7		1.9		2.2		2.5		3.3	ns
t <sub>RD8</sub>	FO = 8 Routing Delay		2.8		3.2		3.6		4.2		5.5	ns
Logic N	Iodule Sequential Timing	-	-			-				-	-	
t <sub>SUD</sub>	Flip-Flop Data Input Setup	0.5		0.6		0.7		0.8		0.8		ns
t <sub>HD</sub>	Flip-Flop Data Input Hold	0.0		0.0		0.0		0.0		0.0		ns
t <sub>SUD</sub>	Latch Data Input Setup	0.5		0.6		0.7		0.8		0.8		ns
t <sub>HD</sub>	Latch Data Input Hold	0.0		0.0		0.0		0.0		0.0		ns
t <sub>WASYN</sub>	Asynchronous Pulse Width	1.9		2.4		3.2		3.8		4.8		ns
t <sub>WCLKA</sub>	Flip-Flop Clock Pulse Width	1.9		2.4		3.2		3.8		4.8		ns
t <sub>A</sub>	Flip-Flop Clock Input Period	4.0		5.0		6.8		8.0		10.0		ns
f <sub>MAX</sub>	Flip-Flop Clock Frequency		250		200		150		125		100	MHz

Notes:

1. VCC = 3.0 V for 3.3 V specifications.

2. For dual-module macros, use  $t_{PD} + t_{RD1} + t_{PDn} + t_{CO} + t_{RD1} + t_{PDn}$  or  $t_{PD1} + t_{RD1} + t_{SUD}$ , whichever is appropriate.

3. The –2 and –3 speed grades have been discontinued. Refer to PDN 0104, PDN 0203, PDN 0604, and PDN 1004 at http://www.microsemi.com/soc/support/notifications/default.aspx#pdn.

4. Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual worst-case performance. Post-route timing is based on actual routing delay measurements performed on the device prior to shipment.



## A1440A, A14V40A Timing Characteristics (continued)

Table 2-28 • A1440A, A14V40A Worst-Case Commercial Conditions, VCC = 4.75 V, T<sub>J</sub> = 70°C

I/O Module – TTL Output Timing <sup>1</sup>		-3 Sp	Speed <sup>2</sup> –2 Speed <sup>2</sup>		beed <sup>2</sup>	-1 Speed		Std. Speed		d 3.3 V Speed <sup>1</sup>		Units
Parame	eter/Description	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t <sub>DHS</sub>	Data to Pad, High Slew		5.0		5.6		6.4		7.5		9.8	ns
t <sub>DLS</sub>	Data to Pad, Low Slew		8.0		9.0		10.2		12.0		15.6	ns
t <sub>ENZHS</sub>	Enable to Pad, Z to H/L, High Slew		4.0		4.5		5.1		6.0		7.8	ns
t <sub>ENZLS</sub>	Enable to Pad, Z to H/L, Low Slew		7.4		8.3		9.4		11.0		14.3	ns
t <sub>ENHSZ</sub>	Enable to Pad, H/L to Z, High Slew		7.4		8.3		9.4		11.0		14.3	ns
t <sub>ENLSZ</sub>	Enable to Pad, H/L to Z, Low Slew		7.4		8.3		9.4		11.0		14.3	ns
t <sub>CKHS</sub>	IOCLK Pad to Pad H/L, High Slew		8.5		8.5		9.5		11.0		14.3	ns
t <sub>CKLS</sub>	IOCLK Pad to Pad H/L, Low Slew		11.3		11.3		13.5		15.0		19.5	ns
d <sub>TLHHS</sub>	Delta Low to High, High Slew		0.02		0.02		0.03		0.03		0.04	ns/pF
d <sub>TLHLS</sub>	Delta Low to High, Low Slew		0.05		0.05		0.06		0.07		0.09	ns/pF
d <sub>THLHS</sub>	Delta High to Low, High Slew		0.04		0.04		0.04		0.05		0.07	ns/pF
d <sub>THLLS</sub>	Delta High to Low, Low Slew		0.05		0.05		0.06		0.07		0.09	ns/pF
I/O Mod	dule – CMOS Output Timing <sup>1</sup>			-					-	-		
t <sub>DHS</sub>	Data to Pad, High Slew		6.2		7.0		7.9		9.3		12.1	ns
t <sub>DLS</sub>	Data to Pad, Low Slew		11.7		13.1		14.9		17.5		22.8	ns
t <sub>ENZHS</sub>	Enable to Pad, Z to H/L, High Slew		5.2		5.9		6.6		7.8		10.1	ns
t <sub>ENZLS</sub>	Enable to Pad, Z to H/L, Low Slew		8.9		10.0		11.3		13.3		17.3	ns
t <sub>ENHSZ</sub>	Enable to Pad, H/L to Z, High Slew		7.4		8.3		9.4		11.0		14.3	ns
t <sub>ENLSZ</sub>	Enable to Pad, H/L to Z, Low Slew		7.4		8.3		9.4		11.0		14.3	ns
t <sub>CKHS</sub>	IOCLK Pad to Pad H/L, High Slew		9.0		9.0		10.1		11.8		14.3	ns
t <sub>CKLS</sub>	IOCLK Pad to Pad H/L, Low Slew		13.0		13.0		15.6		17.3		22.5	ns
d <sub>TLHHS</sub>	Delta Low to High, High Slew		0.04		0.04		0.05		0.06		0.08	ns/pF
d <sub>TLHLS</sub>	Delta Low to High, Low Slew		0.07		0.08		0.09		0.11		0.14	ns/pF
d <sub>THLHS</sub>	Delta High to Low, High Slew		0.03		0.03		0.03		0.04		0.05	ns/pF
d <sub>THLLS</sub>	Delta High to Low, Low Slew		0.04		0.04		0.04		0.05		0.07	ns/pF

Notes:

1. Delays based on 35 pF loading.

2. The –2 and –3 speed grades have been discontinued. Refer to PDN 0104, PDN 0203, PDN 0604, and PDN 1004 at http://www.microsemi.com/soc/support/notifications/default.aspx#pdn.



# **Pin Descriptions**

#### CLKA Clock A (Input)

Clock input for clock distribution networks. The Clock input is buffered prior to clocking the logic modules. This pin can also be used as an I/O.

#### CLKB Clock B (Input)

Clock input for clock distribution networks. The Clock input is buffered prior to clocking the logic modules. This pin can also be used as an I/O.

#### GND Ground

LOW supply voltage.

#### HCLK Dedicated (Hard-wired) Array Clock (Input)

Clock input for sequential modules. This input is directly wired to each S-Module and offers clock speeds independent of the number of S-Modules being driven. This pin can also be used as an I/O.

#### I/O Input/Output (Input, Output)

The I/O pin functions as an input, output, three-state, or bidirectional buffer. Input and output levels are compatible with standard TTL and CMOS specifications. Unused I/O pins are tristated by the Designer Series software.

#### IOCLK Dedicated (Hard-wired) I/O Clock (Input)

Clock input for I/O modules. This input is directly wired to each I/O module and offers clock speeds independent of the number of I/O modules being driven. This pin can also be used as an I/O.

#### IOPCL Dedicated (Hard-wired) I/O Preset/Clear (Input)

Input for I/O preset or clear. This global input is directly wired to the preset and clear inputs of all I/O registers. This pin functions as an I/O when no I/O preset or clear macros are used.

#### MODE Mode (Input)

The MODE pin controls the use of diagnostic pins (DCLK, PRA, PRB, SDI). When the MODE pin is HIGH, the special functions are active. When the MODE pin is LOW, the pins function as I/Os. To provide Actionprobe capability, the MODE pin should be terminated to GND through a 10K resistor so that the MODE pin can be pulled high when required.

#### NC No Connection

This pin is not connected to circuitry within the device.

#### PRA Probe A (Output)

The Probe A pin is used to output data from any user-defined design node within the device. This independent diagnostic pin can be used in conjunction with the Probe B pin to allow real-time diagnostic output of any signal path within the device. The Probe A pin can be used as a user-defined I/O when debugging has been completed. The pin's probe capabilities can be permanently disabled to protect programmed design confidentiality. PRA is accessible when the MODE pin is HIGH. This pin functions as an I/O when the MODE pin is LOW.

#### PRB Probe B (Output)

The Probe B pin is used to output data from any user-defined design node within the device. This independent diagnostic pin can be used in conjunction with the Probe A pin to allow real-time diagnostic output of any signal path within the device. The Probe B pin can be used as a user-defined I/O when debugging has been completed. The pin's probe capabilities can be permanently disabled to protect programmed design confidentiality. PRB is accessible when the MODE pin is HIGH. This pin functions as an I/O when the MODE pin is LOW.

#### SDI Serial Data Input (Input)

Serial data input for diagnostic probe and device programming. SDI is active when the MODE pin is HIGH. This pin functions as an I/O when the MODE pin is LOW.



Package Pin Assignments

# **TQ176**



Note: This is the top view.

## Note

For Package Manufacturing and Environmental information, visit the Resource Center at http://www.microsemi.com/soc/products/solutions/package/docs.aspx



Package Pin Assignments

# VQ100



Note: This is the top view.

#### Note

For Package Manufacturing and Environmental information, visit the Resource Center at http://www.microsemi.com/soc/products/solutions/package/docs.aspx

Accelerator Series FPGAs - ACT 3 Family

CQ132			CQ132
Pin Number	A1425 Function	Pin Number	A1425 Function
1	NC	67	NC
2	GND	74	GND
3	SDI, I/O	75	VCC
9	MODE	78	VCC
10	GND	89	VCC
11	VCC	90	GND
22	VCC	91	VCC
26	GND	92	GND
27	VCC	98	IOCLK, I/O
34	NC	99	NC
36	GND	100	NC
42	GND	101	GND
43	VCC	106	GND
48	PRB, I/O	107	VCC
50	HCLK, I/O	116	CLKA, I/O
58	GND	117	CLKB, I/O
59	VCC	118	PRA, I/O
63	SDO	122	GND
64	IOPCL, I/O	123	VCC
65	GND	131	DCLK, I/O
66	NC	132	NC

- 1. All unlisted pin numbers are user I/Os.
- 2. NC denotes no connection.
- 3. MODE should be terminated to GND through a 10K resistor to enable Actionprobe usage; otherwise it can be terminated directly to GND.



Package Pin Assignments

# CQ196



Note: This is the top view.

## Note

For Package Manufacturing and Environmental information, visit the Resource Center at http://www.microsemi.com/soc/products/solutions/package/docs.aspx

Accelerator Series FPGAs – ACT 3 Family

BG225					
A1460 Function	Location				
CLKA or I/O	C8				
CLKB or I/O	B8				
DCLK or I/O	B2				
GND	A1, A15, D15, F8, G7, G8, G9, H6, H7, H8, H9, H10, J7, J8, J9, K8, P2, R15				
HCLK or I/O	P9				
IOCLK or I/O	B14				
IOPCL or I/O	P14				
MODE	D1				
NC	A11, B5, B7, D8, D12, F6, F11, H1, H12, H14, K11, L1, L13, N8, P5, R1, R8, R11, R14				
PRA or I/O	A7				
PRB or I/O	L7				
SDI or I/O	D4				
SDO	N13				
VCC	A8, B12, D5, D14, E3, E8, E13, H2, H3, H11, H15, K4, L2, L12, M8, M15, P4, P8, R13				

- 1. All unlisted pin numbers are user I/Os.
- 2. NC denotes no connection.
- 3. MODE should be terminated to GND through a 10K resistor to enable Actionprobe usage; otherwise it can be terminated directly to GND.
- 4. The BG225 package has been discontinued.

Accelerator Series FPGAs – ACT 3 Family

	BG313
A14100, A14V100 Function	Location
CLKA or I/O	J13
CLKB or I/O	G13
DCLK or I/O	B2
GND	A1, A25, AD2, AE25, J21, L13, M12, M14, N11, N13, N15, P12, P14, R13
HCLK or I/O	T14
IOCLK or I/O	B24
IOPCL or I/O	AD24
MODE	G3
NC	A3, A13, A23, AA5, AA9, AA23, AB2, AB4, AB20, AC13, AC25, AD22, AE1, AE21, B14, C5, C25, D4, D24, E3, E21, F6, F10, F16, G1, G25, H18, H24, J1, J7, J25, K12, L15, L17, M6, N1, N5, N7, N21, N23, P20, R11, T6, T8, U9, U13, U21, V16, W7, Y20, Y24
PRA or I/O	H12
PRB or I/O	AD12
SDI or I/O	C1
SDO	AE23
VCC	AB18, AD6, AE13, C13, C19, E13, G9, H22, K8, K20, M16, N3, N9, N25, U5, W13, V2, V22, V24

- 1. All unlisted pin numbers are user I/Os.
- 2. NC denotes no connection.
- 3. MODE should be terminated to GND through a 10K resistor to enable Actionprobe usage; otherwise it can be terminated directly to GND.

Accelerator Series FPGAs – ACT 3 Family

PG257					
A14100 Function	Location				
CLKA or I/O	L4				
CLKB or I/O	L5				
DCLK or I/O	E4				
GND	B16, C4, D4, D10, D16, E11, J5, K4, K16, L15, R4, T4, T10, T16, T17, X7				
HCLK or I/O	J16				
IOCLK or I/O	Т5				
IOPCL or I/O	R16				
MODE	A5				
NC	E5				
PRA or I/O	J1				
PRB or I/O	J17				
SDI or I/O	B4				
SDO	R17				
VCC	C3, C10, C13, C17, K3, K17, V3, V7, V10, V17, X14				

- 1. All unlisted pin numbers are user I/Os.
- 2. NC denotes no connection.
- 3. MODE should be terminated to GND through a 10K resistor to enable Actionprobe usage; otherwise it can be terminated directly to GND.

# **Datasheet Categories**

## Categories

In order to provide the latest information to designers, some datasheet parameters are published before data has been fully characterized from silicon devices. The data provided for a given device is designated as either "Product Brief," "Advance," "Preliminary," or "Production." The definitions of these categories are as follows:

## **Product Brief**

The product brief is a summarized version of a datasheet (advance or production) and contains general product information. This document gives an overview of specific device and family information.

## Advance

This version contains initial estimated information based on simulation, other products, devices, or speed grades. This information can be used as estimates, but not for production. This label only applies to the DC and Switching Characteristics chapter of the datasheet and will only be used when the data has not been fully characterized.

## Preliminary

The datasheet contains information based on simulation and/or initial characterization. The information is believed to be correct, but changes are possible.

## Production

This version contains information that is considered to be final.

## **Export Administration Regulations (EAR)**

The products described in this document are subject to the Export Administration Regulations (EAR). They could require an approved export license prior to export from the United States. An export includes release of product or disclosure of technology to a foreign national inside or outside the United States.

# Safety Critical, Life Support, and High-Reliability Applications Policy

The products described in this advance status document may not have completed the Microsemi qualification process. Products may be amended or enhanced during the product introduction and qualification process, resulting in changes in device functionality or performance. It is the responsibility of each customer to ensure the fitness of any product (but especially a new product) for a particular purpose, including appropriateness for safety-critical, life-support, and other high-reliability applications. Consult the Microsemi SoC Products Group Terms and Conditions for specific liability exclusions relating to life-support applications. A reliability report covering all of the SoC Products Group's products is available at http://www.microsemi.com/soc/documents/ORT\_Report.pdf. Microsemi also offers a variety of enhanced qualification and lot acceptance screening procedures. Contact your local sales office for additional reliability information.