Welcome to E-XFL.COM

## Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

## Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

| Details | |
|---|---|
| Product Status | Obsolete |
| Number of LABs/CLBs | 848 |
| Number of Logic Elements/Cells | - |
| Total RAM Bits | - |
| Number of I/O | 151 |
| Number of Gates | 6000 |
| Voltage - Supply | 4.5V ~ 5.5V |
| Mounting Type | Surface Mount |
| Operating Temperature | 0°C ~ 70°C (TA) |
| Package / Case | 176-LQFP |
| Supplier Device Package | 176-TQFP (24x24) |
| Purchase URL | https://www.e-xfl.com/product-detail/microsemi/a1460a-tqg176c |

# Plastic Device Resources

| Device Series | Logic Modules | Gates | User I/Os | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | PL84 | PQ100 | PQ160 | PQ/RQ208 | VQ100 | TQ176 | BG225* | BG313 |
| A1415 | 200 | 1500 | 70 | 80 | – | – | 80 | – | – | – |
| A1425 | 310 | 2500 | 70 | 80 | 100 | – | 83 | – | – | – |
| A1440 | 564 | 4000 | 70 | – | 131 | – | 83 | 140 | – | – |
| A1460 | 848 | 6000 | – | – | 131 | 167 | – | 151 | 168 | – |
| A14100 | 1377 | 10000 | – | – | – | 175 | – | – | – | 228 |

*Note: *Discontinued*

# Hermetic Device Resources

| Device Series | Logic Modules | Gates | User I/Os | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | PG100* | PG133* | PG175* | PG207 | PG257 | CQ132 | CQ196 | CQ256 |
| A1415 | 200 | 1500 | 80 | – | – | – | – | – | – | – |
| A1425 | 310 | 2500 | – | 100 | – | – | – | 100 | – | – |
| A1440 | 564 | 4000 | – | – | 140 | – | – | – | – | – |
| A1460 | 848 | 6000 | – | – | – | 168 | – | – | 168 | – |
| A14100 | 1377 | 10000 | – | – | – | – | 228 | – | – | 228 |

*Note: *Discontinued*

Contact your local Microsemi SoC Products Group (formerly Actel) representative for device availability:
http://www.microsemi.com/soc/contact/default.aspx.

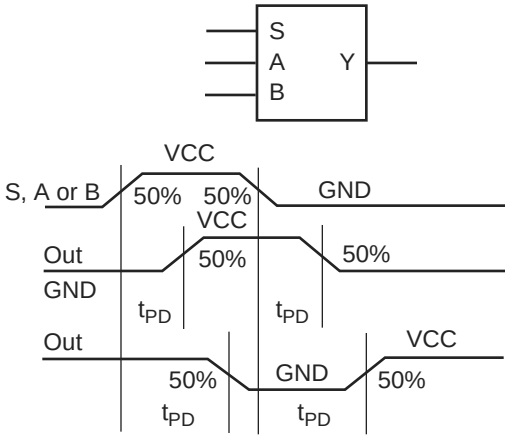



***Figure 2-14 •*** **Module Delays**

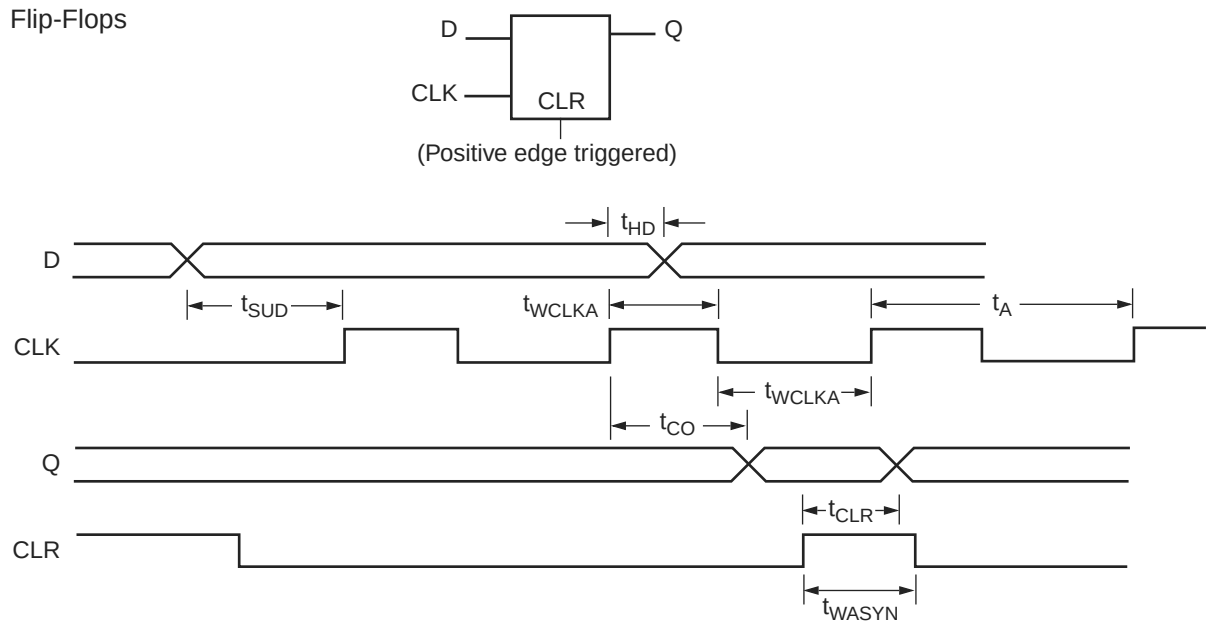



***Figure 2-15 •*** **Sequential Module Timing Characteristics**

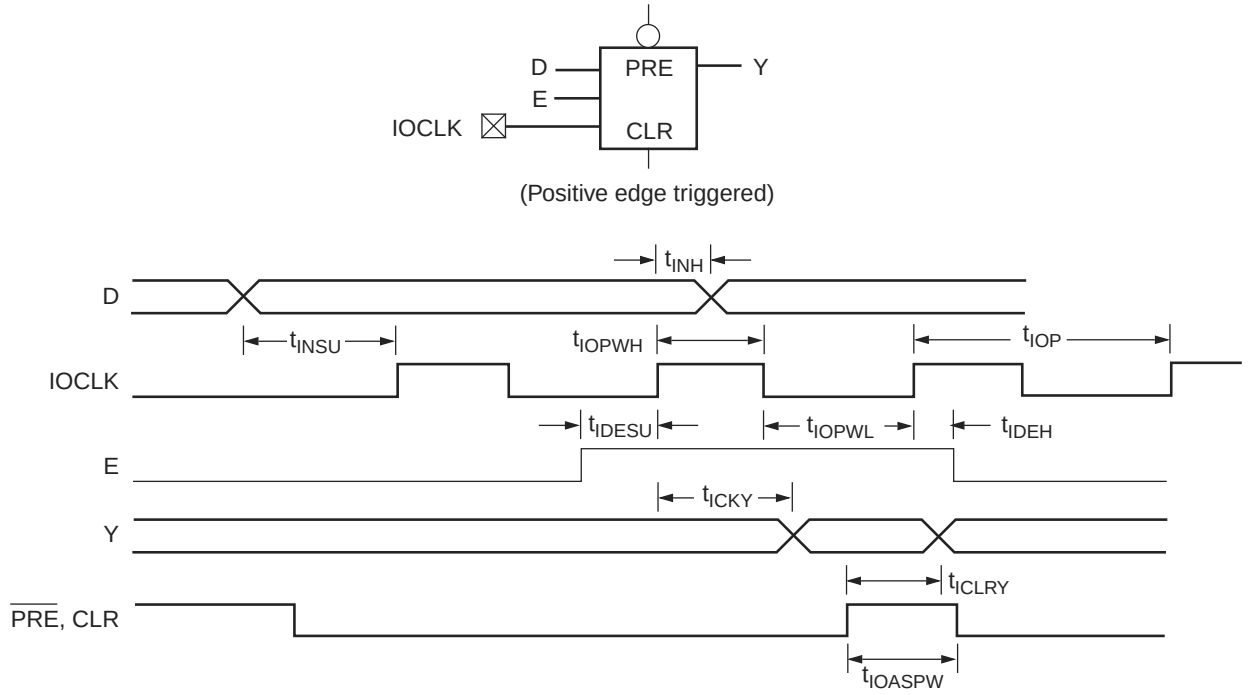



***Figure 2-16 •*** **I/O Module: Sequential Input Timing Characteristics**

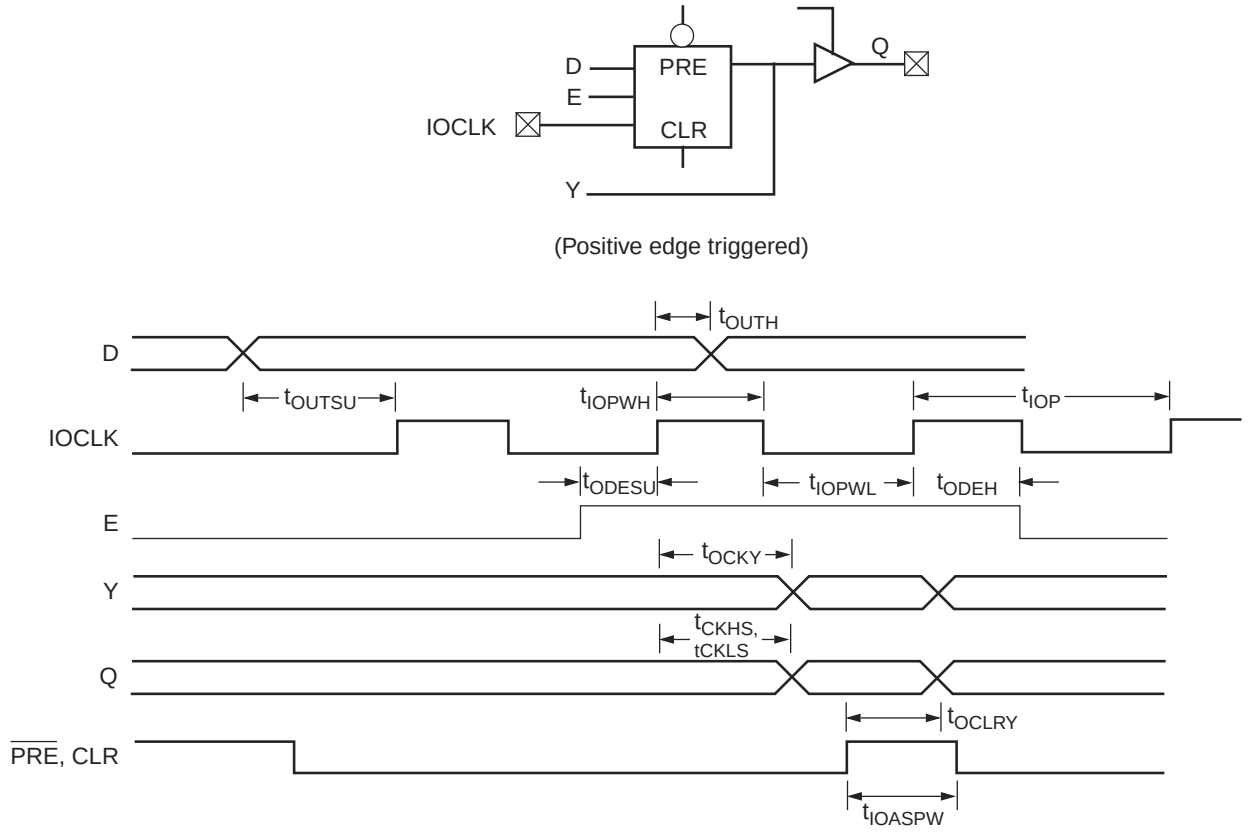



***Figure 2-17 •*** **I/O Module: Sequential Output Timing Characteristics**

## A14100A, A14V100A Timing Characteristics

**Table 2-34 • A14100A, A14V100A Worst-Case Commercial Conditions, VCC = 4.75 V, $T_J$ = 70°C[1]**

| Logic Module Propagation Delays[2] | | –3 Speed[3] | | –2 Speed [3] | | –1 Speed | | Std. Speed | | 3.3 V Speed[1] | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Parameter/Description | | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | |
| $t_{PD}$ | Internal Array Module | | 2.0 | | 2.3 | | 2.6 | | 3.0 | | 3.9 | ns |
| $t_{CO}$ | Sequential Clock to Q | | 2.0 | | 2.3 | | 2.6 | | 3.0 | | 3.9 | ns |
| $t_{CLR}$ | Asynchronous Clear to Q | | 2.0 | | 2.3 | | 2.6 | | 3.0 | | 3.9 | ns |
| **Predicted Routing Delays[4]** | | | | | | | | | | | | |
| $t_{RD1}$ | FO = 1 Routing Delay | | 0.9 | | 1.0 | | 1.1 | | 1.3 | | 1.7 | ns |
| $t_{RD2}$ | FO = 2 Routing Delay | | 1.2 | | 1.4 | | 1.6 | | 1.8 | | 2.4 | ns |
| $t_{RD3}$ | FO = 3 Routing Delay | | 1.4 | | 1.6 | | 1.8 | | 2.1 | | 2.8 | ns |
| $t_{RD4}$ | FO = 4 Routing Delay | | 1.7 | | 1.9 | | 2.2 | | 2.5 | | 3.3 | ns |
| $t_{RD8}$ | FO = 8 Routing Delay | | 2.8 | | 3.2 | | 3.6 | | 4.2 | | 5.5 | ns |
| **Logic Module Sequential Timing** | | | | | | | | | | | | |
| $t_{SUD}$ | Flip-Flop Data Input Setup | 0.5 | | 0.6 | | 0.8 | | 0.8 | | 0.8 | | ns |
| $t_{HD}$ | Flip-Flop Data Input Hold | 0.0 | | 0.0 | | 0.5 | | 0.5 | | 0.5 | | ns |
| $t_{SUD}$ | Latch Data Input Setup | 0.5 | | 0.6 | | 0.8 | | 0.8 | | 0.8 | | ns |
| $t_{HD}$ | Latch Data Input Hold | 0.0 | | 0.0 | | 0.5 | | 0.5 | | 0.5 | | ns |
| $t_{WASYN}$ | Asynchronous Pulse Width | 2.4 | | 3.2 | | 3.8 | | 4.8 | | 6.5 | | ns |
| $t_{WCLKA}$ | Flip-Flop Clock Pulse Width | 2.4 | | 3.2 | | 3.8 | | 4.8 | | 6.5 | | ns |
| $t_A$ | Flip-Flop Clock Input Period | 5.0 | | 6.8 | | 8.0 | | 10.0 | | 13.4 | | ns |
| $f_{MAX}$ | Flip-Flop Clock Frequency | | 200 | | 150 | | 125 | | 100 | | 75 | MHz |

*Notes:*

1. *VCC = 3.0 V for 3.3 V specifications.*
2. *For dual-module macros, use $t_{PD} + t_{RD1} + t_{PDn} + t_{CO} + t_{RD1} + t_{PDn}$ or $t_{PD1} + t_{RD1} + t_{SUD}$, whichever is appropriate.*
3. *The –2 and –3 speed grades have been discontinued. Refer to PDN 0104, PDN 0203, PDN 0604, and PDN 1004 at http://www.microsemi.com/soc/support/notifications/default.aspx#pdn.*
4. *Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual worst-case performance. Post-route timing is based on actual routing delay measurements performed on the device prior to shipment.*

# Pin Descriptions

**CLKA Clock A (Input)**

Clock input for clock distribution networks. The Clock input is buffered prior to clocking the logic modules. This pin can also be used as an I/O.

**CLKB Clock B (Input)**

Clock input for clock distribution networks. The Clock input is buffered prior to clocking the logic modules. This pin can also be used as an I/O.

**GND Ground**

LOW supply voltage.

**HCLK Dedicated (Hard-wired) Array Clock (Input)**

Clock input for sequential modules. This input is directly wired to each S-Module and offers clock speeds independent of the number of S-Modules being driven. This pin can also be used as an I/O.

**I/O Input/Output (Input, Output)**

The I/O pin functions as an input, output, three-state, or bidirectional buffer. Input and output levels are compatible with standard TTL and CMOS specifications. Unused I/O pins are tristated by the Designer Series software.

**IOCLK Dedicated (Hard-wired) I/O Clock (Input)**

Clock input for I/O modules. This input is directly wired to each I/O module and offers clock speeds independent of the number of I/O modules being driven. This pin can also be used as an I/O.

**IOPCL Dedicated (Hard-wired) I/O Preset/Clear (Input)**

Input for I/O preset or clear. This global input is directly wired to the preset and clear inputs of all I/O registers. This pin functions as an I/O when no I/O preset or clear macros are used.

**MODE Mode (Input)**

The MODE pin controls the use of diagnostic pins (DCLK, PRA, PRB, SDI). When the MODE pin is HIGH, the special functions are active. When the MODE pin is LOW, the pins function as I/Os. To provide Actionprobe capability, the MODE pin should be terminated to GND through a 10K resistor so that the MODE pin can be pulled high when required.

**NC No Connection**

This pin is not connected to circuitry within the device.

**PRA Probe A (Output)**

The Probe A pin is used to output data from any user-defined design node within the device. This independent diagnostic pin can be used in conjunction with the Probe B pin to allow real-time diagnostic output of any signal path within the device. The Probe A pin can be used as a user-defined I/O when debugging has been completed. The pin's probe capabilities can be permanently disabled to protect programmed design confidentiality. PRA is accessible when the MODE pin is HIGH. This pin functions as an I/O when the MODE pin is LOW.

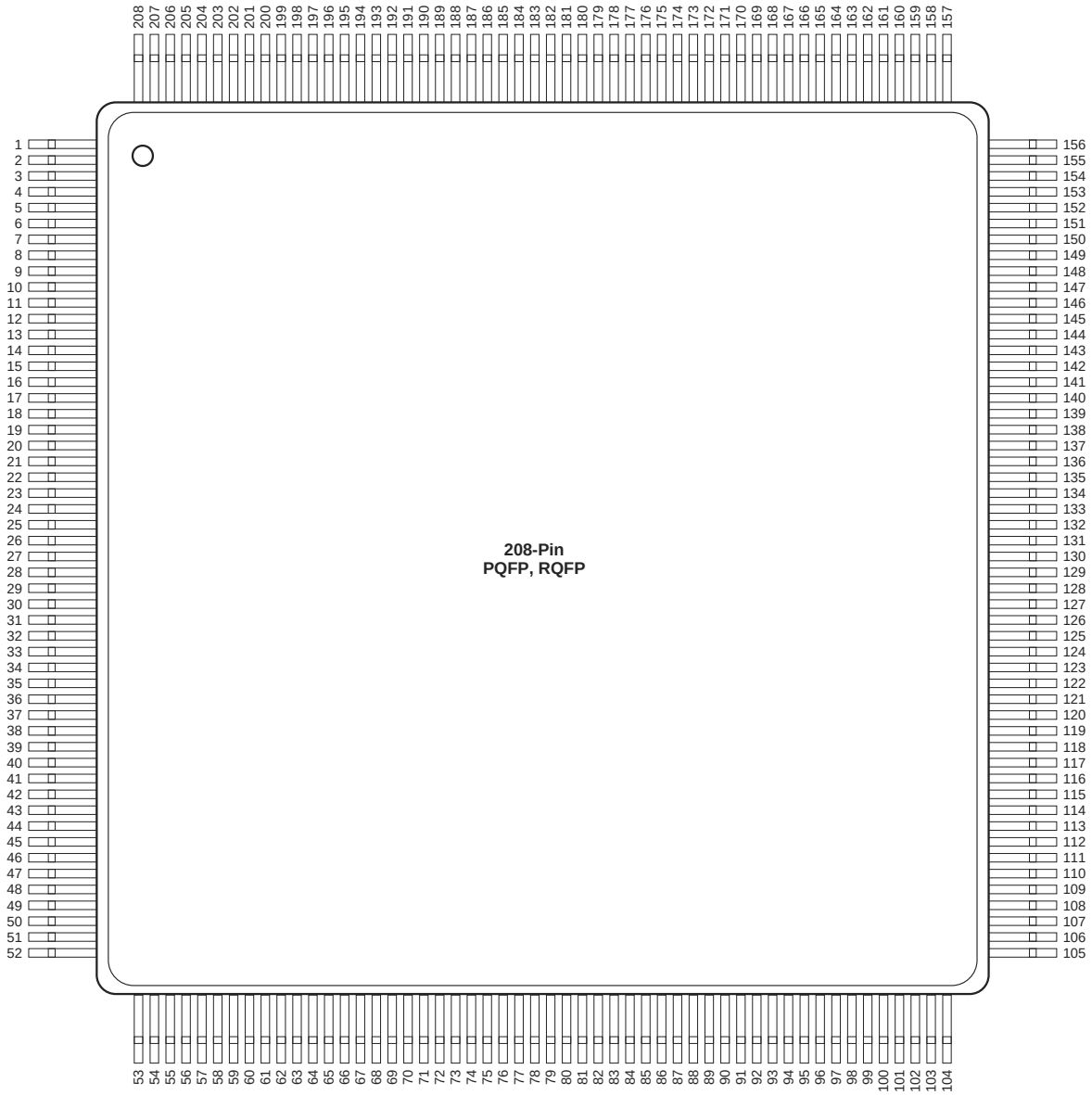
**PRB Probe B (Output)**

The Probe B pin is used to output data from any user-defined design node within the device. This independent diagnostic pin can be used in conjunction with the Probe A pin to allow real-time diagnostic output of any signal path within the device. The Probe B pin can be used as a user-defined I/O when debugging has been completed. The pin's probe capabilities can be permanently disabled to protect programmed design confidentiality. PRB is accessible when the MODE pin is HIGH. This pin functions as an I/O when the MODE pin is LOW.

**SDI Serial Data Input (Input)**

Serial data input for diagnostic probe and device programming. SDI is active when the MODE pin is HIGH. This pin functions as an I/O when the MODE pin is LOW.

# PQ208, RQ208

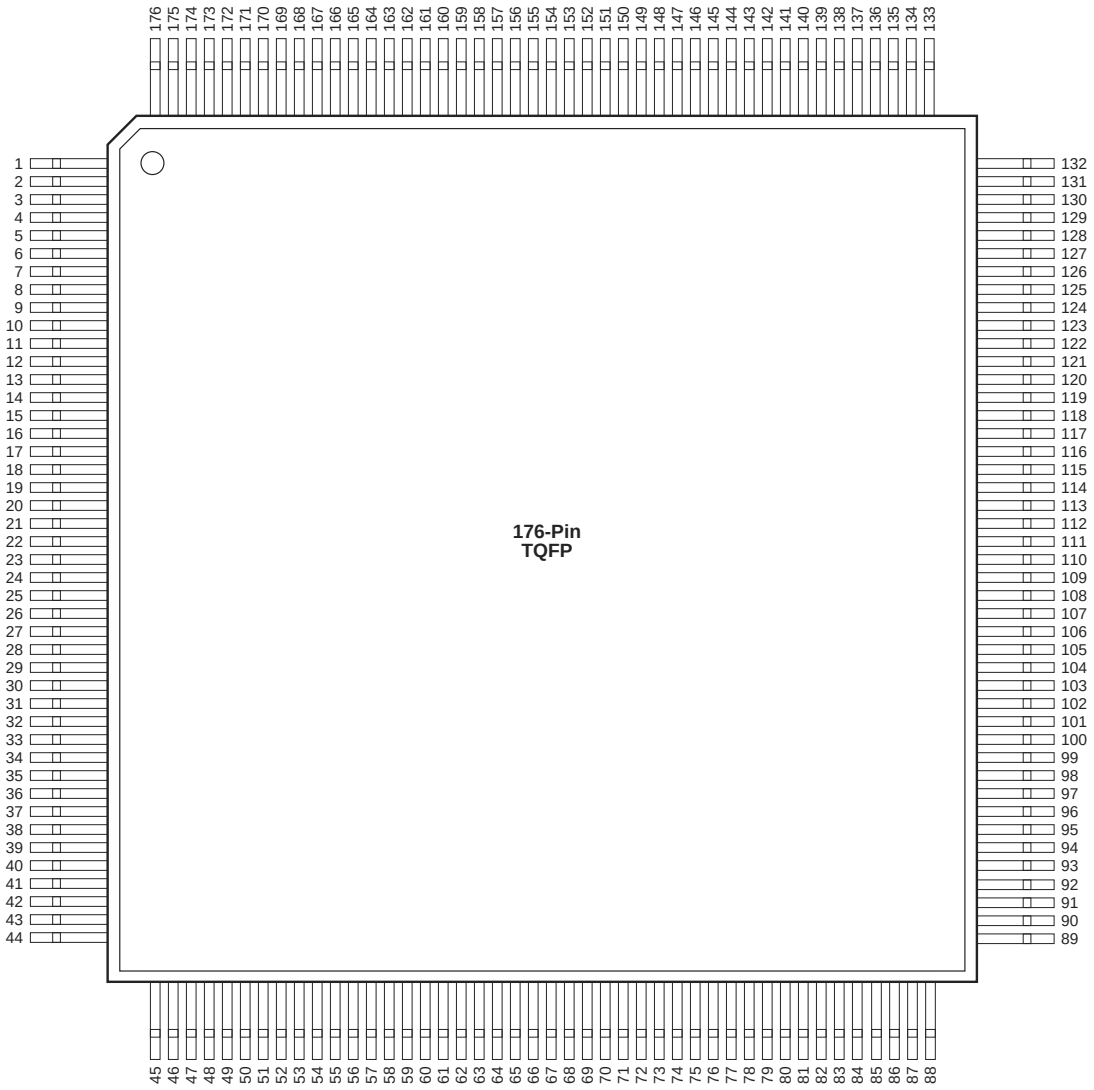



*Note: This is the top view of the package*

## Note

For Package Manufacturing and Environmental information, visit the Resource Center at http://www.microsemi.com/soc/products/solutions/package/docs.aspx

# TQ176

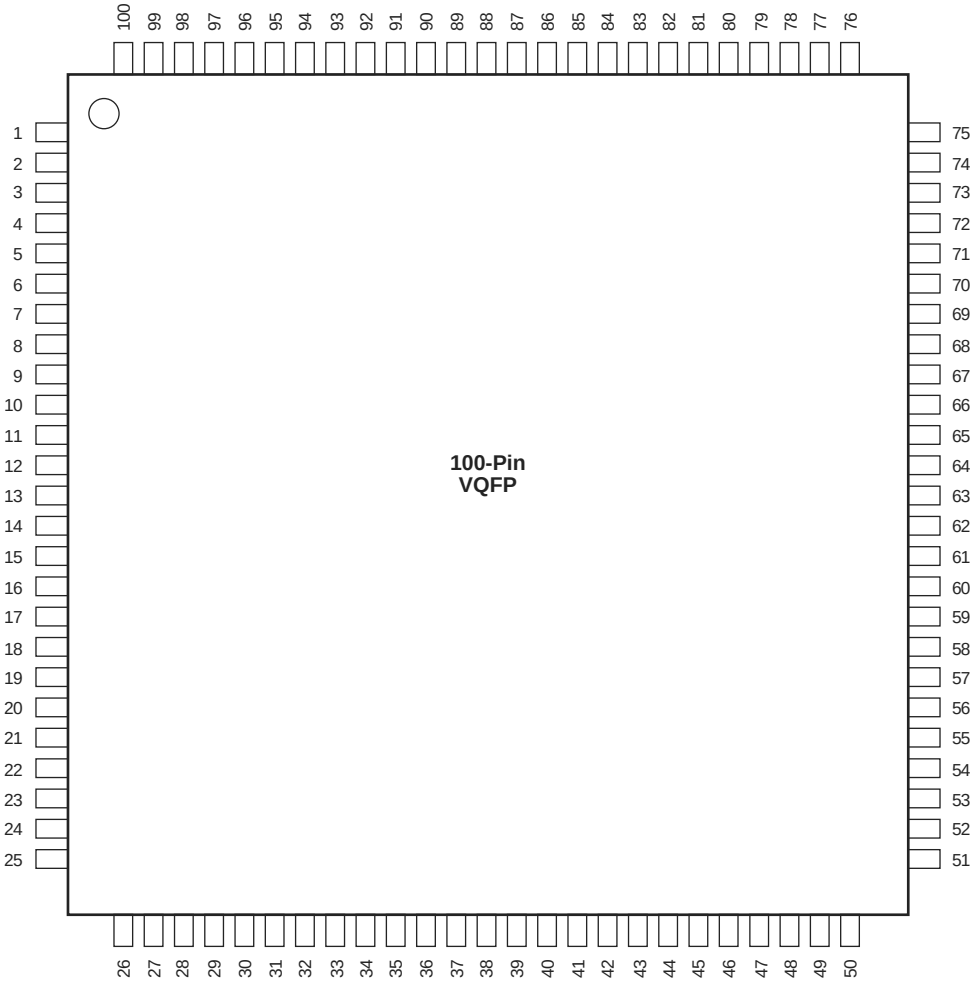



*Note: This is the top view.*

## Note

For Package Manufacturing and Environmental information, visit the Resource Center at http://www.microsemi.com/soc/products/solutions/package/docs.aspx

# VQ100

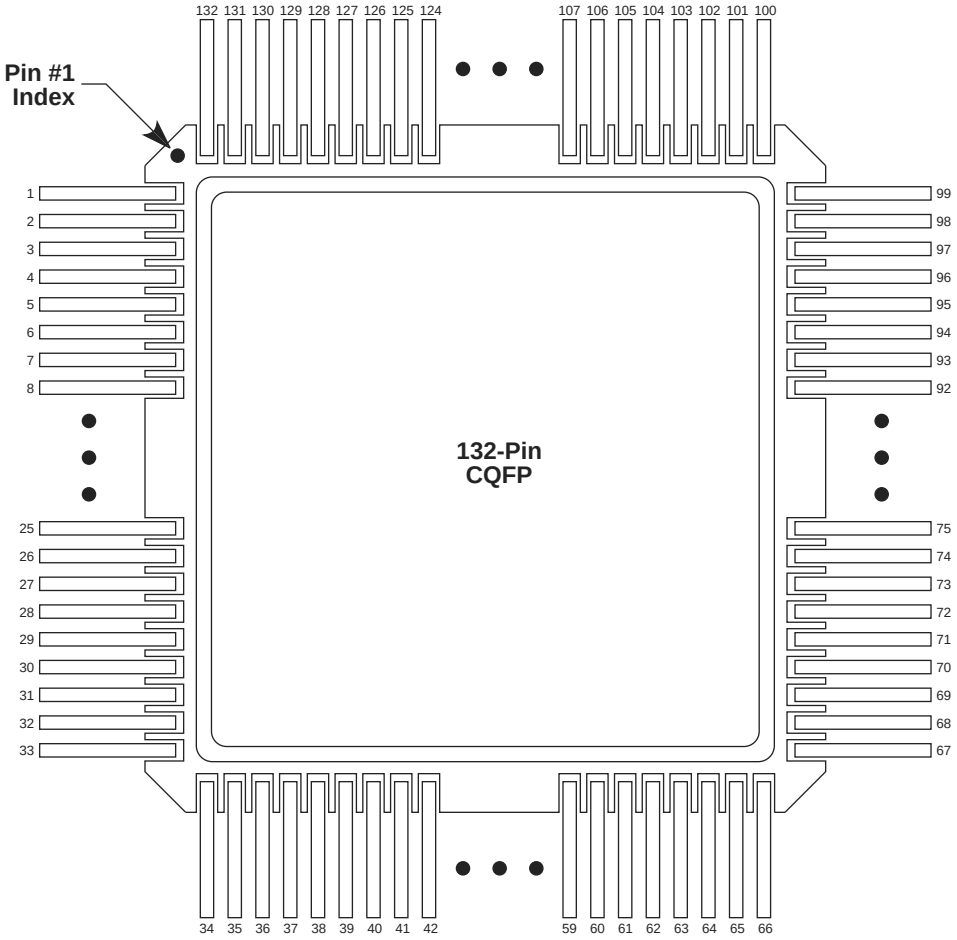



*Note: This is the top view.*

## Note

For Package Manufacturing and Environmental information, visit the Resource Center at http://www.microsemi.com/soc/products/solutions/package/docs.aspx

# CQ132




*Note: This is the top view*

## Note

For Package Manufacturing and Environmental information, visit the Resource Center at http://www.microsemi.com/soc/products/solutions/package/docs.aspx

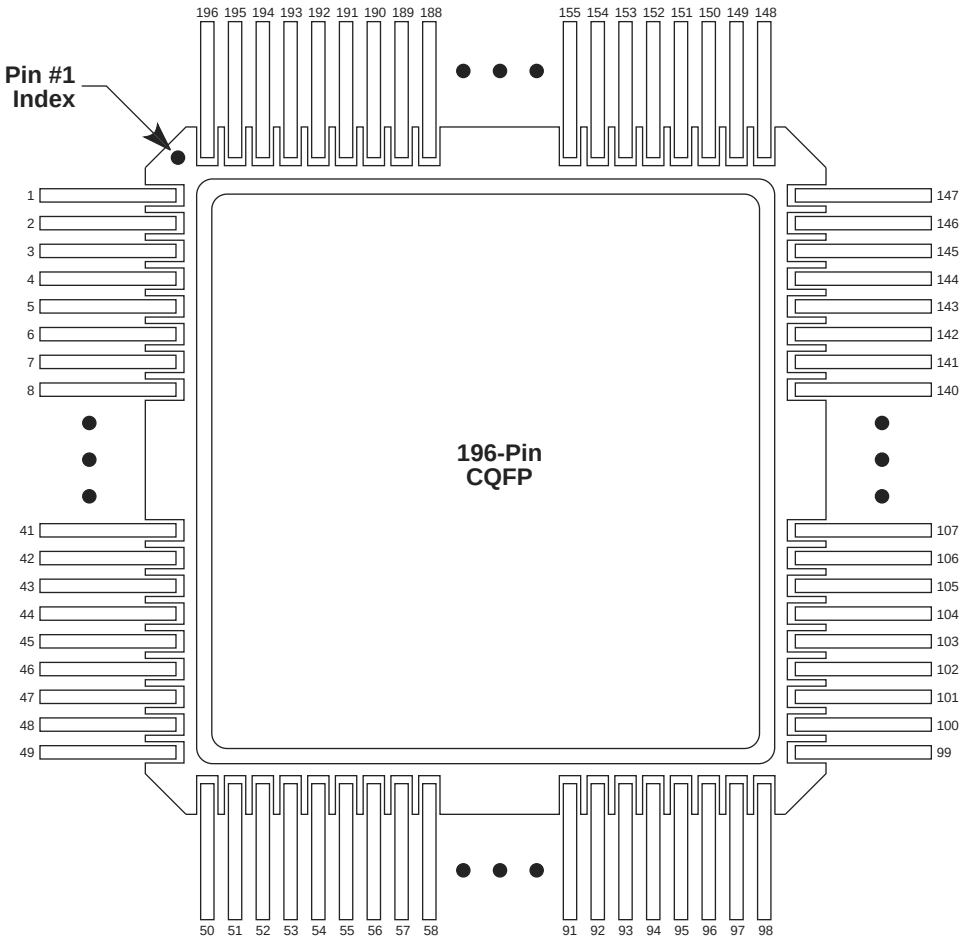
| CQ132 | |
|---|---|
| **Pin Number** | **A1425 Function** |
| 1 | NC |
| 2 | GND |
| 3 | SDI, I/O |
| 9 | MODE |
| 10 | GND |
| 11 | VCC |
| 22 | VCC |
| 26 | GND |
| 27 | VCC |
| 34 | NC |
| 36 | GND |
| 42 | GND |
| 43 | VCC |
| 48 | PRB, I/O |
| 50 | HCLK, I/O |
| 58 | GND |
| 59 | VCC |
| 63 | SDO |
| 64 | IOPCL, I/O |
| 65 | GND |
| 66 | NC |

| CQ132 | |
|---|---|
| **Pin Number** | **A1425 Function** |
| 67 | NC |
| 74 | GND |
| 75 | VCC |
| 78 | VCC |
| 89 | VCC |
| 90 | GND |
| 91 | VCC |
| 92 | GND |
| 98 | IOCLK, I/O |
| 99 | NC |
| 100 | NC |
| 101 | GND |
| 106 | GND |
| 107 | VCC |
| 116 | CLKA, I/O |
| 117 | CLKB, I/O |
| 118 | PRA, I/O |
| 122 | GND |
| 123 | VCC |
| 131 | DCLK, I/O |
| 132 | NC |

*Notes:*

1. All unlisted pin numbers are user I/Os.
2. NC denotes no connection.
3. MODE should be terminated to GND through a 10K resistor to enable Actionprobe usage; otherwise it can be terminated directly to GND.

# CQ196

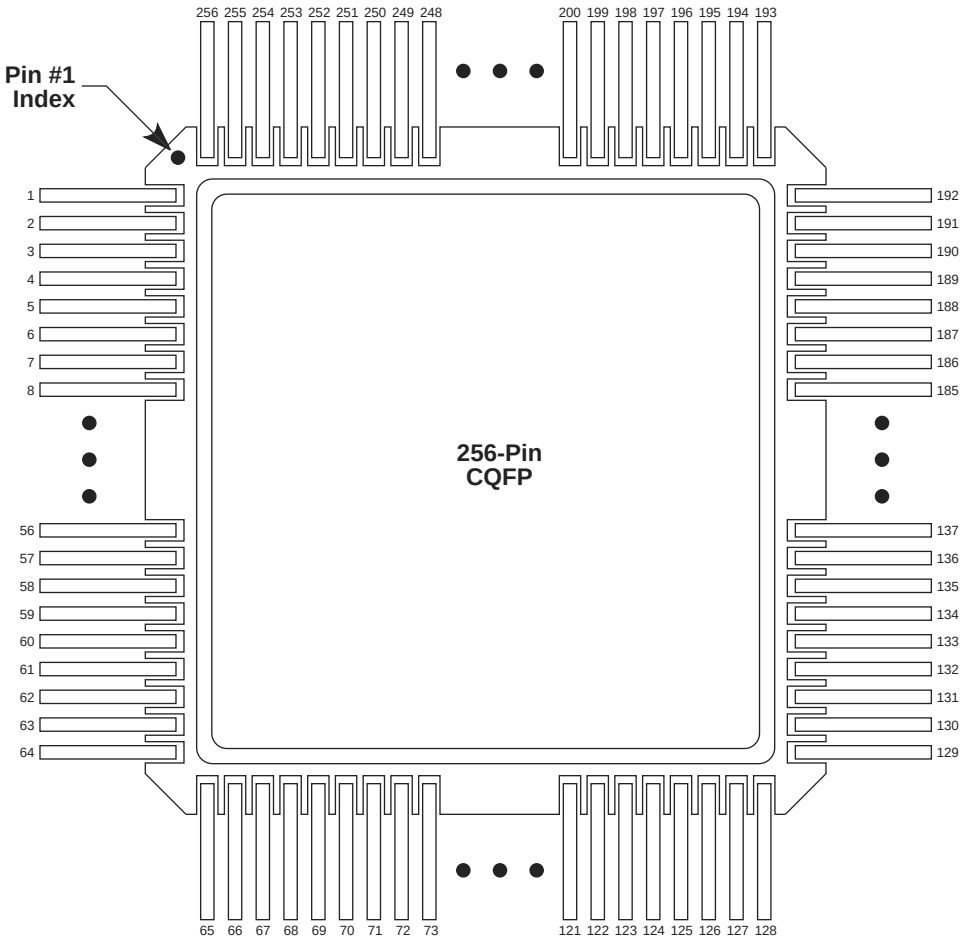



*Note: This is the top view.*

## Note

For Package Manufacturing and Environmental information, visit the Resource Center at http://www.microsemi.com/soc/products/solutions/package/docs.aspx

# CQ256




*Note: This is the top view.*

## Note

For Package Manufacturing and Environmental information, visit the Resource Center at http://www.microsemi.com/soc/products/solutions/package/docs.aspx

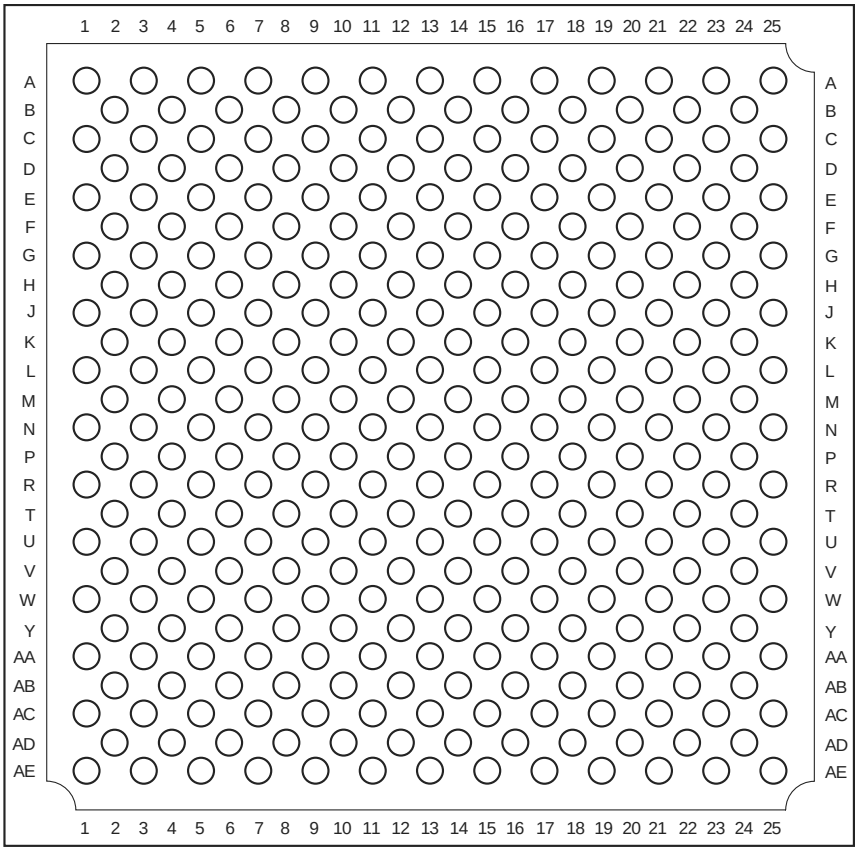
| CQ256 | |
|---|---|
| **Pin Number** | **A14100 Function** |
| 1 | GND |
| 2 | SDI, I/O |
| 11 | MODE |
| 28 | VCC |
| 29 | GND |
| 30 | VCC |
| 31 | GND |
| 46 | VCC |
| 59 | GND |
| 90 | PRB, I/O |
| 91 | GND |
| 92 | VCC |
| 93 | GND |
| 94 | VCC |
| 96 | HCLK, I/O |
| 110 | GND |
| 126 | SDO |
| 127 | IOPCL, I/O |
| 128 | GND |

| CQ256 | |
|---|---|
| **Pin Number** | **A14100 Function** |
| 141 | VCC |
| 158 | GND |
| 159 | VCC |
| 160 | GND |
| 161 | VCC |
| 174 | VCC |
| 175 | GND |
| 176 | GND |
| 188 | IOCLK, I/O |
| 189 | GND |
| 219 | CLKA, I/O |
| 220 | CLKB, I/O |
| 221 | VCC |
| 222 | GND |
| 223 | VCC |
| 224 | GND |
| 225 | PRA, I/O |
| 240 | GND |
| 256 | DCLK, I/O |

*Notes:*

1. All unlisted pin numbers are user I/Os.
2. NC denotes no connection.
3. MODE should be terminated to GND through a 10K resistor to enable Actionprobe usage; otherwise it can be terminated directly to GND.

# BG313

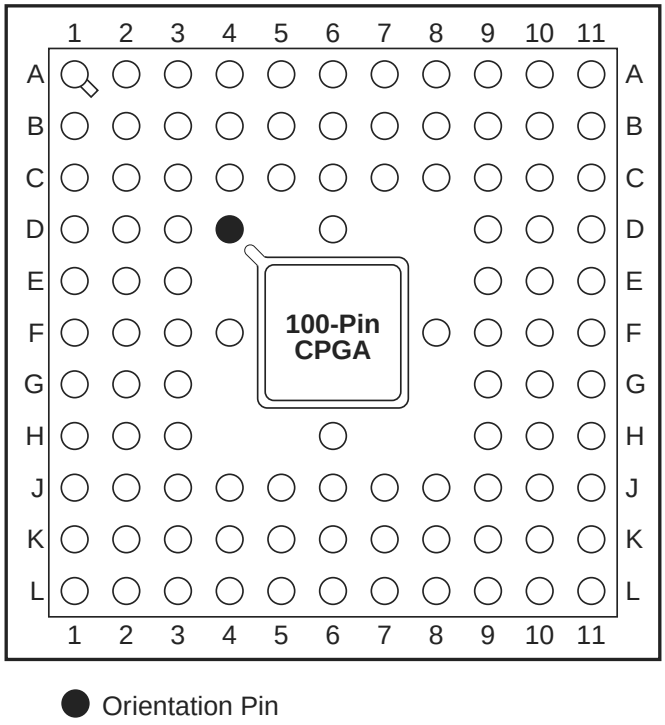



*Note: This is the top view.*

## Note

For Package Manufacturing and Environmental information, visit the Resource Center at http://www.microsemi.com/soc/products/solutions/package/docs.aspx

# PG100




*Note: This is the top view.*

## Note

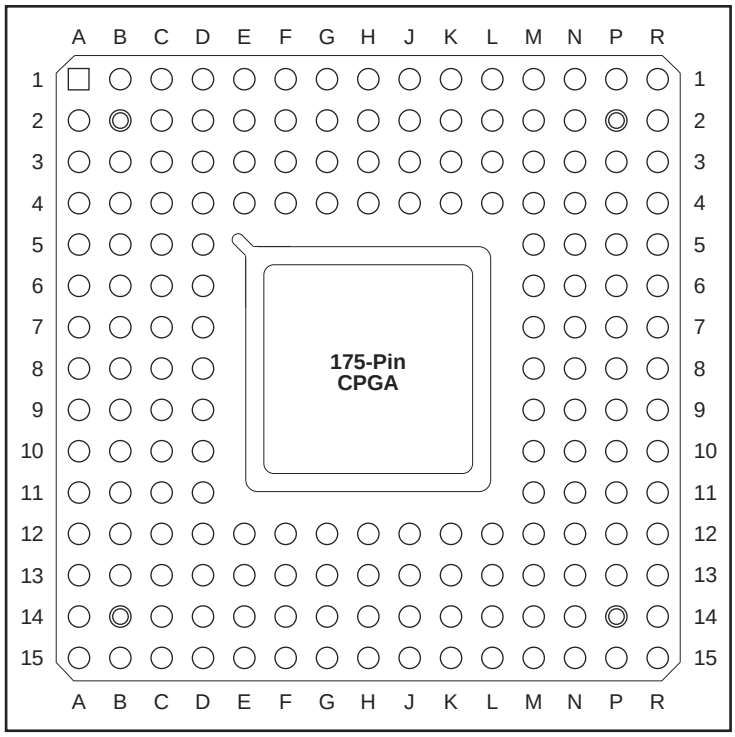
For Package Manufacturing and Environmental information, visit the Resource Center at http://www.microsemi.com/soc/products/solutions/package/docs.aspx

| PG133 | |
|---|---|
| **A1425 Function** | **Location** |
| CLKA or I/O | D7 |
| CLKB or I/O | B6 |
| DCLK or I/O | D4 |
| GND | A2, C3, C7, C11, C12, F10, G3, G11, L3, L7, L11, M3, N12 |
| HCLK or I/O | K7 |
| IOCLK or I/O | C10 |
| IOPCL or I/O | L10 |
| MODE | E3 |
| NC | A1, A7, A13, G1, G13, N1, N7, N13 |
| PRA or I/O | A6 |
| PRB or I/O | L6 |
| SDI or I/O | C2 |
| SDO | M11 |
| VCC | B2, B7, B12, E11, G2, G12, J2, J12, M2, M7, M12 |

*Notes:*

1. All unlisted pin numbers are user I/Os.
2. NC denotes no connection.
3. MODE should be terminated to GND through a 10K resistor to enable Actionprobe usage; otherwise it can be terminated directly to GND.
4. The PG133 package has been discontinued.

# PG175

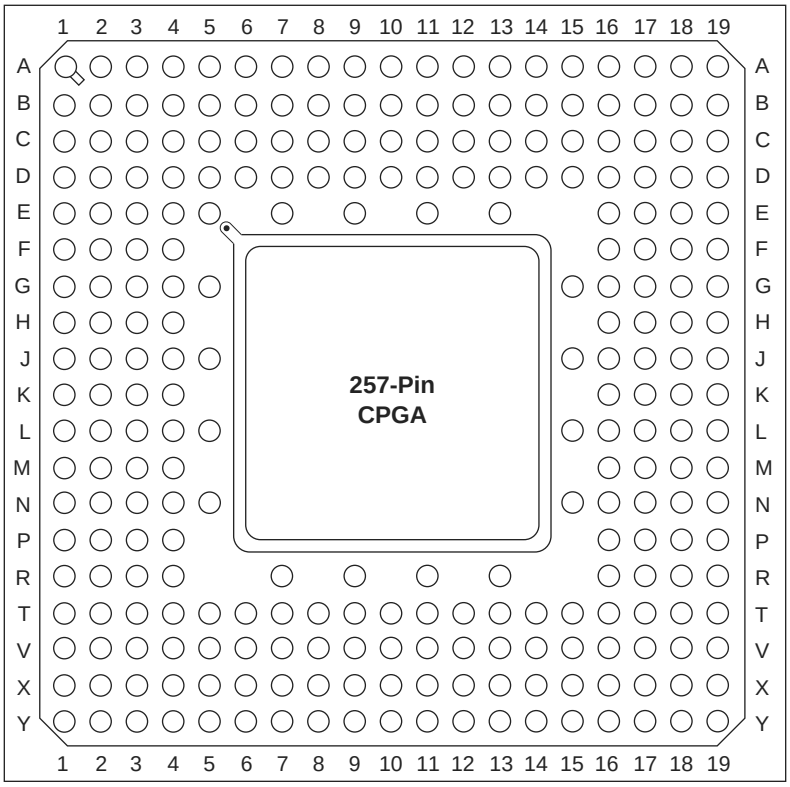



*Note: This is the top view.*

## Note

For Package Manufacturing and Environmental information, visit the Resource Center at http://www.microsemi.com/soc/products/solutions/package/docs.aspx

# PG257




*Note: This is the top view.*

## Note

For Package Manufacturing and Environmental information, visit the Resource Center at http://www.microsemi.com/soc/products/solutions/package/docs.aspx