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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications,

Details	
Product Status	Obsolete
Number of LABs/CLBs	1377
Number of Logic Elements/Cells	-
Total RAM Bits	-
Number of I/O	228
Number of Gates	10000
Voltage - Supply	3V ~ 3.6V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 70°C (TA)
Package / Case	313-BBGA
Supplier Device Package	313-PBGA (35x35)
Purchase URL	https://www.e-xfl.com/product-detail/microsemi/a14v100a-bg313c

Ordering Information

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A14100   A   –   1   RQ   G   208   C
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Application (Temperature Range)
C = Commercial (0 to +70°C)
I = Industrial (–40 to +85°C)
M = Military (–55 to +125°C)
B = MIL-STD-883

Package Lead Count

Lead-Free Packaging
Blank = Standard Packaging
G = RoHS Compliant Packaging

Package Type
PG = Ceramic Pin Grid Array
PL = Plastic Leaded Chip Carrier
PQ = Plastic Quad Flatpack
RQ = Plastic Power Quad Flatpack
VQ = Very Thin (1.0 mm) Quad Flatpack
TQ = Thin (1.4 mm) Quad Flatpack
CQ = Ceramic Quad Flatpack
BG = Plastic Ball Grid Array

Speed Grade
Std = Standard Speed
–1 = Approximately 15% faster than Standard
–2 = Approximately 25% faster than Standard
–3 = Approximately 35% faster than Standard

Die Revision
A = 1.0 mm CMOS Process

Part Number
A1415A = 1,500 Gates
A14V15A = 1,500 Gates (3.3 V)
A1425A = 2,500 Gates
A14V25A = 2,500 Gates (3.3 V)
A1440A = 4,000 Gates
A14V40A = 4,000 Gates (3.3 V)
A1460A = 6,000 Gates
A14V60A = 6,000 Gates (3.3 V)
A14100A = 10,000 Gates
A14V100A = 10,000 Gates (3.3 V)

Notes:
1. The –2 and –3 speed grades have been discontinued.
2. The Ceramic Pin Grid Array packages PG100, PG133, and PG175 have been discontinued in all device densities, speed grades, and temperature grades.
3. The Plastic Ball Grid Array package BG225 has been discontinued in all device densities (specifically for A1460A), all speed grades, and all temperature grades.
4. Military Grade devices are no longer available for the A1440A device.
5. For more information about discontinued devices, refer to the Product Discontinuation Notices (PDNs) listed below, available on the Microsemi SoC Products Group website:
   PDN March 2001
   PDN 0104
   PDN 0203
   PDN 0604
   PDN 1004

The I/O module output Y is used to bring Pad signals into the array or to feed the output register back into the array. This allows the output register to be used in high-speed state machine applications. Side I/O modules have a dedicated output segment for Y extending into the routing channels above and below (similar to logic modules). Top/Bottom I/O modules have no dedicated output segment. Signals coming into the chip from the top or bottom are routed using F-fuses and LVTs (F-fuses and LVTs are explained in detail in the routing section).

I/O Pad Drivers

All pad drivers are capable of being tristate. Each buffer connects to an associated I/O module with four signals: OE (Output Enable), IE (Input Enable), DataOut, and DataIn. Certain special signals used only during programming and test also connect to the pad drivers: OUTEN (global output enable), INEN (global input enable), and SLEW (individual slew selection). See Figure 2-5.
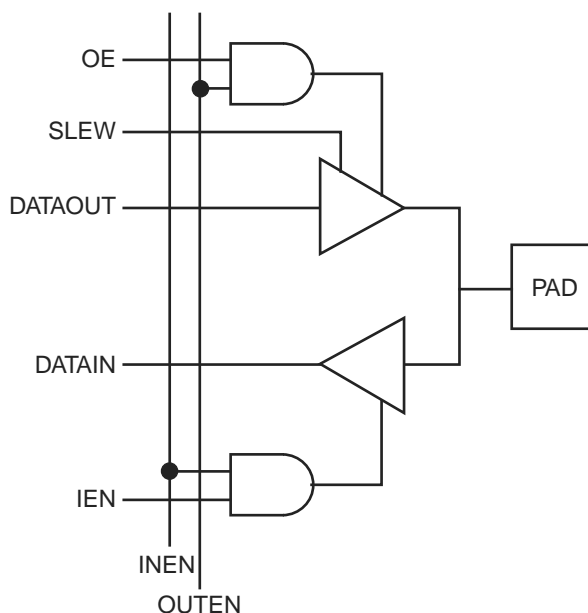

Figure 2-5 •   Function Diagram for I/O Pad Driver

Special I/Os

The special I/Os are of two types: temporary and permanent. Temporary special I/Os are used during programming and testing. They function as normal I/Os when the MODE pin is inactive. Permanent special I/Os are user programmed as either normal I/Os or special I/Os. Their function does not change once the device has been programmed. The permanent special I/Os consist of the array clock input buffers (CLKA and CLKB), the hard-wired array clock input buffer (HCLK), the hard-wired I/O clock input buffer (IOCLK), and the hard-wired I/O register preset/clear input buffer (IOPCL). Their function is determined by the I/O macros selected.

Clock Networks

The ACT 3 architecture contains four clock networks: two high-performance dedicated clock networks and two general purpose routed networks. The high-performance networks function up to 200 MHz, while the general purpose routed networks function up to 150 MHz.

Package Thermal Characteristics

The device junction to case thermal characteristic is θjc, and the junction to ambient air characteristic is θja. The thermal characteristics for θja are shown with two different air flow rates.

Maximum junction temperature is 150°C.

A sample calculation of the absolute maximum power dissipation allowed for a CPGA 175-pin package at commercial temperature and still air is as follows:

$$\frac{\text{Max. junction temp. (°C)} - \text{Max. ambient temp. (°C)}}{\theta_{ja}\text{°C/W}} = \frac{150\text{°C} - 70\text{°C}}{25\text{°C/W}} = 3.2\text{ W}$$

EQ 2

Table 2-8 • **Package Thermal Characteristics**

Package Type*	Pin Count	θ_{jc}	θ_{ja} Still Air	θ_{ja} 300 ft./min.	Units
Ceramic Pin Grid Array	100	20	35	17	°C/W
	133	20	30	15	°C/W
	175	20	25	14	°C/W
	207	20	22	13	°C/W
	257	20	15	8	°C/W
Ceramic Quad Flatpack	132	13	55	30	°C/W
	196	13	36	24	°C/W
	256	13	30	18	°C/W
Plastic Quad Flatpack	100	13	51	40	°C/W
	160	10	33	26	°C/W
	208	10	33	26	°C/W
Very Thin Quad Flatpack	100	12	43	35	°C/W
Thin Quad Flatpack	176	11	32	25	°C/W
Power Quad Flatpack	208	0.4	17	13	°C/W
Plastic Leaded Chip Carrier	84	12	37	28	°C/W
Plastic Ball Grid Array	225	10	25	19	°C/W
	313	10	23	17	°C/W

Note: Maximum power dissipation in still air:
PQ160 = 2.4 W
PQ208 = 2.4 W
PQ100 = 1.6 W
VQ100 = 1.9 W
TQ176 = 2.5 W
PL84 = 2.2 W
RQ208 = 4.7 W
BG225 = 3.2 W
BG313 = 3.5 W

Power Dissipation

$$P = [ICC\ standby + Iactive] * VCC * IOL * VOL * N + IOH* (VCC - VOH) * M$$

<div align="right">EQ 3</div>

where:

ICC standby is the current flowing when no inputs or outputs are changing

Iactive is the current flowing due to CMOS switching.

IOL and IOH are TTL sink/source current.

VOL and VOH are TTL level output voltages.

N is the number of outputs driving TTL loads to VOL.

M equals the number of outputs driving TTL loads to VOH.

An accurate determination of N and M is problematic because their values depend on the design and on the system I/O. The power can be divided into two components: static and active.

Static Power Component

Microsemi FPGAs have small static power components that result in lower power dissipation than PALs or PLDs. By integrating multiple PALs/PLDs into one FPGA, an even greater reduction in board-level power dissipation can be achieved.

The power due to standby current is typically a small component of the overall power. Standby power is calculated in Table 2-9 for commercial, worst case conditions.

Table 2-9 • **Standby Power Calculation**

ICC	VCC	Power
2 mA	5.25 V	10.5 mW

The static power dissipated by TTL loads depends on the number of outputs driving high or low and the DC load current. Again, this value is typically small. For instance, a 32-bit bus sinking 4 mA at 0.33 V will generate 42 mW with all outputs driving low, and 140 mW with all outputs driving high. The actual dissipation will average somewhere between as I/Os switch states with time.

Active Power Component

Power dissipation in CMOS devices is usually dominated by the active (dynamic) power dissipation. This component is frequency dependent, a function of the logic and the external I/O. Active power dissipation results from charging internal chip capacitances of the interconnect, unprogrammed antifuses, module inputs, and module outputs, plus external capacitance due to PC board traces and load device inputs.

An additional component of the active power dissipation is the totem-pole current in CMOS transistor pairs. The net effect can be associated with an equivalent capacitance that can be combined with frequency and voltage to represent active power dissipation.

Equivalent Capacitance

The power dissipated by a CMOS circuit can be expressed by EQ 4.

$$Power\ (\mu W) = C_{EQ} * VCC^2 * F$$

<div align="right">EQ 4</div>

Where:

C_{EQ} is the equivalent capacitance expressed in pF.

VCC is the power supply in volts.

F is the switching frequency in MHz.

A1415A, A14V15A Timing Characteristics (continued)

Table 2-19 • **A1415A, A14V15A Worst-Case Commercial Conditions, VCC = 4.75 V, T$_J$ = 70°C**

I/O Module Input Propagation Delays		–3 Speed[1]		–2 Speed[1]		–1 Speed		Std. Speed		3.3 V Speed[2]		Units
Parameter/Description		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t$_{INY}$	Input Data Pad to Y		2.8		3.2		3.6		4.2		5.5	ns
t$_{ICKY}$	Input Reg IOCLK Pad to Y		4.7		5.3		6.0		7.0		9.2	ns
t$_{OCKY}$	Output Reg IOCLK Pad to Y		4.7		5.3		6.0		7.0		9.2	ns
t$_{ICLRY}$	Input Asynchronous Clear to Y		4.7		5.3		6.0		7.0		9.2	ns
t$_{OCLRY}$	Output Asynchronous Clear to Y		4.7		5.3		6.0		7.0		9.2	ns
Predicted Input Routing Delays[2]												
t$_{RD1}$	FO = 1 Routing Delay		0.9		1.0		1.1		1.3		1.7	ns
t$_{RD2}$	FO = 2 Routing Delay		1.2		1.4		1.6		1.8		2.4	ns
t$_{RD3}$	FO = 3 Routing Delay		1.4		1.6		1.8		2.1		2.8	ns
t$_{RD4}$	FO = 4 Routing Delay		1.7		1.9		2.2		2.5		3.3	ns
t$_{RD8}$	FO = 8 Routing Delay		2.8		3.2		3.6		4.2		5.5	ns
I/O Module Sequential Timing (wrt IOCLK pad)												
t$_{INH}$	Input F-F Data Hold	0.0		0.0		0.0		0.0		0.0		ns
t$_{INSU}$	Input F-F Data Setup	2.0		2.3		2.5		3.0		3.0		ns
t$_{IDEH}$	Input Data Enable Hold	0.0		0.0		0.0		0.0		0.0		ns
t$_{IDESU}$	Input Data Enable Setup	5.8		6.5		7.5		8.6		8.6		ns
t$_{OUTH}$	Output F-F Data hold	0.7		0.8		0.9		1.0		1.0		ns
t$_{OUTSU}$	Output F-F Data Setup	0.7		0.8		0.9		1.0		1.0		ns
t$_{ODEH}$	Output Data Enable Hold	0.3		0.4		0.4		0.5		0.5		ns
f$_{ODESU}$	Output Data Enable Setup	1.3		1.5		1.7		2.0		2.0		ns

Notes:

1. The –2 and –3 speed grades have been discontinued. Please refer to the Product Discontinuation Notices (PDNs) listed below:

> *PDN March 2001*
> *PDN 0104*
> *PDN 0203*
> *PDN 0604*
> *PDN 1004*

2. Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual worst-case performance. Post-route timing is based on actual routing delay measurements performed on the device prior to shipment.

A1440A, A14V40A Timing Characteristics (continued)

Table 2-28 • **A1440A, A14V40A Worst-Case Commercial Conditions, VCC = 4.75 V, T$_J$ = 70°C**

I/O Module – TTL Output Timing[1]		–3 Speed[2]		–2 Speed[2]		–1 Speed		Std. Speed		3.3 V Speed[1]		Units
Parameter/Description		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t$_{DHS}$	Data to Pad, High Slew		5.0		5.6		6.4		7.5		9.8	ns
t$_{DLS}$	Data to Pad, Low Slew		8.0		9.0		10.2		12.0		15.6	ns
t$_{ENZHS}$	Enable to Pad, Z to H/L, High Slew		4.0		4.5		5.1		6.0		7.8	ns
t$_{ENZLS}$	Enable to Pad, Z to H/L, Low Slew		7.4		8.3		9.4		11.0		14.3	ns
t$_{ENHSZ}$	Enable to Pad, H/L to Z, High Slew		7.4		8.3		9.4		11.0		14.3	ns
t$_{ENLSZ}$	Enable to Pad, H/L to Z, Low Slew		7.4		8.3		9.4		11.0		14.3	ns
t$_{CKHS}$	IOCLK Pad to Pad H/L, High Slew		8.5		8.5		9.5		11.0		14.3	ns
t$_{CKLS}$	IOCLK Pad to Pad H/L, Low Slew		11.3		11.3		13.5		15.0		19.5	ns
d$_{TLHHS}$	Delta Low to High, High Slew		0.02		0.02		0.03		0.03		0.04	ns/pF
d$_{TLHLS}$	Delta Low to High, Low Slew		0.05		0.05		0.06		0.07		0.09	ns/pF
d$_{THLHS}$	Delta High to Low, High Slew		0.04		0.04		0.04		0.05		0.07	ns/pF
d$_{THLLS}$	Delta High to Low, Low Slew		0.05		0.05		0.06		0.07		0.09	ns/pF
I/O Module – CMOS Output Timing[1]												
t$_{DHS}$	Data to Pad, High Slew		6.2		7.0		7.9		9.3		12.1	ns
t$_{DLS}$	Data to Pad, Low Slew		11.7		13.1		14.9		17.5		22.8	ns
t$_{ENZHS}$	Enable to Pad, Z to H/L, High Slew		5.2		5.9		6.6		7.8		10.1	ns
t$_{ENZLS}$	Enable to Pad, Z to H/L, Low Slew		8.9		10.0		11.3		13.3		17.3	ns
t$_{ENHSZ}$	Enable to Pad, H/L to Z, High Slew		7.4		8.3		9.4		11.0		14.3	ns
t$_{ENLSZ}$	Enable to Pad, H/L to Z, Low Slew		7.4		8.3		9.4		11.0		14.3	ns
t$_{CKHS}$	IOCLK Pad to Pad H/L, High Slew		9.0		9.0		10.1		11.8		14.3	ns
t$_{CKLS}$	IOCLK Pad to Pad H/L, Low Slew		13.0		13.0		15.6		17.3		22.5	ns
d$_{TLHHS}$	Delta Low to High, High Slew		0.04		0.04		0.05		0.06		0.08	ns/pF
d$_{TLHLS}$	Delta Low to High, Low Slew		0.07		0.08		0.09		0.11		0.14	ns/pF
d$_{THLHS}$	Delta High to Low, High Slew		0.03		0.03		0.03		0.04		0.05	ns/pF
d$_{THLLS}$	Delta High to Low, Low Slew		0.04		0.04		0.04		0.05		0.07	ns/pF

Notes:

1. *Delays based on 35 pF loading.*
2. *The –2 and –3 speed grades have been discontinued. Refer to PDN 0104, PDN 0203, PDN 0604, and PDN 1004 at http://www.microsemi.com/soc/support/notifications/default.aspx#pdn.*

A14100A, A14V100A Timing Characteristics (continued)

Table 2-35 • **A14100A, A14V100A Worst-Case Commercial Conditions, VCC = 4.75 V, T$_J$ = 70°C**

I/O Module Input Propagation Delays		–3 Speed[1]		–2 Speed[1]		–1 Speed		Std. Speed		3.3 V Speed[1]		Units
Parameter/Description		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t$_{INY}$	Input Data Pad to Y		2.8		3.2		3.6		4.2		5.5	ns
t$_{ICKY}$	Input Reg IOCLK Pad to Y		4.7		5.3		6.0		7.0		9.2	ns
t$_{OCKY}$	Output Reg IOCLK Pad to Y		4.7		5.3		6.0		7.0		9.2	ns
t$_{ICLRY}$	Input Asynchronous Clear to Y		4.7		5.3		6.0		7.0		9.2	ns
t$_{OCLRY}$	Output Asynchronous Clear to Y		4.7		5.3		6.0		7.0		9.2	ns
Predicted Input Routing Delays[2]												
t$_{RD1}$	FO = 1 Routing Delay		0.9		1.0		1.1		1.3		1.7	ns
t$_{RD2}$	FO = 2 Routing Delay		1.2		1.4		1.6		1.8		2.4	ns
t$_{RD3}$	FO = 3 Routing Delay		1.4		1.6		1.8		2.1		2.8	ns
t$_{RD4}$	FO = 4 Routing Delay		1.7		1.9		2.2		2.5		3.3	ns
t$_{RD8}$	FO = 8 Routing Delay		2.8		3.2		3.6		4.2		5.5	ns
I/O Module Sequential Timing (wrt IOCLK pad)												
t$_{INH}$	Input F-F Data Hold	0.0		0.0		0.0		0.0		0.0		ns
t$_{INSU}$	Input F-F Data Setup	1.2		1.4		1.5		1.8		1.8		ns
t$_{IDEH}$	Input Data Enable Hold	0.0		0.0		0.0		0.0		0.0		ns
t$_{IDESU}$	Input Data Enable Setup	5.8		6.5		7.5		8.6		8.6		ns
t$_{OUTH}$	Output F-F Data hold	0.7		0.8		1.0		1.0		1.0		ns
t$_{OUTSU}$	Output F-F Data Setup	0.7		0.8		1.0		1.0		1.0		ns
t$_{ODEH}$	Output Data Enable Hold	0.3		0.4		0.5		0.5		0.5		ns
f$_{ODESU}$	Output Data Enable Setup	1.3		1.5		2.0		2.0		2.0		ns

Notes: *

1. *The –2 and –3 speed grades have been discontinued. Refer to PDN 0104, PDN 0203, PDN 0604, and PDN 1004 at http://www.microsemi.com/soc/support/notifications/default.aspx#pdn.*

2. *Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual worst-case performance. Post-route timing is based on actual routing delay measurements performed on the device prior to shipment.*

A14100A, A14V100A Timing Characteristics (continued)

*Table 2-36 • A14100A, A14V100A Worst-Case Commercial Conditions, VCC = 4.75 V, T$_J$ = 70°C*

I/O Module – TTL Output Timing[1]		–3 Speed[2]		–2 Speed[2]		–1 Speed		Std. Speed		3.3 V Speed[1]		Units
Parameter/Description		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t$_{DHS}$	Data to Pad, High Slew		5.0		5.6		6.4		7.5		9.8	ns
t$_{DLS}$	Data to Pad, Low Slew		8.0		9.0		10.2		12.0		15.6	ns
t$_{ENZHS}$	Enable to Pad, Z to H/L, High Slew		4.0		4.5		5.1		6.0		7.8	ns
t$_{ENZLS}$	Enable to Pad, Z to H/L, Low Slew		7.4		8.3		9.4		11.0		14.3	ns
t$_{ENHSZ}$	Enable to Pad, H/L to Z, High Slew		8.0		9.0		10.2		12.0		15.6	ns
t$_{ENLSZ}$	Enable to Pad, H/L to Z, Low Slew		7.4		8.3		9.4		11.0		14.3	ns
t$_{CKHS}$	IOCLK Pad to Pad H/L, High Slew		9.5		9.5		10.5		12.0		15.6	ns
t$_{CKLS}$	IOCLK Pad to Pad H/L, Low Slew		12.8		12.8		15.3		17.0		22.1	ns
d$_{TLHHS}$	Delta Low to High, High Slew		0.02		0.02		0.03		0.03		0.04	ns/pF
d$_{TLHLS}$	Delta Low to High, Low Slew		0.05		0.05		0.06		0.07		0.09	ns/pF
d$_{THLHS}$	Delta High to Low, High Slew		0.04		0.04		0.04		0.05		0.07	ns/pF
d$_{THLLS}$	Delta High to Low, Low Slew		0.05		0.05		0.06		0.07		0.09	ns/pF
I/O Module – CMOS Output Timing[1]												
t$_{DHS}$	Data to Pad, High Slew		6.2		7.0		7.9		9.3		12.1	ns
t$_{DLS}$	Data to Pad, Low Slew		11.7		13.1		14.9		17.5		22.8	ns
t$_{ENZHS}$	Enable to Pad, Z to H/L, High Slew		5.2		5.9		6.6		7.8		10.1	ns
t$_{ENZLS}$	Enable to Pad, Z to H/L, Low Slew		8.9		10.0		11.3		13.3		17.3	ns
t$_{ENHSZ}$	Enable to Pad, H/L to Z, High Slew		8.0		9.0		10.0		12.0		15.6	ns
t$_{ENLSZ}$	Enable to Pad, H/L to Z, Low Slew		7.4		8.3		9.4		11.0		14.3	ns
t$_{CKHS}$	IOCLK Pad to Pad H/L, High Slew		10.4		10.4		12.4		13.8		17.9	ns
t$_{CKLS}$	IOCLK Pad to Pad H/L, Low Slew		14.5		14.5		17.4		19.3		25.1	ns
d$_{TLHHS}$	Delta Low to High, High Slew		0.04		0.04		0.05		0.06		0.08	ns/pF
d$_{TLHLS}$	Delta Low to High, Low Slew		0.07		0.08		0.09		0.11		0.14	ns/pF
d$_{THLHS}$	Delta High to Low, High Slew		0.03		0.03		0.03		0.04		0.05	ns/pF
d$_{THLLS}$	Delta High to Low, Low Slew		0.04		0.04		0.04		0.05		0.07	ns/pF

Notes: *

1. Delays based on 35 pF loading.

2. The –2 and –3 speed grades have been discontinued. Refer to PDN 0104, PDN 0203, PDN 0604, and PDN 1004 at http://www.microsemi.com/soc/support/notifications/default.aspx#pdn.

3 – Package Pin Assignments

PL84
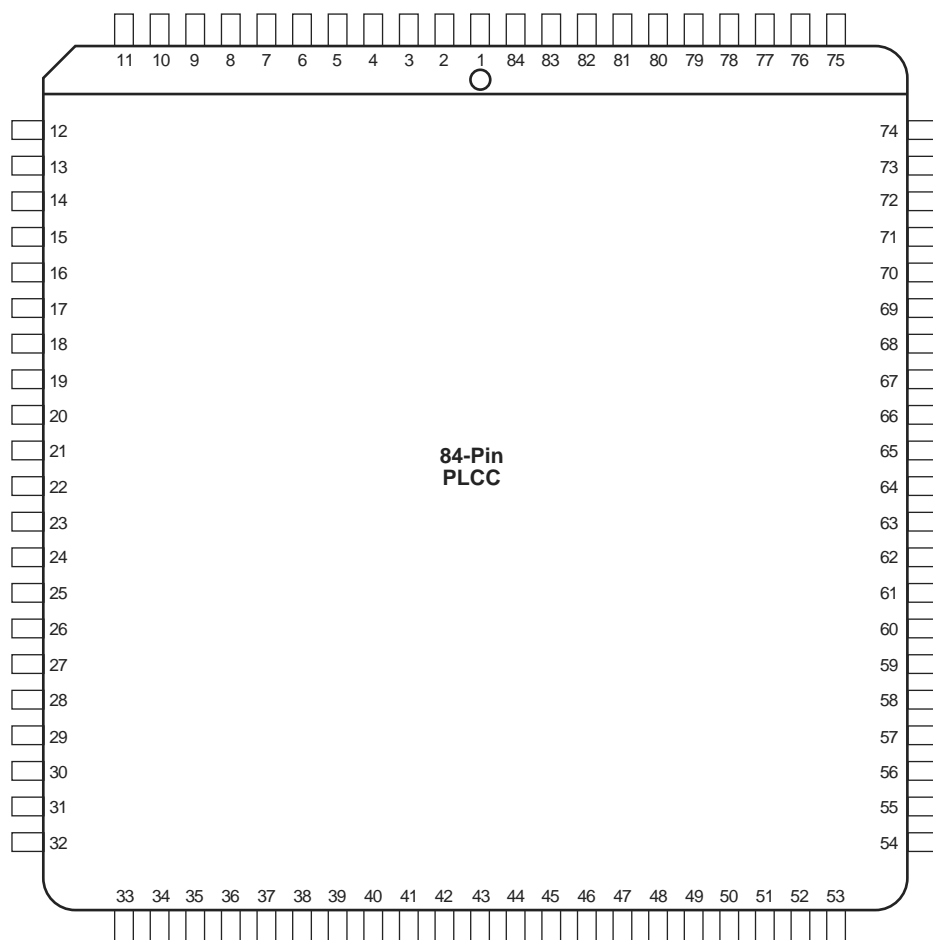
Note: This is the top view of the package.

Note

For Package Manufacturing and Environmental information, visit the Resource Center at
http://www.microsemi.com/soc/products/solutions/package/docs.aspx.

PQ100		
Pin Number	**A1415 Function**	**A1425 Function**
2	IOCLK, I/O	IOCLK, I/O
14	CLKA, I/O	CLKA, I/O
15	CLKB, I/O	CLKB, I/O
16	VCC	VCC
17	GND	GND
18	VCC	VCC
19	GND	GND
20	PRA, I/O	PRA, I/O
27	DCLK, I/O	DCLK, I/O
28	GND	GND
29	SDI, I/O	SDI, I/O
34	MODE	MODE
35	VCC	VCC
36	GND	GND
47	GND	GND
48	VCC	VCC
61	PRB, I/O	PRB, I/O
62	GND	GND
63	VCC	VCC
64	GND	GND
65	VCC	VCC
67	HCLK, I/O	HCLK, I/O
77	SDO	SDO
78	IOPCL, I/O	IOPCL, I/O
79	GND	GND
85	VCC	VCC
86	VCC	VCC
87	GND	GND
96	VCC	VCC
97	GND	GND

Notes:

1. All unlisted pin numbers are user I/Os.
2. NC denotes no connection.
3. MODE should be terminated to GND through a 10K resistor to enable Actionprobe usage; otherwise it can be terminated directly to GND.

PQ160
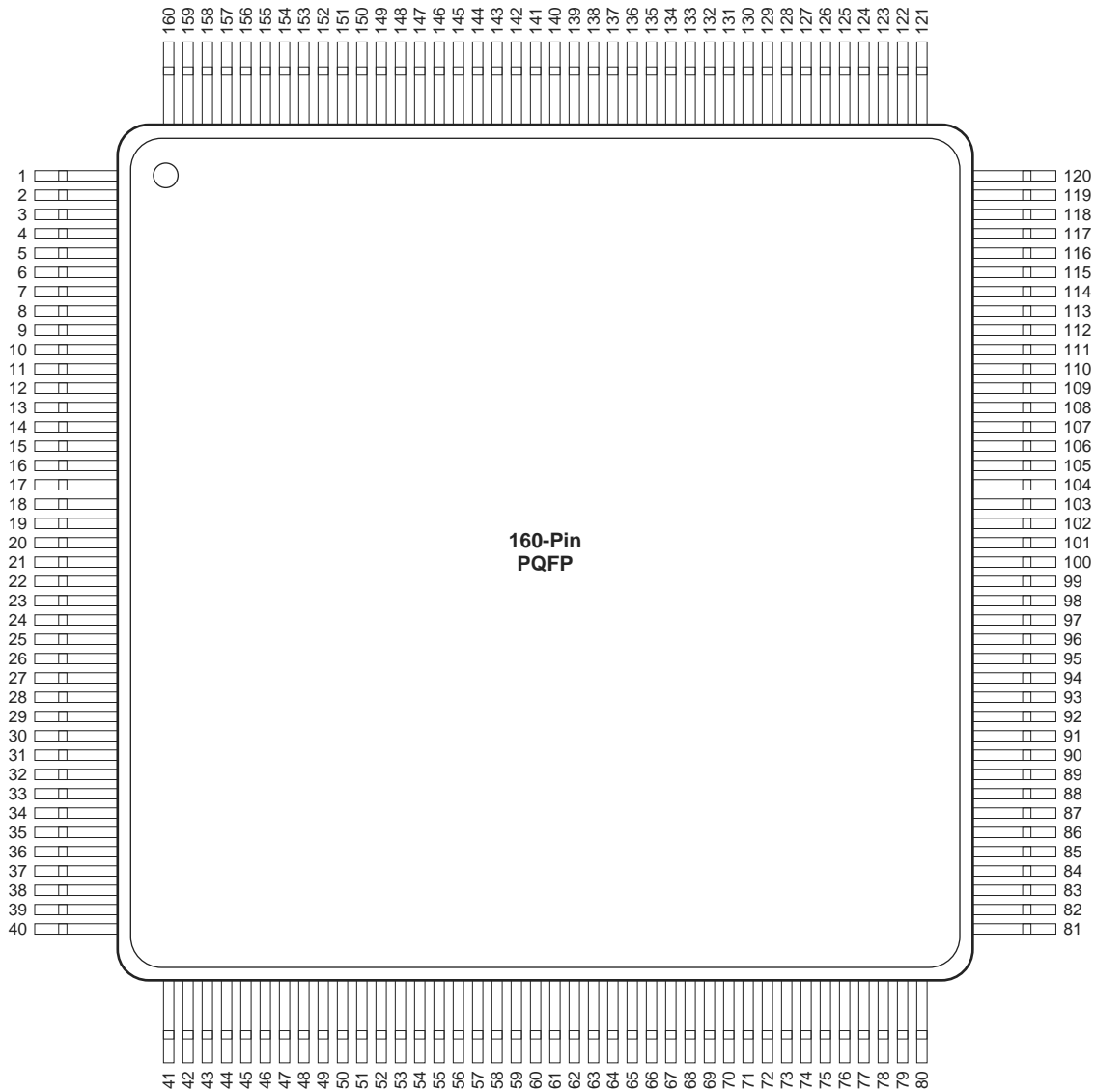
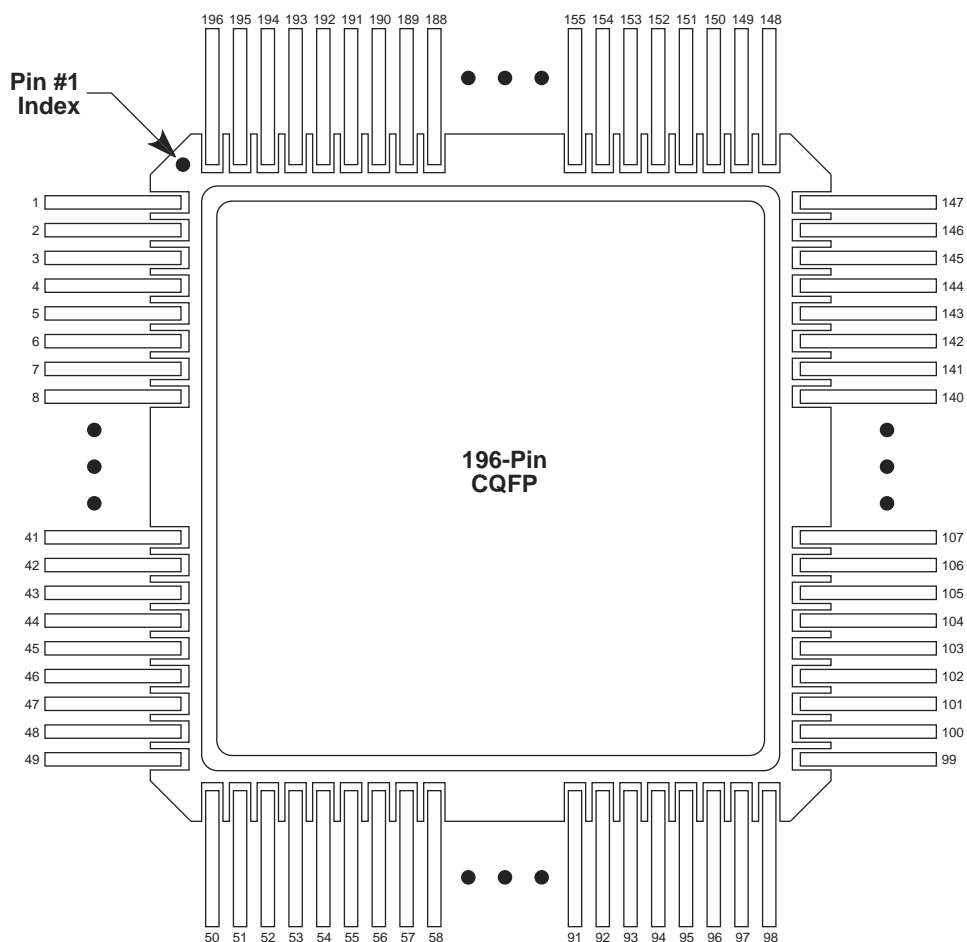160-Pin
PQFP

Note: This is the top view of the package

Note

For Package Manufacturing and Environmental information, visit the Resource Center at
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PQ160			
Pin Number	A1425, A14V25 Function	A1440, A14V40 Function	A1460, A14V60 Function
92	NC	I/O	I/O
93	NC	I/O	I/O
98	GND	GND	GND
99	VCC	VCC	VCC
100	NC	I/O	I/O
103	GND	GND	GND
107	NC	I/O	I/O
109	NC	I/O	I/O
110	VCC	VCC	VCC
111	GND	GND	GND
112	VCC	VCC	VCC
113	NC	I/O	I/O
119	NC	I/O	I/O
120	IOCLK, I/O	IOCLK, I/O	IOCLK, I/O
121	GND	GND	GND
124	NC	I/O	I/O
127	NC	I/O	I/O
136	CLKA, I/O	CLKA, I/O	CLKA, I/O
137	CLKB, I/O	CLKB, I/O	CLKB, I/O
138	VCC	VCC	VCC
139	GND	GND	GND
140	VCC	VCC	VCC
141	GND	GND	GND
142	PRA, I/O	PRA, I/O	PRA, I/O
143	NC	I/O	I/O
145	NC	I/O	I/O
147	NC	I/O	I/O
149	NC	I/O	I/O
151	NC	I/O	I/O
153	NC	I/O	I/O
154	VCC	VCC	VCC
160	DCLK, I/O	DCLK, I/O	DCLK, I/O

Notes:

1. All unlisted pin numbers are user I/Os.

2. NC denotes no connection.

3. MODE should be terminated to GND through a 10K resistor to enable Actionprobe usage; otherwise it can be terminated directly to GND.

PQ208, RQ208

**208-Pin
PQFP, RQFP**

Note: This is the top view of the package

Note

For Package Manufacturing and Environmental information, visit the Resource Center at
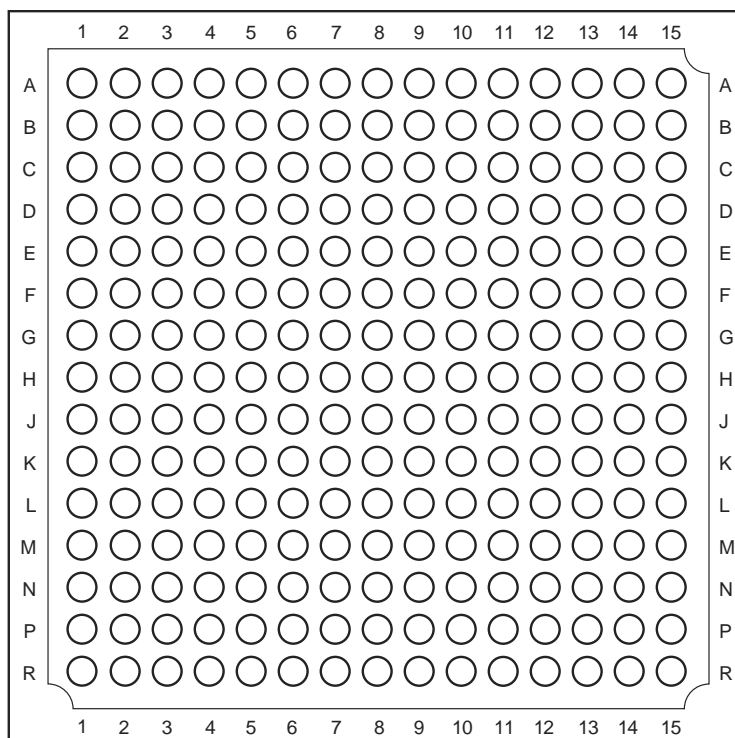http://www.microsemi.com/soc/products/solutions/package/docs.aspx

![Microsemi logo]

CQ196

Note: This is the top view.

Note

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BG225

Note: This is the top view.

Note

For Package Manufacturing and Environmental information, visit the Resource Center at
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PG100	
A1415 Function	**Location**
CLKA or I/O	C7
CLKB or I/O	D6
DCLK or I/O	C4
GND	C3, C6, C9, E9, F3, F9, J3, J6, J8, J9
HCLK or I/O	H6
IOCLK or I/O	C10
IOPCL or I/O	K9
MODE	C2
PRA or I/O	A6
PRB or I/O	L3
SDI or I/O	B3
SDO	L9
VCC	B6, B10, E11, F2, F10, G2, K2, K6, K10

Notes:

1. All unlisted pin numbers are user I/Os.
2. NC denotes no connection.
3. MODE should be terminated to GND through a 10K resistor to enable Actionprobe usage; otherwise it can be terminated directly to GND.
4. The PG100 package has been discontinued.

PG133	
A1425 Function	**Location**
CLKA or I/O	D7
CLKB or I/O	B6
DCLK or I/O	D4
GND	A2, C3, C7, C11, C12, F10, G3, G11, L3, L7, L11, M3, N12
HCLK or I/O	K7
IOCLK or I/O	C10
IOPCL or I/O	L10
MODE	E3
NC	A1, A7, A13, G1, G13, N1, N7, N13
PRA or I/O	A6
PRB or I/O	L6
SDI or I/O	C2
SDO	M11
VCC	B2, B7, B12, E11, G2, G12, J2, J12, M2, M7, M12

Notes:

1. All unlisted pin numbers are user I/Os.
2. NC denotes no connection.
3. MODE should be terminated to GND through a 10K resistor to enable Actionprobe usage; otherwise it can be terminated directly to GND.
4. The PG133 package has been discontinued.

PG207
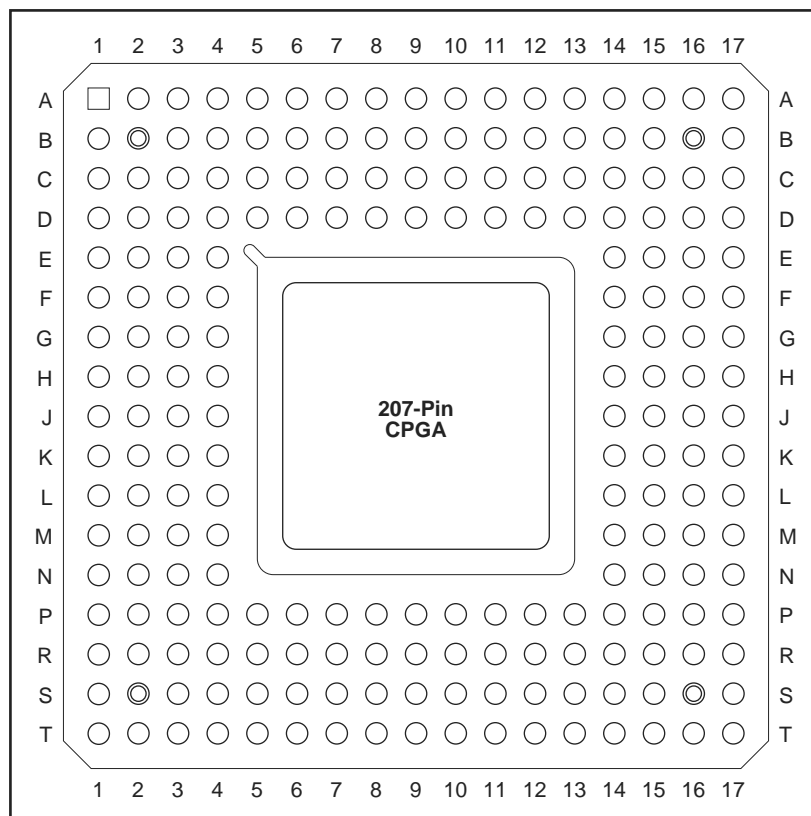
Note: This is the top view.

Note

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Microsemi

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