# Microsemi Corporation - A14V15A-PLG84C Datasheet

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## Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

## Applications of Embedded - FPGAs

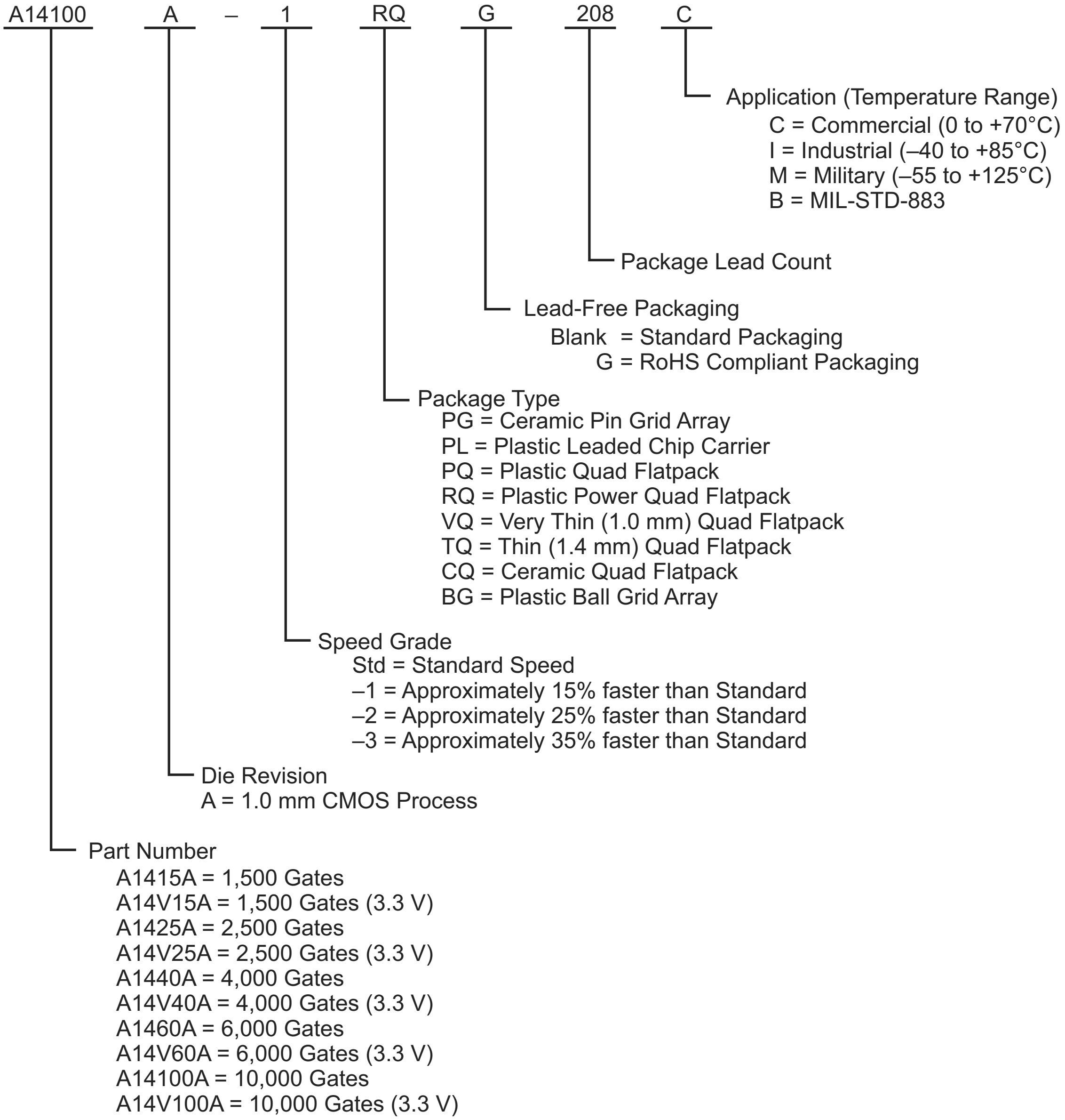
The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications,

| **Details** | |
|---|---|
| Product Status | Obsolete |
| Number of LABs/CLBs | 200 |
| Number of Logic Elements/Cells | - |
| Total RAM Bits | - |
| Number of I/O | 70 |
| Number of Gates | 1500 |
| Voltage - Supply | 3V ~ 3.6V |
| Mounting Type | Surface Mount |
| Operating Temperature | 0°C ~ 70°C (TA) |
| Package / Case | 84-LCC (J-Lead) |
| Supplier Device Package | 84-PLCC (29.31x29.31) |
| Purchase URL | https://www.e-xfl.com/product-detail/microsemi/a14v15a-plg84c |

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

## Ordering Information



A14100 A – 1 RQ G 208 C

Application (Temperature Range)
C = Commercial (0 to +70°C)
I = Industrial (–40 to +85°C)
M = Military (–55 to +125°C)
B = MIL-STD-883

Package Lead Count

Lead-Free Packaging
Blank = Standard Packaging
G = RoHS Compliant Packaging

Package Type
PG = Ceramic Pin Grid Array
PL = Plastic Leaded Chip Carrier
PQ = Plastic Quad Flatpack
RQ = Plastic Power Quad Flatpack
VQ = Very Thin (1.0 mm) Quad Flatpack
TQ = Thin (1.4 mm) Quad Flatpack
CQ = Ceramic Quad Flatpack
BG = Plastic Ball Grid Array

Speed Grade
Std = Standard Speed
–1 = Approximately 15% faster than Standard
–2 = Approximately 25% faster than Standard
–3 = Approximately 35% faster than Standard

Die Revision
A = 1.0 mm CMOS Process

Part Number
A1415A = 1,500 Gates
A14V15A = 1,500 Gates (3.3 V)
A1425A = 2,500 Gates
A14V25A = 2,500 Gates (3.3 V)
A1440A = 4,000 Gates
A14V40A = 4,000 Gates (3.3 V)
A1460A = 6,000 Gates
A14V60A = 6,000 Gates (3.3 V)
A14100A = 10,000 Gates
A14V100A = 10,000 Gates (3.3 V)

Notes:

1. *The –2 and –3 speed grades have been discontinued.*
2. *The Ceramic Pin Grid Array packages PG100, PG133, and PG175 have been discontinued in all device densities, speed grades, and temperature grades.*
3. *The Plastic Ball Grid Array package BG225 has been discontinued in all device densities (specifically for A1460A), all speed grades, and all temperature grades.*
4. *Military Grade devices are no longer available for the A1440A device.*
5. *For more information about discontinued devices, refer to the Product Discontinuation Notices (PDNs) listed below, available on the Microsemi SoC Products Group website:*
   *PDN March 2001*
   *PDN 0104*
   *PDN 0203*
   *PDN 0604*
   *PDN 1004*

# Logic Modules

ACT 3 logic modules are enhanced versions of the 1200XL family logic modules. As in the 1200XL family, there are two types of modules: C-modules and S-modules (Figure 2-2 and Figure 2-3). The C-module is functionally equivalent to the 1200XL C-module and implements high fanin combinatorial macros, such as 5-input AND, 5-input OR, and so on. It is available for use as the CM8 hard macro. The S-module is designed to implement high-speed sequential functions within a single module.

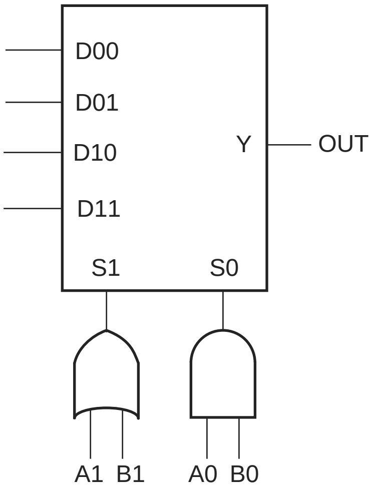


***Figure 2-2 •*** **C-Module Diagram**

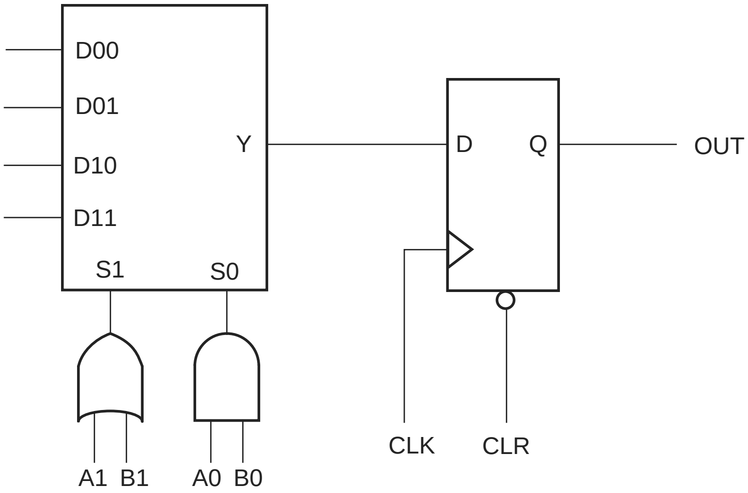


***Figure 2-3 •*** **S-Module Diagram**

S-modules consist of a full C-module driving a flip-flop, which allows an additional level of logic to be implemented without additional propagation delay. It is available for use as the DFM8A/B and DLM8A/B hard macros. C-modules and S-modules are arranged in pairs called module-pairs. Module-pairs are arranged in alternating patterns and make up the bulk of the array. This arrangement allows the placement software to support two-module macros of four types (CC, CS, SC, and SS). The C-module implements the following function:

$$Y = !S1 * !S0 * D00 + !S1 * S0 * D01 + S1 * !S0 * D10 + S1 * S0 * D11$$

*EQ 1*

where: $S0 = A0 * B0$ and $S1 = A1 + B1$

The I/O module output Y is used to bring Pad signals into the array or to feed the output register back into the array. This allows the output register to be used in high-speed state machine applications. Side I/O modules have a dedicated output segment for Y extending into the routing channels above and below (similar to logic modules). Top/Bottom I/O modules have no dedicated output segment. Signals coming into the chip from the top or bottom are routed using F-fuses and LVTs (F-fuses and LVTs are explained in detail in the routing section).

## I/O Pad Drivers

All pad drivers are capable of being tristate. Each buffer connects to an associated I/O module with four signals: OE (Output Enable), IE (Input Enable), DataOut, and DataIn. Certain special signals used only during programming and test also connect to the pad drivers: OUTEN (global output enable), INEN (global input enable), and SLEW (individual slew selection). See Figure 2-5.

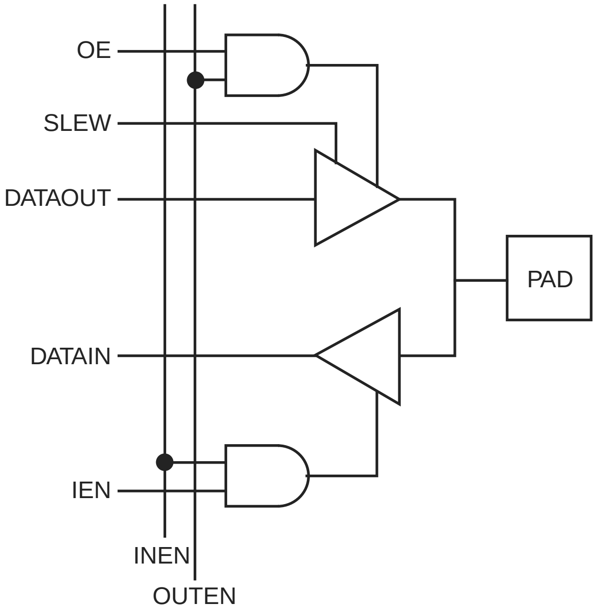


*Figure 2-5 •* **Function Diagram for I/O Pad Driver**

## Special I/Os

The special I/Os are of two types: temporary and permanent. Temporary special I/Os are used during programming and testing. They function as normal I/Os when the MODE pin is inactive. Permanent special I/Os are user programmed as either normal I/Os or special I/Os. Their function does not change once the device has been programmed. The permanent special I/Os consist of the array clock input buffers (CLKA and CLKB), the hard-wired array clock input buffer (HCLK), the hard-wired I/O clock input buffer (IOCLK), and the hard-wired I/O register preset/clear input buffer (IOPCL). Their function is determined by the I/O macros selected.

# Clock Networks

The ACT 3 architecture contains four clock networks: two high-performance dedicated clock networks and two general purpose routed networks. The high-performance networks function up to 200 MHz, while the general purpose routed networks function up to 150 MHz.

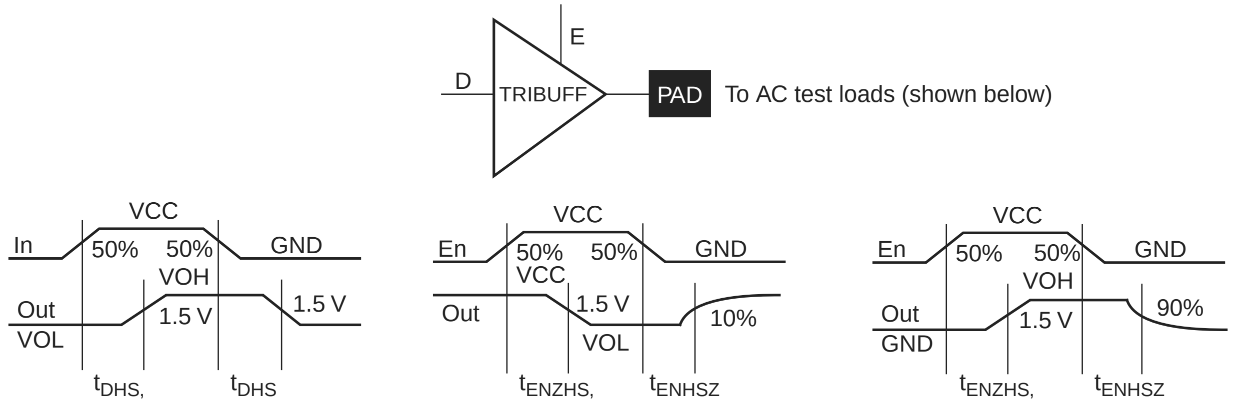
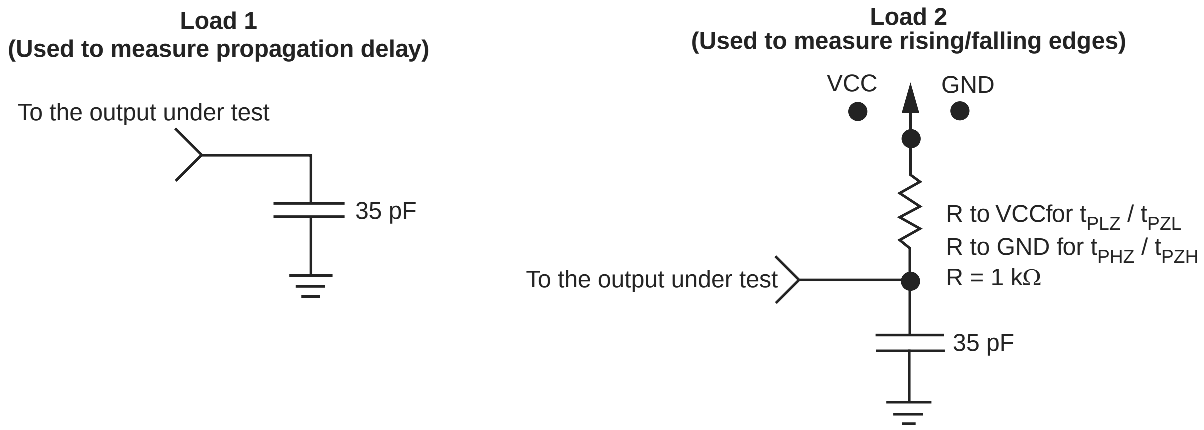


*Figure 2-11* • **Output Buffers**


**Load 1**
**(Used to measure propagation delay)**

**Load 2**
**(Used to measure rising/falling edges)**

*Figure 2-12* • **AC Test Loads**

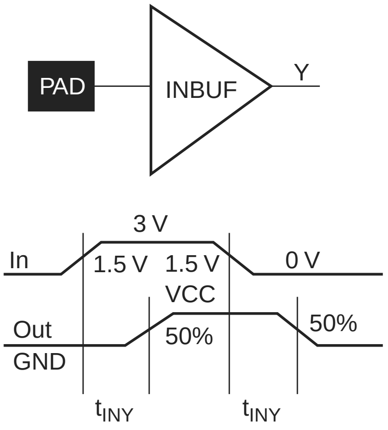


*Figure 2-13* • **Input Buffer Delays**

## Tightest Delay Distributions

Propagation delay between logic modules depends on the resistive and capacitive loading of the routing tracks, the interconnect elements, and the module inputs being driven. Propagation delay increases as the length of routing tracks, the number of interconnect elements, or the number of inputs increases.

From a design perspective, the propagation delay can be statistically correlated or modeled by the fanout (number of loads) driven by a module. Higher fanout usually requires some paths to have longer lengths of routing track. The ACT 3 family delivers the tightest fanout delay distribution of any FPGA. This tight distribution is achieved in two ways: by decreasing the delay of the interconnect elements and by decreasing the number of interconnect elements per path.

Microsemi's patented PLICE antifuse offers a very low resistive/capacitive interconnect. The ACT 3 family's antifuses, fabricated in 0.8 micron m lithography, offer nominal levels of 200Ω resistance and 6 femtofarad (fF) capacitance per antifuse. The ACT 3 fanout distribution is also tighter than alternative devices due to the low number of antifuses required per interconnect path. The ACT 3 family's proprietary architecture limits the number of antifuses per path to only four, with 90% of interconnects using only two antifuses.

The ACT 3 family's tight fanout delay distribution offers an FPGA design environment in which fanout can be traded for the increased performance of reduced logic level designs. This also simplifies performance estimates when designing with ACT 3 devices.

***Table 2-14* • Logic Module and Routing Delay by Fanout (ns); Worst-Case Commercial Conditions**

| **Speed Grade** | **FO = 1** | **FO = 2** | **FO = 3** | **FO = 4** | **FO = 8** |
|---|---|---|---|---|---|
| ACT 3 –3 | 2.9 | 3.2 | 3.4 | 3.7 | 4.8 |
| ACT 3 –2 | 3.3 | 3.7 | 3.9 | 4.2 | 5.5 |
| ACT 3 –1 | 3.7 | 4.2 | 4.4 | 4.8 | 6.2 |
| ACT 3 STD | 4.3 | 4.8 | 5.1 | 5.5 | 7.2 |

*Notes:*

1. *Obtained by added $t_{RD(x=FO)}$ to $t_{PD}$ from the Logic Module Timing Characteristics Tables found in this datasheet.*
2. *The –2 and –3 speed grades have been discontinued. Refer to PDN 0104, PDN 0203, PDN 0604, and PDN 1004 at http://www.microsemi.com/soc/support/notifications/default.aspx#pdn.*

## Timing Characteristics

Timing characteristics for ACT 3 devices fall into three categories: family dependent, device dependent, and design dependent. The input and output buffer characteristics are common to all ACT 3 family members. Internal routing delays are device dependent. Design dependency means actual delays are not determined until after placement and routing of the user's design is complete. Delay values may then be determined by using the ALS Timer utility or performing simulation with post-layout delays.

### *Critical Nets and Typical Nets*

Propagation delays are expressed only for typical nets, which are used for initial design performance evaluation. Critical net delays can then be applied to the most time-critical paths. Critical nets are determined by net property assignment prior to placement and routing. Up to 6% of the nets in a design may be designated as critical, while 90% of the nets in a design are typical.

### *Long Tracks*

Some nets in the design use long tracks. Long tracks are special routing resources that span multiple rows, columns, or modules. Long tracks employ three and sometimes four antifuse connections. This increases capacitance and resistance, result ng in longer net delays for macros connected to long tracks. Typically up to 6% of nets in a fully utilized device require long tracks. Long tracks contribute approximately 4 ns to 14 ns delay. This additional delay is represented statistically in higher fanout (FO = 8) routing delays in the datasheet specifications section.

## A1440A, A14V40A Timing Characteristics (continued)

***Table 2-27*** **• A1440A, A14V40A Worst-Case Commercial Conditions, VCC = 4.75 V, $T_J$ = 70°C**

| **I/O Module Input Propagation Delays** | | **–3 Speed[1]** | | **–2 Speed[1]** | | **–1 Speed** | | **Std. Speed** | | **3.3 V Speed[1]** | | **Units** |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **Parameter/Description** | | **Min.** | **Max.** | **Min.** | **Max.** | **Min.** | **Max.** | **Min.** | **Max.** | **Min.** | **Max.** | |
| $t_{INY}$ | Input Data Pad to Y | | 2.8 | | 3.2 | | 3.6 | | 4.2 | | 5.5 | ns |
| $t_{ICKY}$ | Input Reg IOCLK Pad to Y | | 4.7 | | 5.3 | | 6.0 | | 7.0 | | 9.2 | ns |
| $t_{OCKY}$ | Output Reg IOCLK Pad to Y | | 4.7 | | 5.3 | | 6.0 | | 7.0 | | 9.2 | ns |
| $t_{ICLRY}$ | Input Asynchronous Clear to Y | | 4.7 | | 5.3 | | 6.0 | | 7.0 | | 9.2 | ns |
| $t_{OCLRY}$ | Output Asynchronous Clear to Y | | 4.7 | | 5.3 | | 6.0 | | 7.0 | | 9.2 | ns |
| **Predicted Input Routing Delays[2]** | | | | | | | | | | | | |
| $t_{RD1}$ | FO = 1 Routing Delay | | 0.9 | | 1.0 | | 1.1 | | 1.3 | | 1.7 | ns |
| $t_{RD2}$ | FO = 2 Routing Delay | | 1.2 | | 1.4 | | 1.6 | | 1.8 | | 2.4 | ns |
| $t_{RD3}$ | FO = 3 Routing Delay | | 1.4 | | 1.6 | | 1.8 | | 2.1 | | 2.8 | ns |
| $t_{RD4}$ | FO = 4 Routing Delay | | 1.7 | | 1.9 | | 2.2 | | 2.5 | | 3.3 | ns |
| $t_{RD8}$ | FO = 8 Routing Delay | | 2.8 | | 3.2 | | 3.6 | | 4.2 | | 5.5 | ns |
| **I/O Module Sequential Timing (wrt IOCLK pad)** | | | | | | | | | | | | |
| $t_{INH}$ | Input F-F Data Hold | 0.0 | | 0.0 | | 0.0 | | 0.0 | | 0.0 | | ns |
| $t_{INSU}$ | Input F-F Data Setup | 1.8 | | 1.7 | | 2.0 | | 2.3 | | 2.3 | | ns |
| $t_{IDEH}$ | Input Data Enable Hold | 0.0 | | 0.0 | | 0.0 | | 0.0 | | 0.0 | | ns |
| $t_{IDESU}$ | Input Data Enable Setup | 5.8 | | 6.5 | | 7.5 | | 8.6 | | 8.6 | | ns |
| $t_{OUTH}$ | Output F-F Data hold | 0.7 | | 0.8 | | 0.9 | | 1.0 | | 1.0 | | ns |
| $t_{OUTSU}$ | Output F-F Data Setup | 0.7 | | 0.8 | | 0.9 | | 1.0 | | 1.0 | | ns |
| $t_{ODEH}$ | Output Data Enable Hold | 0.3 | | 0.4 | | 0.4 | | 0.5 | | 0.5 | | ns |
| $f_{ODESU}$ | Output Data Enable Setup | 1.3 | | 1.5 | | 1.7 | | 2.0 | | 2.0 | | ns |

*Notes:*

1. *The –2 and –3 speed grades have been discontinued. Refer to PDN 0104, PDN 0203, PDN 0604, and PDN 1004 at http://www.microsemi.com/soc/support/notifications/default.aspx#pdn.*
2. *Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual worst-case performance. Post-route timing is based on actual routing delay measurements performed on the device prior to shipment.*

## A1460A, A14V60A Timing Characteristics

***Table 2-30*** **• A1460A, A14V60A Worst-Case Commercial Conditions, VCC = 4.75 V, $T_J$ = 70°C[1]**

| **Logic Module Propagation Delays[2]** | | **–3 Speed[3]** | | **–2 Speed [3]** | | **–1 Speed** | | **Std. Speed** | | **3.3 V Speed[1]** | | **Units** |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **Parameter/Description** | | **Min.** | **Max.** | **Min.** | **Max.** | **Min.** | **Max.** | **Min.** | **Max.** | **Min.** | **Max.** | |
| $t_{PD}$ | Internal Array Module | | 2.0 | | 2.3 | | 2.6 | | 3.0 | | 3.9 | ns |
| $t_{CO}$ | Sequential Clock to Q | | 2.0 | | 2.3 | | 2.6 | | 3.0 | | 3.9 | ns |
| $t_{CLR}$ | Asynchronous Clear to Q | | 2.0 | | 2.3 | | 2.6 | | 3.0 | | 3.9 | ns |
| **Predicted Routing Delays[4]** | | | | | | | | | | | | |
| $t_{RD1}$ | FO = 1 Routing Delay | | 0.9 | | 1.0 | | 1.1 | | 1.3 | | 1.7 | ns |
| $t_{RD2}$ | FO = 2 Routing Delay | | 1.2 | | 1.4 | | 1.6 | | 1.8 | | 2.4 | ns |
| $t_{RD3}$ | FO = 3 Routing Delay | | 1.4 | | 1.6 | | 1.8 | | 2.1 | | 2.8 | ns |
| $t_{RD4}$ | FO = 4 Routing Delay | | 1.7 | | 1.9 | | 2.2 | | 2.5 | | 3.3 | ns |
| $t_{RD8}$ | FO = 8 Routing Delay | | 2.8 | | 3.2 | | 3.6 | | 4.2 | | 5.5 | ns |
| **Logic Module Sequential Timing** | | | | | | | | | | | | |
| $t_{SUD}$ | Flip-Flop Data Input Setup | 0.5 | | 0.6 | | 0.7 | | 0.8 | | 0.8 | | ns |
| $t_{HD}$ | Flip-Flop Data Input Hold | 0.0 | | 0.0 | | 0.0 | | 0.0 | | 0.0 | | ns |
| $t_{SUD}$ | Latch Data Input Setup | 0.5 | | 0.6 | | 0.7 | | 0.8 | | 0.8 | | ns |
| $t_{HD}$ | Latch Data Input Hold | 0.0 | | 0.0 | | 0.0 | | 0.0 | | 0.0 | | ns |
| $t_{WASYN}$ | Asynchronous Pulse Width | 2.4 | | 3.2 | | 3.8 | | 4.8 | | 6.5 | | ns |
| $t_{WCLKA}$ | Flip-Flop Clock Pulse Width | 2.4 | | 3.2 | | 3.8 | | 4.8 | | 6.5 | | ns |
| $t_A$ | Flip-Flop Clock Input Period | 5.0 | | 6.8 | | 8.0 | | 10.0 | | 13.4 | | ns |
| $f_{MAX}$ | Flip-Flop Clock Frequency | | 200 | | 150 | | 125 | | 100 | | 75 | MHz |

*Notes:*

1. *VCC = 3.0 V for 3.3 V specifications.*
2. *For dual-module macros, use $t_{PD} + t_{RD1} + t_{PDn} + t_{CO} + t_{RD1} + t_{PDn}$ or $t_{PD1} + t_{RD1} + t_{SUD}$, whichever is appropriate.*
3. *The –2 and –3 speed grades have been discontinued. Refer to PDN 0104, PDN 0203, PDN 0604, and PDN 1004 at http://www.microsemi.com/soc/support/notifications/default.aspx#pdn.*
4. *Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual worst-case performance. Post-route timing is based on actual routing delay measurements performed on the device prior to shipment.*

## A14100A, A14V100A Timing Characteristics

***Table 2-34*** **• A14100A, A14V100A Worst-Case Commercial Conditions, VCC = 4.75 V, $T_J$ = 70°C[1]**

| **Logic Module Propagation Delays[2]** | | **–3 Speed[3]** | | **–2 Speed [3]** | | **–1 Speed** | | **Std. Speed** | | **3.3 V Speed[1]** | | **Units** |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **Parameter/Description** | | **Min.** | **Max.** | **Min.** | **Max.** | **Min.** | **Max.** | **Min.** | **Max.** | **Min.** | **Max.** | |
| $t_{PD}$ | Internal Array Module | | 2.0 | | 2.3 | | 2.6 | | 3.0 | | 3.9 | ns |
| $t_{CO}$ | Sequential Clock to Q | | 2.0 | | 2.3 | | 2.6 | | 3.0 | | 3.9 | ns |
| $t_{CLR}$ | Asynchronous Clear to Q | | 2.0 | | 2.3 | | 2.6 | | 3.0 | | 3.9 | ns |
| **Predicted Routing Delays[4]** | | | | | | | | | | | | |
| $t_{RD1}$ | FO = 1 Routing Delay | | 0.9 | | 1.0 | | 1.1 | | 1.3 | | 1.7 | ns |
| $t_{RD2}$ | FO = 2 Routing Delay | | 1.2 | | 1.4 | | 1.6 | | 1.8 | | 2.4 | ns |
| $t_{RD3}$ | FO = 3 Routing Delay | | 1.4 | | 1.6 | | 1.8 | | 2.1 | | 2.8 | ns |
| $t_{RD4}$ | FO = 4 Routing Delay | | 1.7 | | 1.9 | | 2.2 | | 2.5 | | 3.3 | ns |
| $t_{RD8}$ | FO = 8 Routing Delay | | 2.8 | | 3.2 | | 3.6 | | 4.2 | | 5.5 | ns |
| **Logic Module Sequential Timing** | | | | | | | | | | | | |
| $t_{SUD}$ | Flip-Flop Data Input Setup | 0.5 | | 0.6 | | 0.8 | | 0.8 | | 0.8 | | ns |
| $t_{HD}$ | Flip-Flop Data Input Hold | 0.0 | | 0.0 | | 0.5 | | 0.5 | | 0.5 | | ns |
| $t_{SUD}$ | Latch Data Input Setup | 0.5 | | 0.6 | | 0.8 | | 0.8 | | 0.8 | | ns |
| $t_{HD}$ | Latch Data Input Hold | 0.0 | | 0.0 | | 0.5 | | 0.5 | | 0.5 | | ns |
| $t_{WASYN}$ | Asynchronous Pulse Width | 2.4 | | 3.2 | | 3.8 | | 4.8 | | 6.5 | | ns |
| $t_{WCLKA}$ | Flip-Flop Clock Pulse Width | 2.4 | | 3.2 | | 3.8 | | 4.8 | | 6.5 | | ns |
| $t_A$ | Flip-Flop Clock Input Period | 5.0 | | 6.8 | | 8.0 | | 10.0 | | 13.4 | | ns |
| $f_{MAX}$ | Flip-Flop Clock Frequency | | 200 | | 150 | | 125 | | 100 | | 75 | MHz |

*Notes:*

1. *VCC = 3.0 V for 3.3 V specifications.*
2. *For dual-module macros, use* $t_{PD} + t_{RD1} + t_{PDn} + t_{CO} + t_{RD1} + t_{PDn}$ *or* $t_{PD1} + t_{RD1} + t_{SUD}$*, whichever is appropriate.*
3. *The –2 and –3 speed grades have been discontinued. Refer to PDN 0104, PDN 0203, PDN 0604, and PDN 1004 at http://www.microsemi.com/soc/support/notifications/default.aspx#pdn.*
4. *Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual worst-case performance. Post-route timing is based on actual routing delay measurements performed on the device prior to shipment.*

# Pin Descriptions

**CLKA** **Clock A (Input)**

Clock input for clock distribution networks. The Clock input is buffered prior to clocking the logic modules. This pin can also be used as an I/O.

**CLKB** **Clock B (Input)**

Clock input for clock distribution networks. The Clock input is buffered prior to clocking the logic modules. This pin can also be used as an I/O.

**GND** **Ground**

LOW supply voltage.

**HCLK** **Dedicated (Hard-wired) Array Clock (Input)**

Clock input for sequential modules. This input is directly wired to each S-Module and offers clock speeds independent of the number of S-Modules being driven. This pin can also be used as an I/O.

**I/O** **Input/Output (Input, Output)**

The I/O pin functions as an input, output, three-state, or bidirectional buffer. Input and output levels are compatible with standard TTL and CMOS specifications. Unused I/O pins are tristated by the Designer Series software.

**IOCLK** **Dedicated (Hard-wired) I/O Clock (Input)**

Clock input for I/O modules. This input is directly wired to each I/O module and offers clock speeds independent of the number of I/O modules being driven. This pin can also be used as an I/O.

**IOPCL** **Dedicated (Hard-wired) I/O Preset/Clear (Input)**

Input for I/O preset or clear. This global input is directly wired to the preset and clear inputs of all I/O registers. This pin functions as an I/O when no I/O preset or clear macros are used.

**MODE** **Mode (Input)**

The MODE pin controls the use of diagnostic pins (DCLK, PRA, PRB, SDI). When the MODE pin is HIGH, the special functions are active. When the MODE pin is LOW, the pins function as I/Os. To provide Actionprobe capability, the MODE pin should be terminated to GND through a 10K resistor so that the MODE pin can be pulled high when required.

**NC** **No Connection**

This pin is not connected to circuitry within the device.

**PRA** **Probe A (Output)**

The Probe A pin is used to output data from any user-defined design node within the device. This independent diagnostic pin can be used in conjunction with the Probe B pin to allow real-time diagnostic output of any signal path within the device. The Probe A pin can be used as a user-defined I/O when debugging has been completed. The pin’s probe capabilities can be permanently disabled to protect programmed design confidentiality. PRA is accessible when the MODE pin is HIGH. This pin functions as an I/O when the MODE pin is LOW.

**PRB** **Probe B (Output)**

The Probe B pin is used to output data from any user-defined design node within the device. This independent diagnostic pin can be used in conjunction with the Probe A pin to allow real-time diagnostic output of any signal path within the device. The Probe B pin can be used as a user-defined I/O when debugging has been completed. The pin’s probe capabilities can be permanently disabled to protect programmed design confidentiality. PRB is accessible when the MODE pin is HIGH. This pin functions as an I/O when the MODE pin is LOW.

**SDI** **Serial Data Input (Input)**

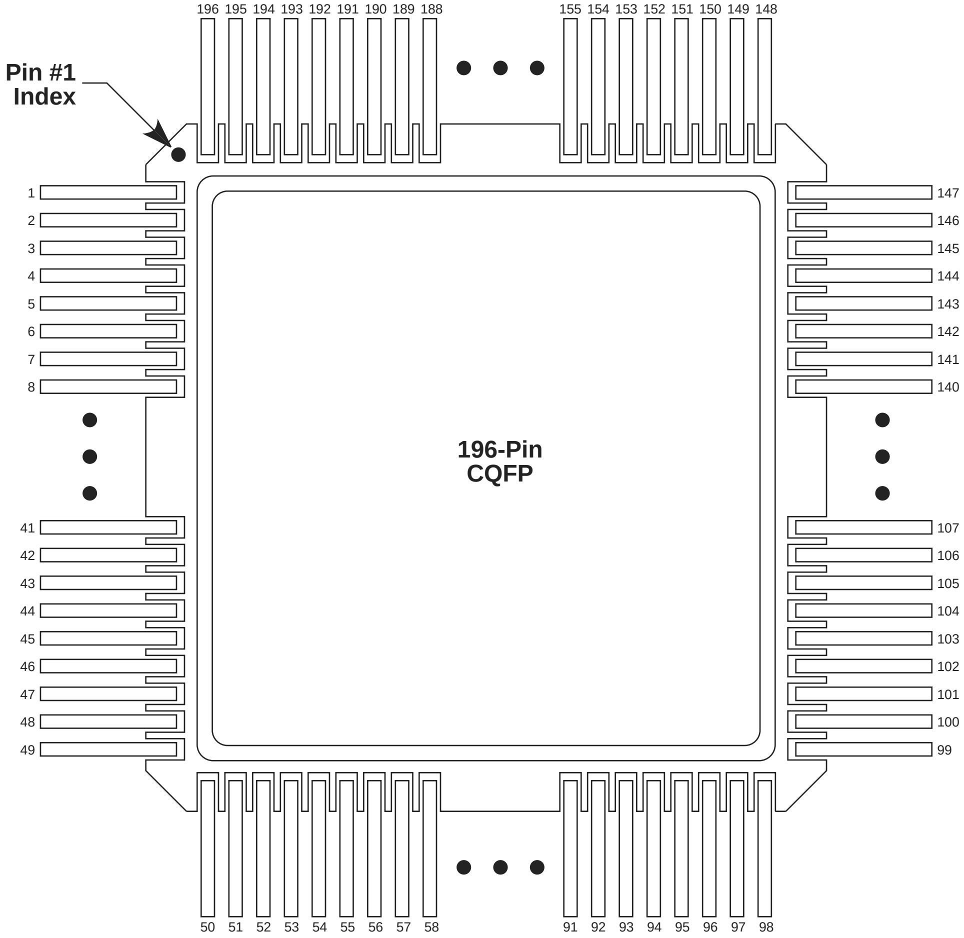
Serial data input for diagnostic probe and device programming. SDI is active when the MODE pin is HIGH. This pin functions as an I/O when the MODE pin is LOW.

| **PL84** | | | |
|---|---|---|---|
| **Pin Number** | **A1415, A14V15 Function** | **A1425, A14V25 Function** | **A1440, A14V40 Function** |
| 1 | VCC | VCC | VCC |
| 2 | GND | GND | GND |
| 3 | VCC | VCC | VCC |
| 4 | PRA, I/O | PRA, I/O | PRA, I/O |
| 11 | DCLK, I/O | DCLK, I/O | DCLK, I/O |
| 12 | SDI, I/O | SDI, I/O | SDI, I/O |
| 16 | MODE | MODE | MODE |
| 27 | GND | GND | GND |
| 28 | VCC | VCC | VCC |
| 40 | PRB, I/O | PRB, I/O | PRB, I/O |
| 41 | VCC | VCC | VCC |
| 42 | GND | GND | GND |
| 43 | VCC | VCC | VCC |
| 45 | HCLK, I/O | HCLK, I/O | HCLK, I/O |
| 52 | SDO | SDO | SDO |
| 53 | IOPCL, I/O | IOPCL, I/O | IOPCL, I/O |
| 59 | VCC | VCC | VCC |
| 60 | VCC | VCC | VCC |
| 61 | GND | GND | GND |
| 68 | VCC | VCC | VCC |
| 69 | GND | GND | GND |
| 74 | IOCLK, I/O | IOCLK, I/O | IOCLK, I/O |
| 83 | CLKA, I/O | CLKA, I/O | CLKA, I/O |
| 84 | CLKB, I/O | CLKB, I/O | CLKB, I/O |

*Notes:*

1. All unlisted pin numbers are user I/Os.
2. NC denotes no connection.
3. MODE should be terminated to GND through a 10K resistor to enable Actionprobe usage; otherwise it can be terminated directly to GND.

## CQ196



*Note: This is the top view.*

### *Note*

For Package Manufacturing and Environmental information, visit the Resource Center at http://www.microsemi.com/soc/products/solutions/package/docs.aspx

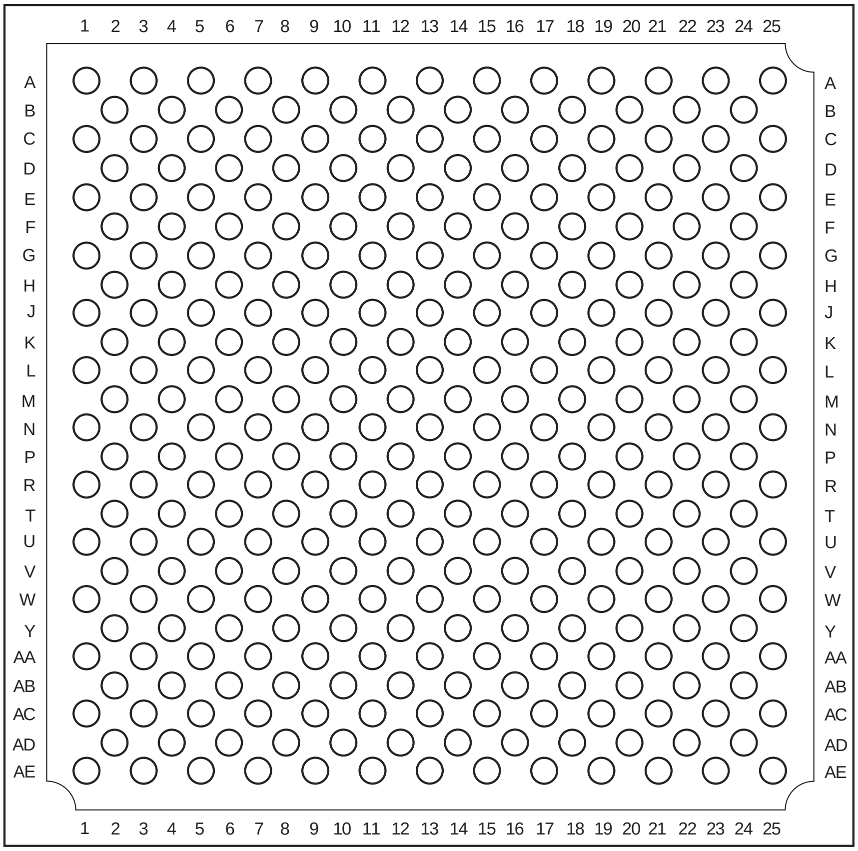
| CQ256 | |
|---|---|
| **Pin Number** | **A14100 Function** |
| 1 | GND |
| 2 | SDI, I/O |
| 11 | MODE |
| 28 | VCC |
| 29 | GND |
| 30 | VCC |
| 31 | GND |
| 46 | VCC |
| 59 | GND |
| 90 | PRB, I/O |
| 91 | GND |
| 92 | VCC |
| 93 | GND |
| 94 | VCC |
| 96 | HCLK, I/O |
| 110 | GND |
| 126 | SDO |
| 127 | IOPCL, I/O |
| 128 | GND |

| CQ256 | |
|---|---|
| **Pin Number** | **A14100 Function** |
| 141 | VCC |
| 158 | GND |
| 159 | VCC |
| 160 | GND |
| 161 | VCC |
| 174 | VCC |
| 175 | GND |
| 176 | GND |
| 188 | IOCLK, I/O |
| 189 | GND |
| 219 | CLKA, I/O |
| 220 | CLKB, I/O |
| 221 | VCC |
| 222 | GND |
| 223 | VCC |
| 224 | GND |
| 225 | PRA, I/O |
| 240 | GND |
| 256 | DCLK, I/O |

*Notes:*

1. All unlisted pin numbers are user I/Os.
2. NC denotes no connection.
3. MODE should be terminated to GND through a 10K resistor to enable Actionprobe usage; otherwise it can be terminated directly to GND.

## BG313



*Note: This is the top view.*

## *Note*

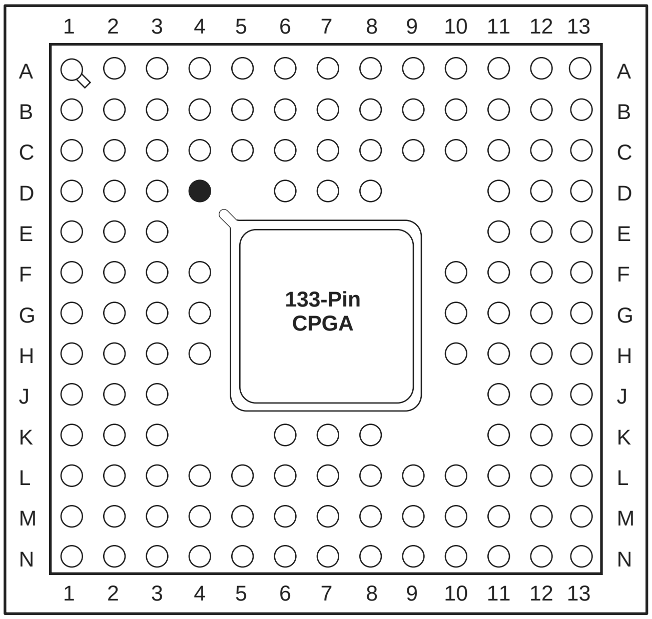
For Package Manufacturing and Environmental information, visit the Resource Center at http://www.microsemi.com/soc/products/solutions/package/docs.aspx

| PG100 | |
|---|---|
| **A1415 Function** | **Location** |
| CLKA or I/O | C7 |
| CLKB or I/O | D6 |
| DCLK or I/O | C4 |
| GND | C3, C6, C9, E9, F3, F9, J3, J6, J8, J9 |
| HCLK or I/O | H6 |
| IOCLK or I/O | C10 |
| IOPCL or I/O | K9 |
| MODE | C2 |
| PRA or I/O | A6 |
| PRB or I/O | L3 |
| SDI or I/O | B3 |
| SDO | L9 |
| VCC | B6, B10, E11, F2, F10, G2, K2, K6, K10 |

*Notes:*

1. All unlisted pin numbers are user I/Os.
2. NC denotes no connection.
3. MODE should be terminated to GND through a 10K resistor to enable Actionprobe usage; otherwise it can be terminated directly to GND.
4. The PG100 package has been discontinued.

# PG133



*Note: This is the top view.*

## *Note*

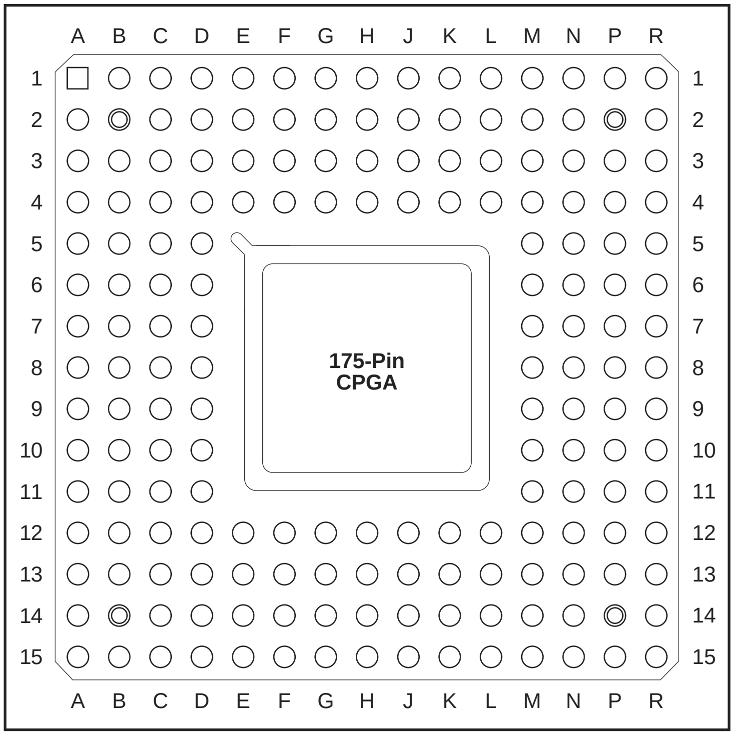
For Package Manufacturing and Environmental information, visit the Resource Center at http://www.microsemi.com/soc/products/solutions/package/docs.aspx

| PG133 | |
|---|---|
| **A1425 Function** | **Location** |
| CLKA or I/O | D7 |
| CLKB or I/O | B6 |
| DCLK or I/O | D4 |
| GND | A2, C3, C7, C11, C12, F10, G3, G11, L3, L7, L11, M3, N12 |
| HCLK or I/O | K7 |
| IOCLK or I/O | C10 |
| IOPCL or I/O | L10 |
| MODE | E3 |
| NC | A1, A7, A13, G1, G13, N1, N7, N13 |
| PRA or I/O | A6 |
| PRB or I/O | L6 |
| SDI or I/O | C2 |
| SDO | M11 |
| VCC | B2, B7, B12, E11, G2, G12, J2, J12, M2, M7, M12 |

*Notes:*

1. All unlisted pin numbers are user I/Os.
2. NC denotes no connection.
3. MODE should be terminated to GND through a 10K resistor to enable Actionprobe usage; otherwise it can be terminated directly to GND.
4. The PG133 package has been discontinued.

# PG175



*Note: This is the top view.*

## *Note*

For Package Manufacturing and Environmental information, visit the Resource Center at http://www.microsemi.com/soc/products/solutions/package/docs.aspx

| PG257 | |
|---|---|
| **A14100 Function** | **Location** |
| CLKA or I/O | L4 |
| CLKB or I/O | L5 |
| DCLK or I/O | E4 |
| GND | B16, C4, D4, D10, D16, E11, J5, K4, K16, L15, R4, T4, T10, T16, T17, X7 |
| HCLK or I/O | J16 |
| IOCLK or I/O | T5 |
| IOPCL or I/O | R16 |
| MODE | A5 |
| NC | E5 |
| PRA or I/O | J1 |
| PRB or I/O | J17 |
| SDI or I/O | B4 |
| SDO | R17 |
| VCC | C3, C10, C13, C17, K3, K17, V3, V7, V10, V17, X14 |

*Notes:*

1. All unlisted pin numbers are user I/Os.
2. NC denotes no connection.
3. MODE should be terminated to GND through a 10K resistor to enable Actionprobe usage; otherwise it can be terminated directly to GND.

| **Revision** | **Changes** | **Page** |
|---|---|---|
| Revision 2 (continued) | In the "Package Pin Assignments" section, notes were added to the pin tables for the following packages, stating that they are discontinued: | |
| | "BG225" | 3-20 |
| | "PG100" | 3-24 |
| | "PG133" | 3-26 |
| | "PG175" | 3-28 |
| Revision 1 (June 2006) | RoHS compliant information was added to the "Ordering Information" section. | II |

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